AMD AM4 B550

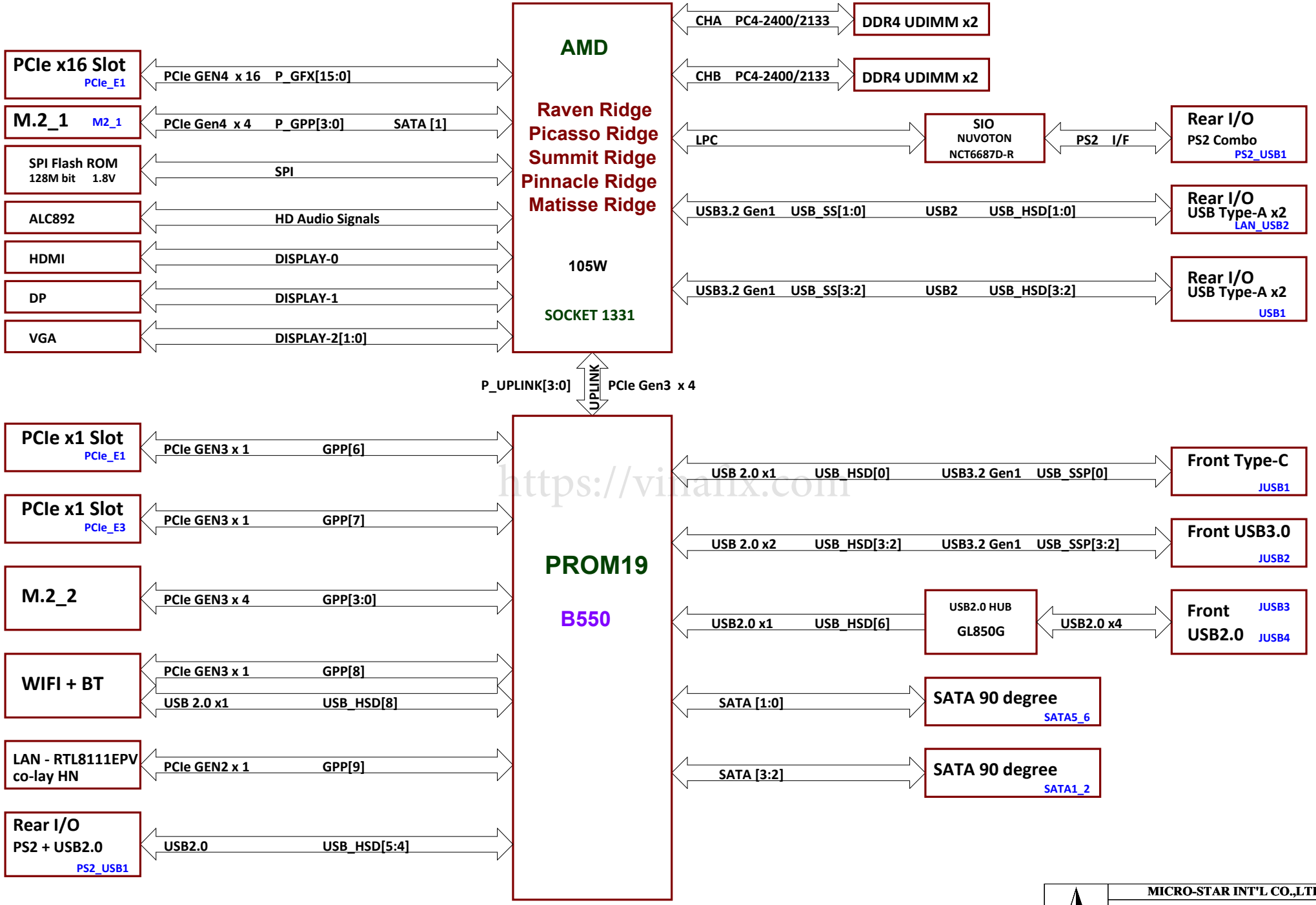
M-ATX (243.84 X 243.84)

MICRO-STAR INT'L CO.,LTD

MS-7C95

Size: Custom | Document Description: 01 Cover Sheet | Rev: 10

Date: Wednesday, April 29, 2020 | Sheet 1 of 74



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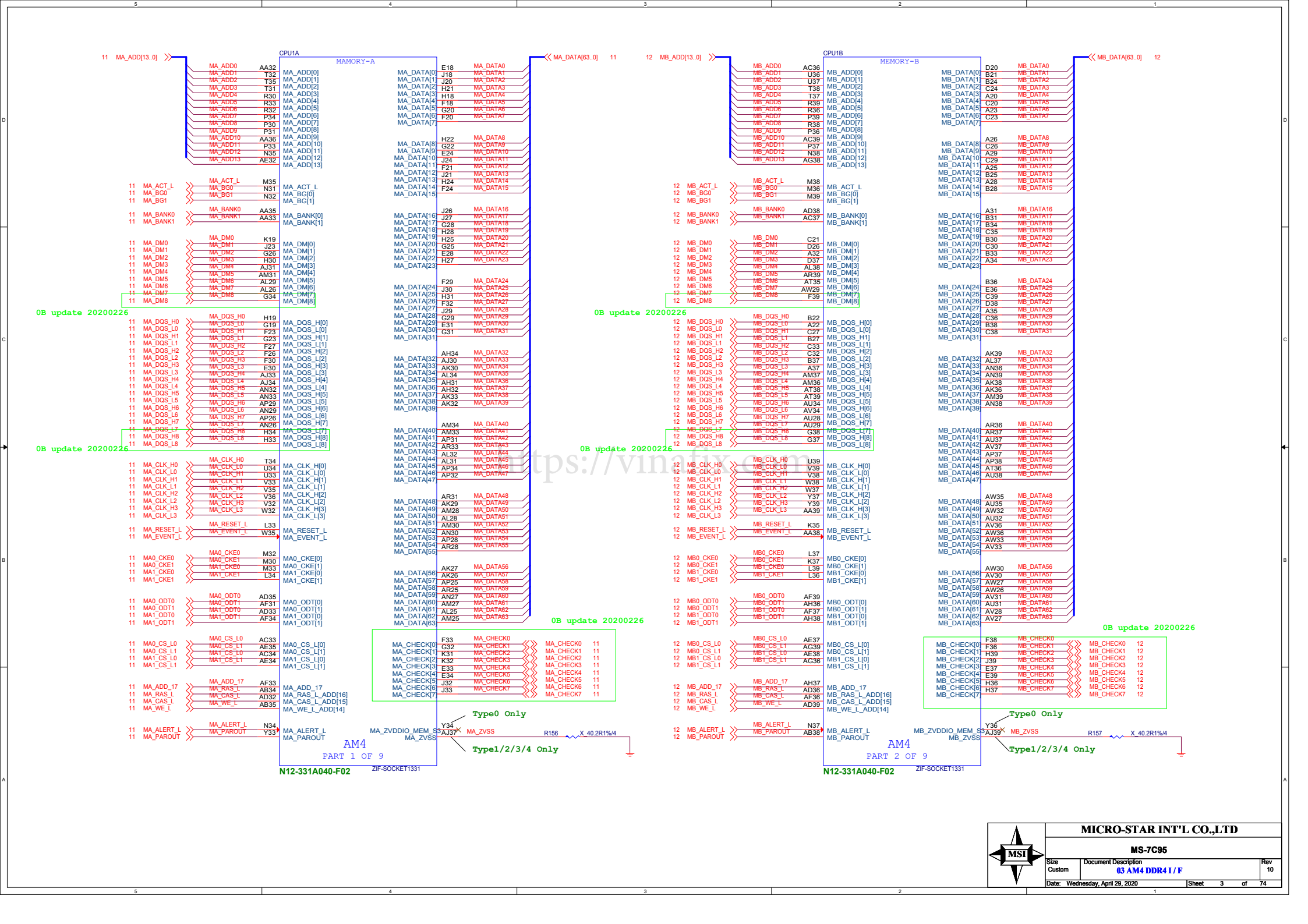
Size: Custom | Document Description: 02 Block Diagram | Rev: 10

Date: Wednesday, April 29, 2020 | Sheet 2 of 74



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MS-7C95

Size	Document Description	Rev
Custom	03 AM4 DDR4 I / F	10

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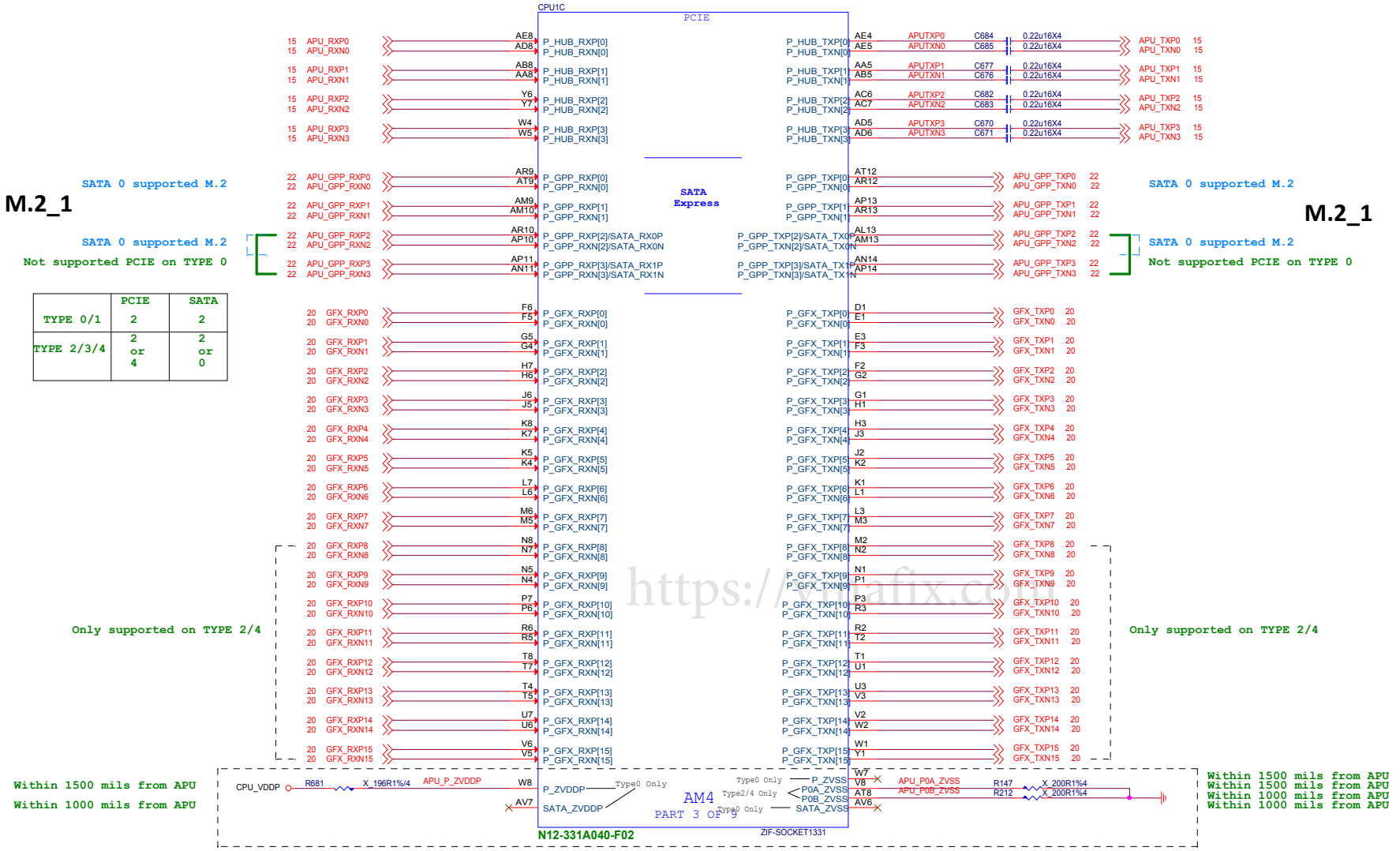
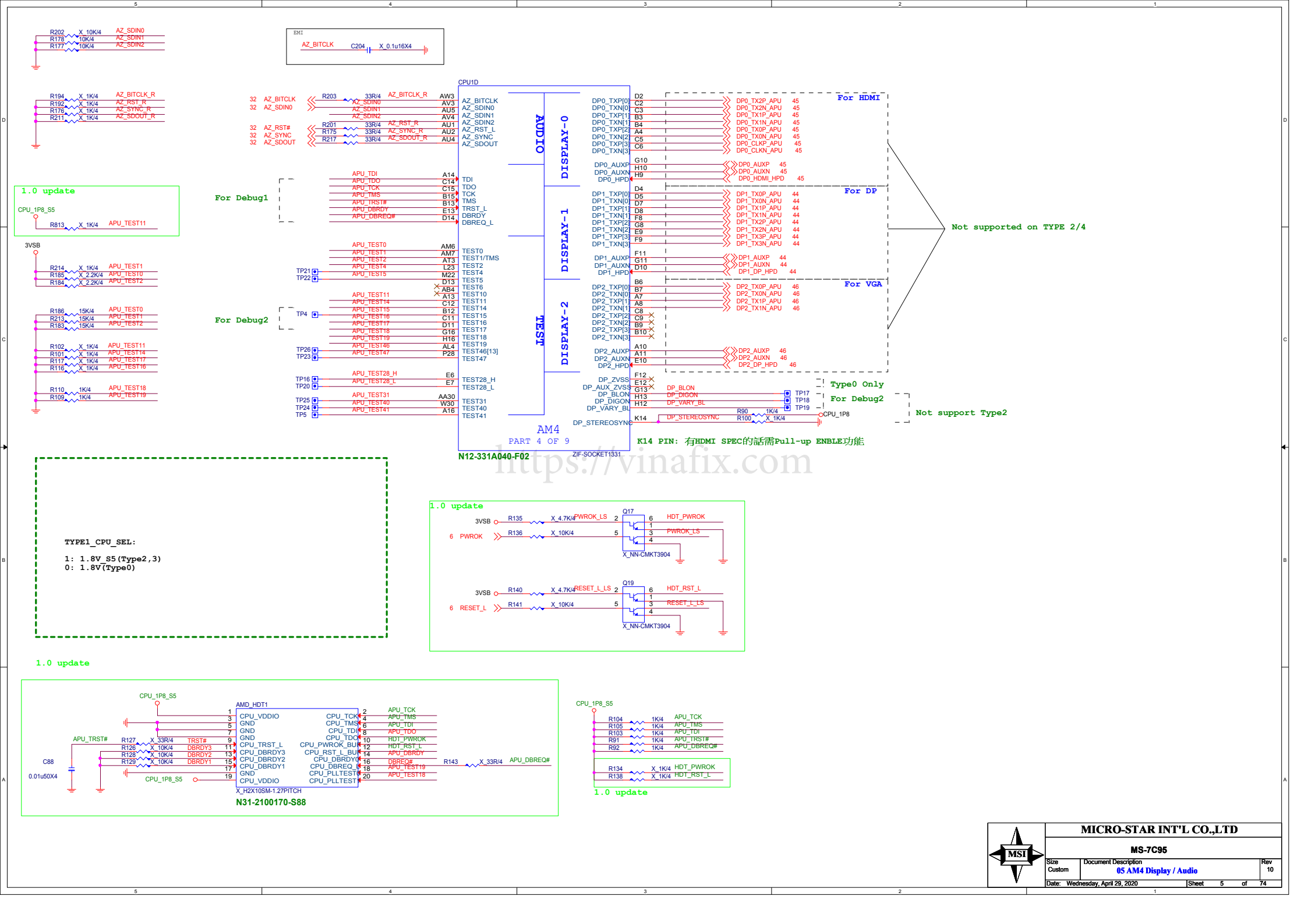


MICRO-STAR INT'L CO.,LTD	
MS-7C95	
Size: Custom	Document Description: 04 AM4 PCIE / SATAE — Rev: 10
Date: Wednesday, April 29, 2020	Sheet 4 of 74



MICRO-STAR INT'L CO.,LTD	
MS-7C95	
Size: Custom	Document Description: 05 AM4 Display / Audio
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1.0 update FIX SMBUS PK-PK issue

Closed FAN , by S0ix.

25,27,28,29,30 FAN_EN
CPU_S0_IDLE
Q34 X_2N7002
R301 100K/4

3VSB C226 0.1u16X4
U18
25,34,44,52,54,57,61 SLP_S3#
R207 100K/4
AHCT1G126GV_SOT23-5-RH
APU_S0A3_GPIO
APU_SLP_S3#
R181 2.2K/4
R180 100K/4
APU_SLP_S3#
1:See APU_S0A3_GPIO
0:High-IMpedance
T33-1G12629-T07
AVL:T33-1G12619-N78
SLP_S3# R206 X_0R/4 APU_SLP_S3#

3VSB R743 10K/4
Q84 2N7002D
G2 D2 D1 S2 G1 S1
25,54,65 CHIP_PWGD
+12V R734 2.7K/4
C1658 0.1u16X4
Q82 2N7002
Q81 2N7002
SCLK0_3VSB 31,40,64
SCLK0 6,11,22,59
SDATA0_3VSB 31,40,64
SDATA0 6,11,22,59

VCC3
SCLK0_R R279 4.7K/4
SDATA0_R R283 4.7K/4
SCLK0_3VSB R384 4.7K/4
SDATA0_3VSB R396 4.7K/4
SCLK1 R162 2.2K/4
SDATA1 R163 2.2K/4
PE2_PE3_WAKE# R678 10K/4
PEGX16_WAKE# R680 10K/4
M22_PE4_WAKE# R679 10K/4
LAN_WAKE# R165 10K/4

VCC3
R107 1K/4 APU_ALERT#
R78 1K/4 APU_PROCHOT#
R111 1K/4 APU_THERMTRIP#

CPU_1P8
Within 500mils
R94 1K/4 APU_SIC
R95 1K/4 APU_SID
R106 300R/4 PWROK
R108 300R/4 RESET_L
Follow CRB

Add for HDT and close to PIN E16 & B16
5 PWROK PWROK
5 RESET_L RESET_L

3VSB
R209 10K/4 PWRBTN#
R234 X_10K/4 APU_AM4R1
R220 10K/4 BLINK
R200 10K/4 APU_WAKE#
R195 10K/4 PCIE_RST
C216 100p50N4 PCIE_REST#

CPU_1P8_S5A
R224 22K/4 RSMRST#
C637 10u6.3X6
C233 1u6.3X4

C68 X_0.1u16X4 APU_PWROK
最新公板Oogir_RevD，新增C2470,請預留不上件

3VSB
Level 3.3V U20
C246 X_0.1u16X4
24 WIFI_BT_RTCCLK
RTCCLK
MC74VHC1GT50DFT1G_SC70-5-RH

For Moderm Standby Fail Use 1.0 update

APU_WAKE# PE2_PE3_WAKE#	R799 R800	X_0R/4 0R/4	PE2_PE3_WK#	PE2_PE3_WK#	21,24
APU_WAKE# PEGX16_WAKE#	R801 R802	X_0R/4 0R/4	PEGX16_WK#	PEGX16_WK#	20
APU_WAKE# M22_PE4_WAKE#	R803 R804	X_0R/4 0R/4	M22_PE4_WK#	M22_PE4_WK#	23
APU_WAKE# LAN_WAKE#	R805 R806	X_0R/4 0R/4	LAN_WK#	LAN_WK#	31

CPU1E

47 APU_SVC	D17	SVC	SVI
47 APU_SVD	C17	SVD	
47 APU_SVT	A17	SVT	
47 APU_PWROK	E16	PWROK	ACPI
54 ALL_PWR_PWRGD	AM3	PWR_GOOD	
	B16	RESET_L	
25,47 APU_PROCHOT#	H15	PROCHOT_L	
	A19	THERMTRIP_L	
25,34,55,57,61 SLP_S5#	AT2	SLP_S3_L	GPIO
	AP2	SLP_S5_L	
APU_S0A3_GPIO	AR3	S0A3_GPIO/AGPIO10/SGPIO0_CLK	
S5_MUX_CTRL	AP4	S5_MUX_CTRL/EGPIO42	
25 PWRBTN#	AN5	PWR_BTN_L/AGPIO0	
BLINK	AT5	BLINK/AGPIO11	
62 SPKR	AW23	SPKR/AGPIO91	
25,54 RSMRST#	AP5	RSMRST_L	MISC
7,54,58,62 SYSRESET#	AM4	SYS_RESET_L/AGPIO1	
7,17,20,22,24,31 PCIE_REST#	AL7	PCIE_RST_L/EGPIO26	
25 KBRST#	AN24	ESPI_RESET_L/KBRST_L	
17,22 APU_WAKE#	AL5	WAKE_L/AGPIO2	
17,25 APU_LPC_PME#	AL2	LPC_PME_L/AGPIO22	
25 APU_SIC	B18	SIC	
25 APU_SID	C18	SID	
APU_ALERT#	D16	ALERT_L	
53,55,61 APU_AM4R1	AL8	AM4R1	
CORETYPE0	AM24	CORETYPE[0]	OC
CORETYPE1	AN9	CORETYPE[1]	
TP30 AGPIO84	AN23	FANIN0/AGPIO84	FAN
	AP23	FANOUT0/AGPIO85	
7 RTCCLK	AP8	RTCCLK	RTC
APU_32K_X1	AW5	X32K_X1	
APU_32K_X2	AW6	X32K_X2	
	AM4		SENSE
	PART 5 OF 9		

N12-331A040-F02 ZIF-SOCKET1331

0B update 20200313
R93 X_R/2 PWROK
KBRST# D4 RESET_L
3.3V X_S-1RB520S-40TTG 1.8V
R797 X_R/2 APU_SLP_S3#
SLP_S3#_R
APU_S0A3_GPIO
S5_MUX_CTRL
TP28

Turn off power when BIOS into deep mode
APU_AM4R1
Q61 2N7002
25,57,61 DEEP_S5

Level 1.8V S5 Domain
7 RTCCLK

0B update 20200313
AU25 SCL0_R R792 0R/4 R280 X_0R/4 SIO_SMB_MSCL 25,46,47,59
AV25 SDA0_R R793 0R/4 R284 X_0R/4 SIO_SMB_MSDA 25,46,47,59
SDATA0 6,11,22,59
SCL0/I2C2_SCL/EGPIO113
SDA0/I2C2_SDA/EGPIO114
AK3 SCLK1 20
AK2 SDATA1 20
SCL1/I2C3_SCL/AGPIO19
SDA1/I2C3_SDA/AGPIO20

AT6 PE2_PE3_WAKE#
AR6 M2_1_SATA_DET 22
AP22 DEVSLP1 22
AN8 CPU_S0_IDLE 55
AP7 LAN_ISOLATEB 31
AN2 AGPIO9
AN3 PEGX16_WAKE#
AR4 M22_PE4_WAKE#
AW17 M2_1_CARD_DET 22
AV22 GENINT1_L
AU23
AM22 SATA_LED# 62
AGPIO3
AGPIO4
AGPIO5/DEVSLP0
AGPIO6
AGPIO8
AGPIO9/SGPIO0_DATAOUT
AGPIO23/SGPIO0_LOAD
AGPIO40/SGPIO0_DATAIN
AGPIO86
GENINT1_L/AGPIO89
GENINT2_L/AGPIO90
SATA_ACT_L/AGPIO130

For Select Auto or Manual
VCC3
R232 8.2K/4 GENINT1_L
R223 X_10K/4
AMD Hardware Validated Boot (HVB)
0 or NC:Disable
1:Enable

AT18 PM_PESLOT_AUX_RST# 21
AW11 PEGX16_AUX_RST# 20
AV12 EGPIO96_DRAM 63
AW12 WIFI_AUX_RST# 24
AU13 PM19_AUX_RST# 17
AV13 M21_AUX_RST# 22
AT14 LAN_AUX_RST# 31
EGPIO70
EGPIO95
EGPIO96
EGPIO97
EGPIO98
EGPIO99
EGPIO100

AT23 CLK_REQ0
AV24 CLK_REQ1_M.2
AT24 CLK_REQ2
AL23 PM19_CLK_REQ_L
AR22 CLK_REQG
CLK_REQ0_L/SATA_IS0_L/SATA_ZP0_L/AGPIO115
CLK_REQ1_L/AGPIO116
CLK_REQ2_L/AGPIO117
CLK_REQ3_L/SATA_IS1_L/SATA_ZP1_L/EGPIO118
CLK_REQG_L/OSCIN/EGPIO132
CLK_REQ1_M.2 22 M2_1
PM19_CLK_REQ_L 17 RROM19 X16
CLK_REQG 20

AL1 APU_OC0
AM1 LAN_WAKE#
AR1
AP1
USB_OC0_L/AGPIO10
USB_OC1_L/TDI/AGPIO11
USB_OC2_L/TCK/AGPIO12
USB_OC3_L/TDO/AGPIO24
APU_OC0 43
3VSB
APU_OC0 R164 200K/4

teknisi indonesia

F14 VDDCR_CPU_SENSE
E15 VDDCR_SOC_SENSE
VDDCR_CPU_SENSE+ 26,47
VDDCR_SOC_SENSE+ 47
G14 VDDIO_MEM_S3_SENSE
F15 VSS_SENSE_A
CP18 CP17 X_COPPER
VDDIO_MEM_S3_SENSE 55
VDDCR_CPU_SENSE- 47
VDDCR_SOC_SENSE- 47
AL22 CPU_VDDP_SENSE
AM23 VSS_SENSE_B
TP27
CPU_VDDP_SENSE 53

VCC3
R252 560R/4 SATA_LED#
R250 10K/4 CLK_REQ1_M.2
R253 X_10K/4 CLK_REQ2
R248 10K/4 CLK_REQG
R442 10K/4 PM19_CLK_REQ_L
R238 X_10K/4 CLK_REQ0
R246 X_10K/4 CLK_REQ1_M.2
R249 X_10K/4 CLK_REQ2
R653 X_10K/4 PM19_CLK_REQ_L
R237 X_10K/4 CLK_REQG

Layout:Place x'tal within 1.5 inch of APU
APU_32K_X2
Y2 32.768KHZ12.5p
APU_32K_X1
R196 20M/6
C207 12p50N6
C206 12p50N6
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2

AM4 CPU TYPE Circuit

3VSB R227 1K/4
CORETYPE1

ATX_5VSB R404 47K/4
TYPE0_CPU_SEL 7,53,54
TYPE0_CPU_SEL
0:RV
1:BR/SR/PR/MTS
CPU_1P8_S5
R414 1K/4
R415 4.7K/4
CORETYPE0
CORETYPE0R
Q47 2N3904
CORETYPE0
0:BR/SR/PR/MTS
1:RV

IB=(CPU_1P8_S5-Vbe)/5.7k
(1.8-0.95)/5.7k=0.149mA

IC=(VCC5-Vce)/47k
(5-0.2)/47k=0.102mA

CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA	X	1	1
SR	2	1	0
RV/ZP	3	1	1
MTS	4	1	0

3VSB PWR_1P8_SW
R273 10K/4
R274 10K/4
AGPIO9
N-PM514BA Q33
TPM_HOLD# 7

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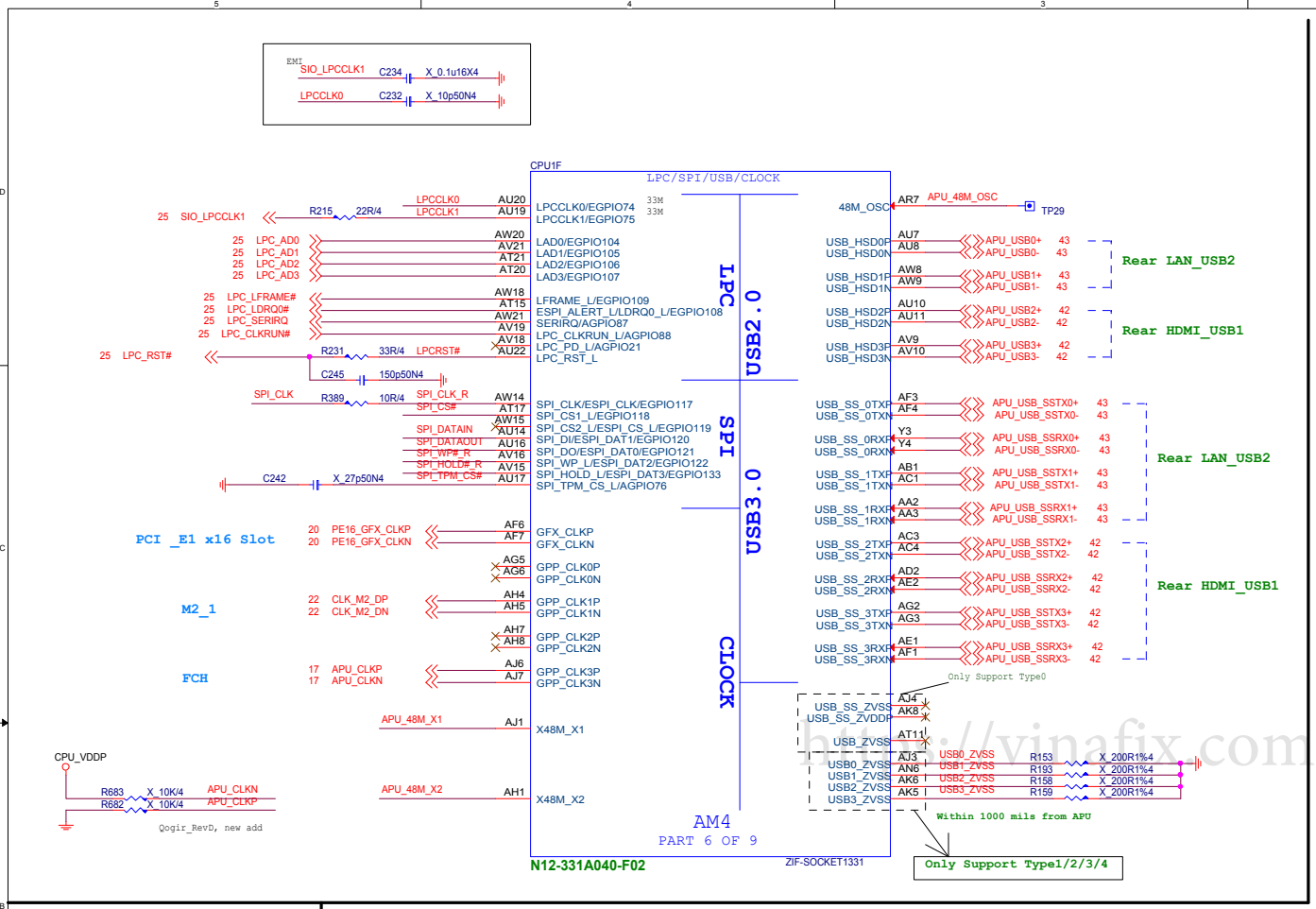
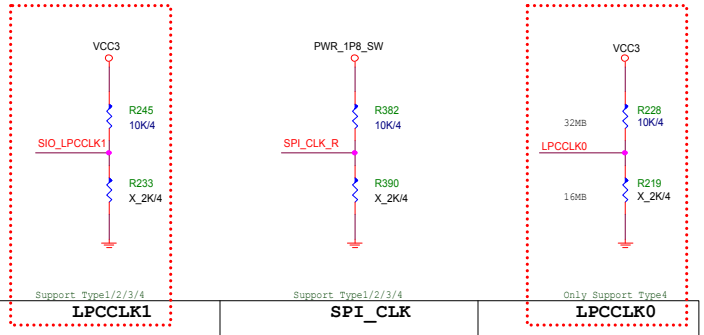


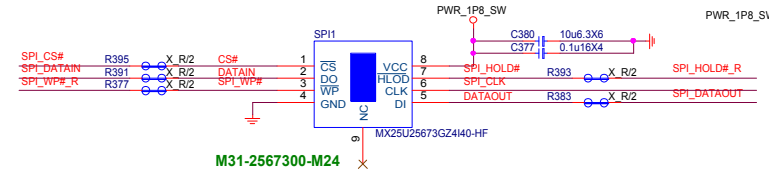
Strapping Options

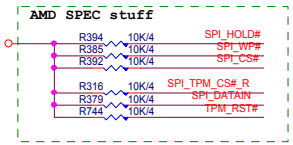


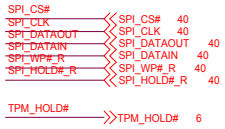
	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator **(Default)**	Use 48Mhz crystal clock and generate both internal and external clocks **(Default)**	PSP should modify SPI page register bits [25:24] to remap physical ROM to upper image **(Default)**
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	PSP should not modify SPI page register bits [25:24]

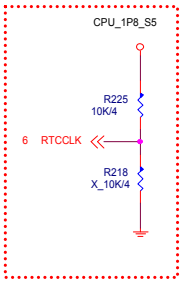
	AGPIO3	LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic	SPI ROM **(Default)**	Normal reset mode **(Default)**
PULL LOW	**(Default)** Traditional Reset logic	LPC ROM	short reset mode

SPI ROM(1.8V)



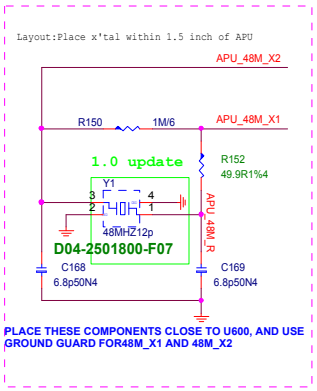


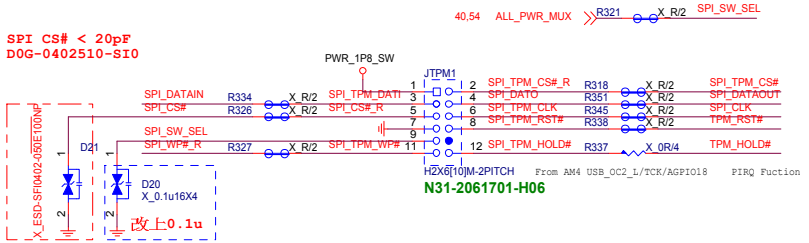


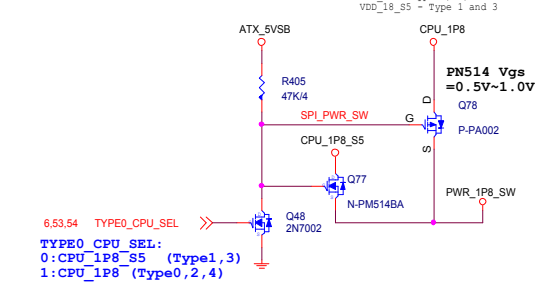


	RTCCLK
PULL HIGH	RTCCLK is input and is used as the bypass clock **(Default)**
PULL LOW	Normal Mode: Use 32Khz xtal as the source of RTC clock

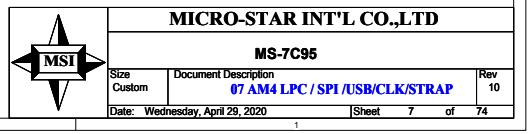
D04-2501800-F07 (Main)
D04-2501000-T16 (AVL)

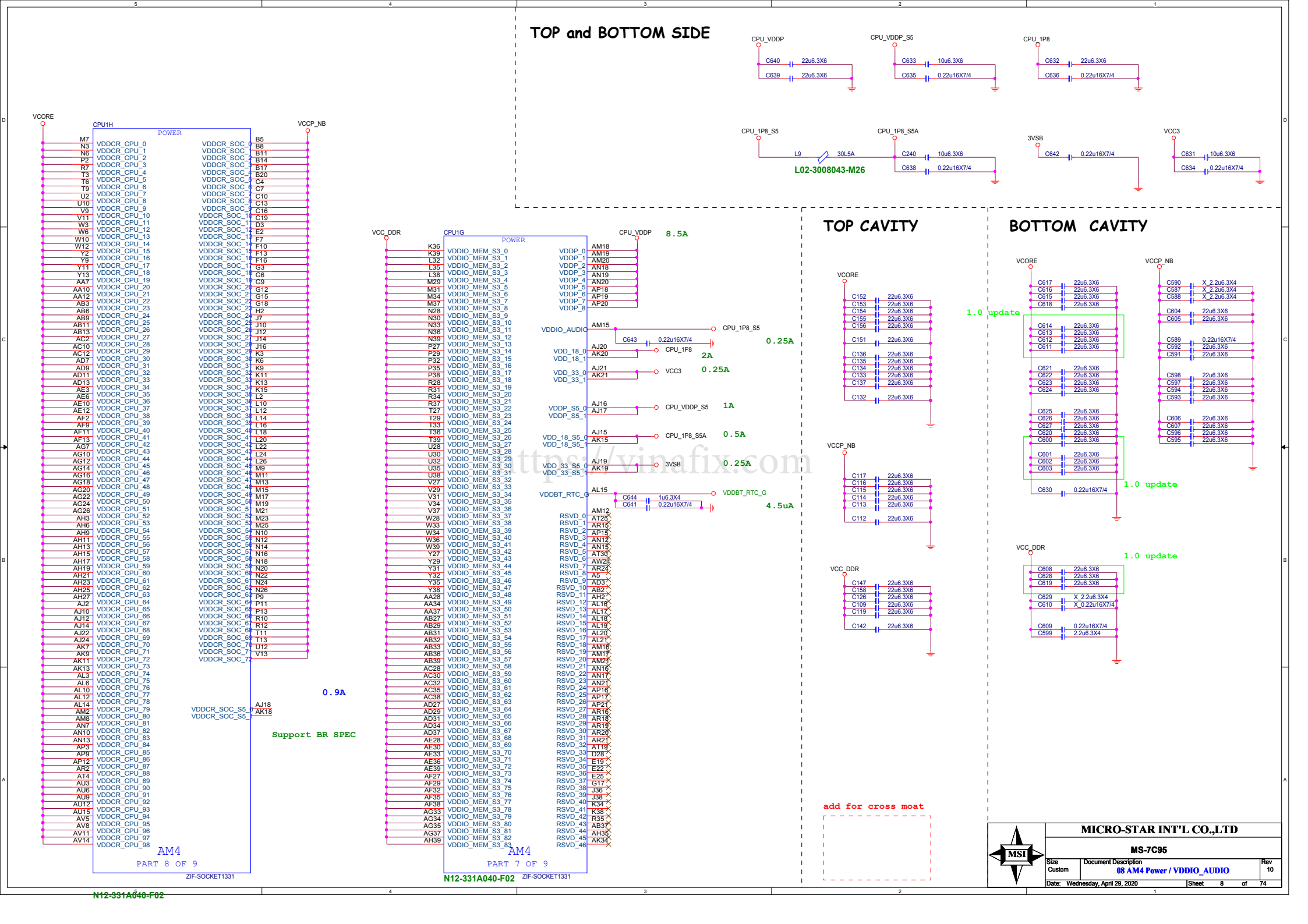


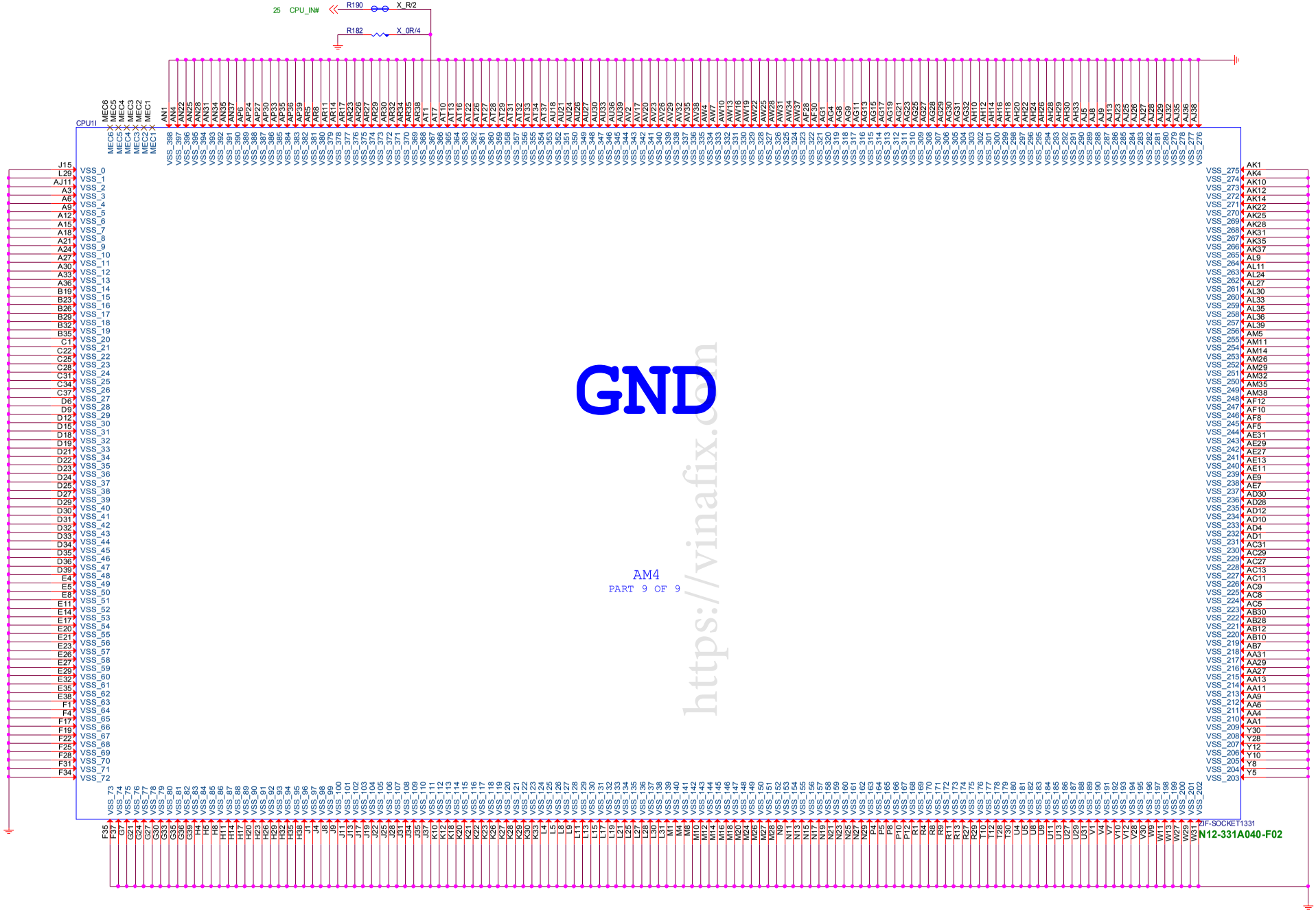




PN514 Vgs =0.5V~1.0V







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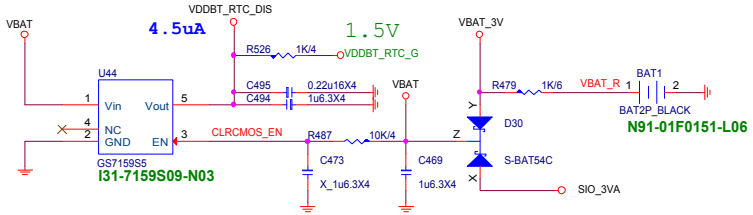
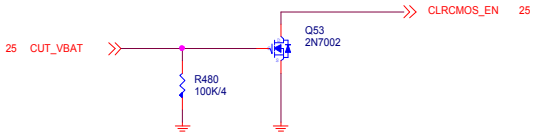
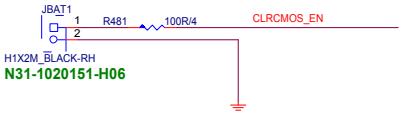
RTC & Clear CMOS Circuit

VDDBT_RTC_G	1.50	All	4.5uA	–	–





Clear CMOS button



RTC Backup

Vinafix.com

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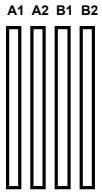

DIMMA1A

DIMMA2A

0B update 20200226

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

DIMM1 (CHANNEL-A) -A0
ADDRESS = 0:0 [SA1:SA0]

DIMM2 (CHANNEL-A) -A4
ADDRESS = 1:0 [SA1:SA0]

DDRIV-288P_BLACK-RH-23

N13-2881271-L06

AVL: N13-2880441-F02

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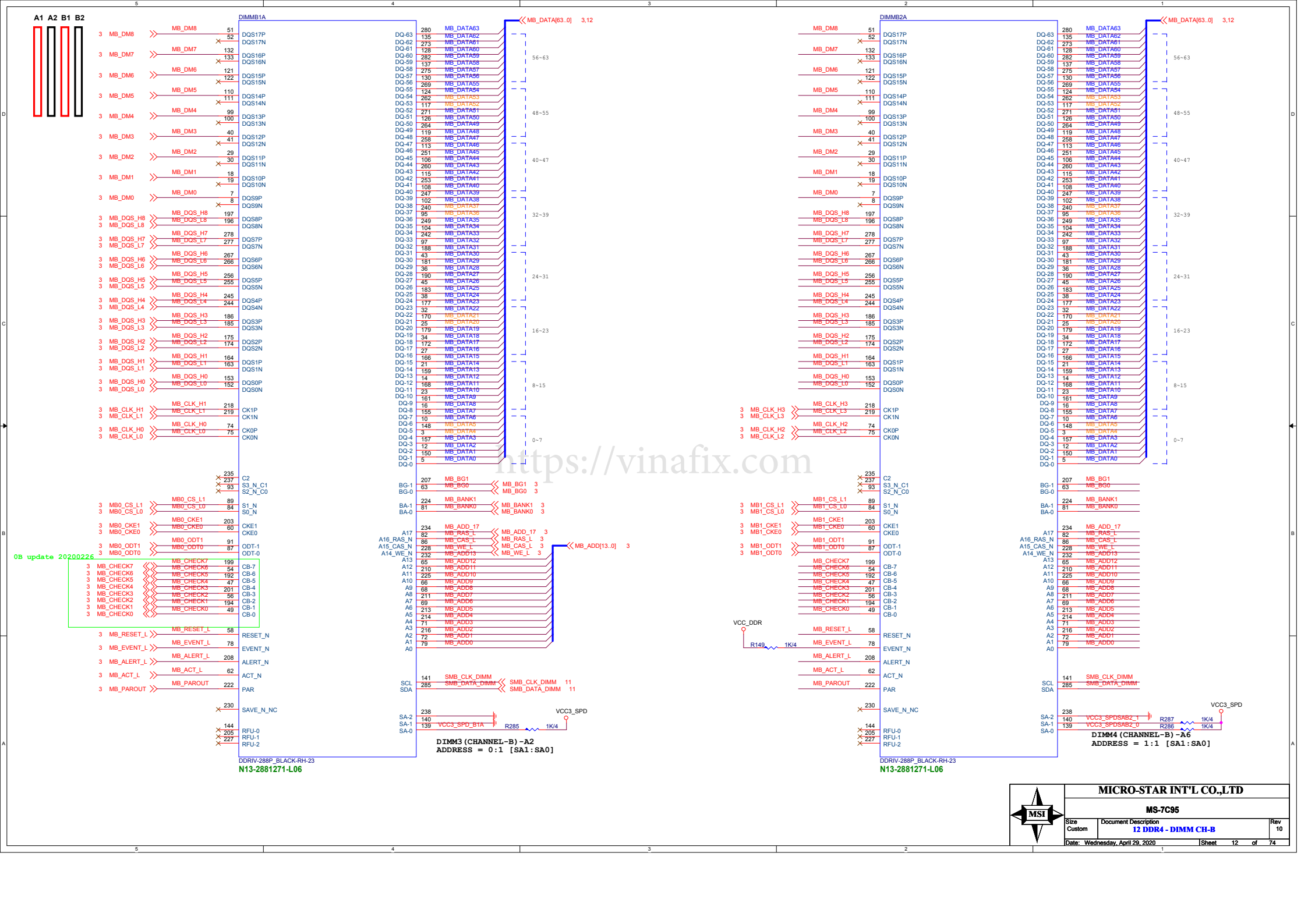
A1 A2 B1 B2
DIMMB1A
DIMMB2A
MB_DATA[63..0] 3,12
MB_ADD[13..0] 3
0B update 20200226
VCC_DDR
R149 1K/4
VCC3_SPD
R285 1K/4
R287 1K/4
R286 1K/4
DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]
DIMM4(CHANNEL-B)-A6
ADDRESS = 1:1 [SA1:SA0]
DDRIV-288P_BLACK-RH-23
N13-2881271-L06
https://vinafix.com
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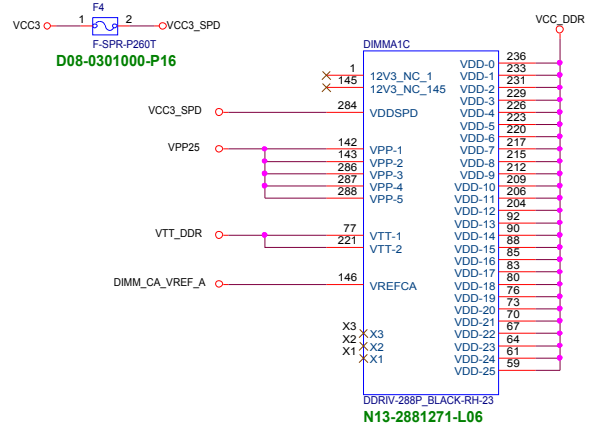
avl:D08-0301100-B07

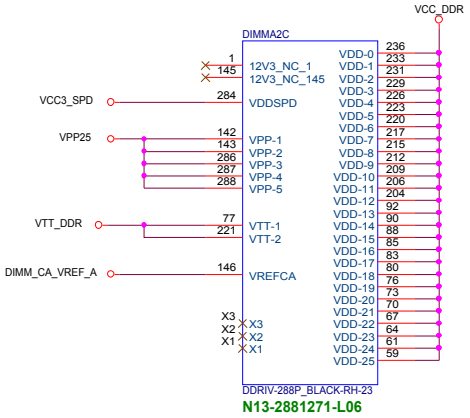
F4
VCC3 1 2 VCC3_SPD
F-SPR-P260T

D08-0301000-P16

DIMM SLOT PN BY SPEC



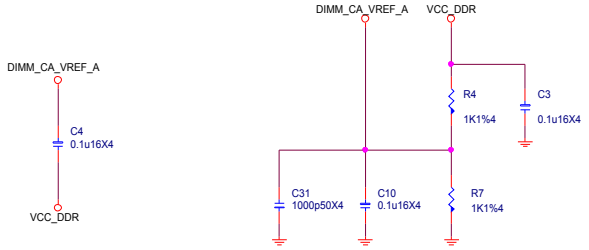
N13-2881271-L06

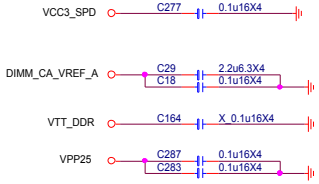


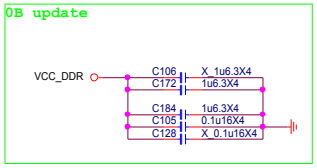
N13-2881271-L06

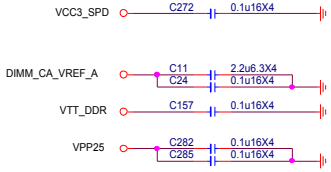
DDR VREF

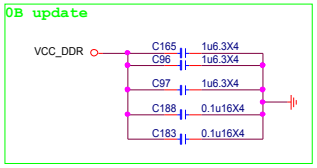
(place resistors close to DIMMs)

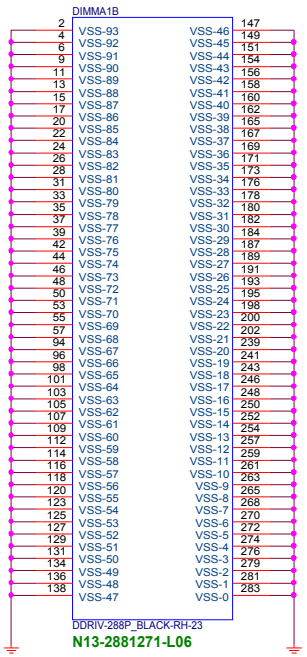




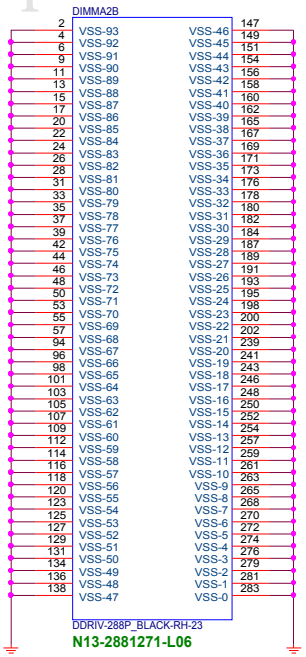








N13-2881271-L06



N13-2881271-L06

MICRO-STAR INT'L CO.,LTD

MS-7C95

Size	Document Description	Rev
Custom	13 DDR4 - POWER/GND-1	10

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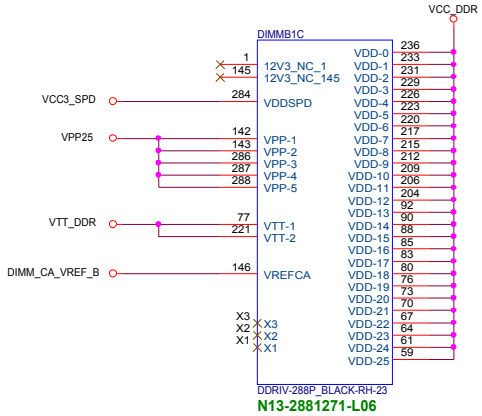
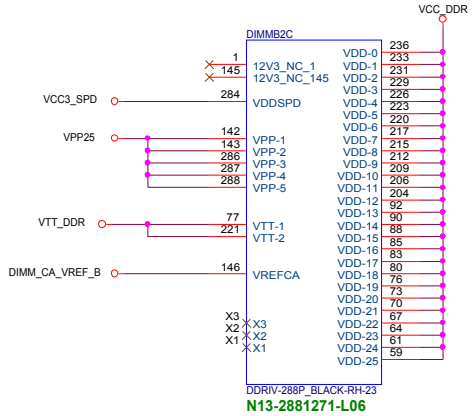
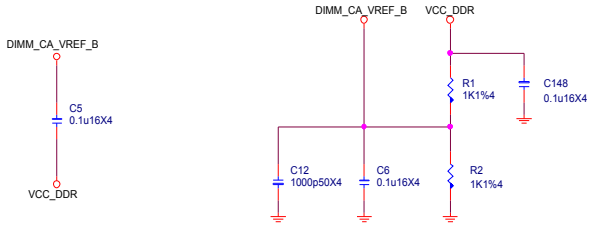
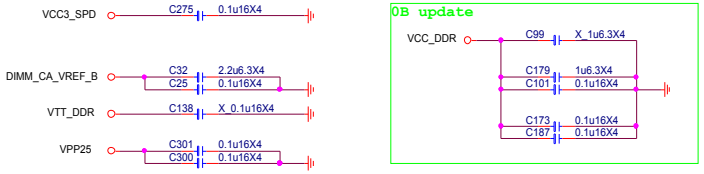


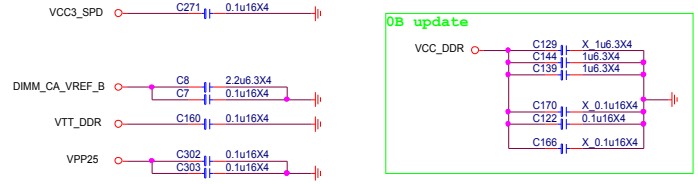


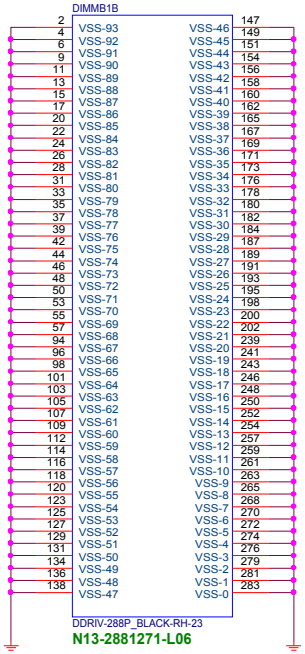
DDR VREF

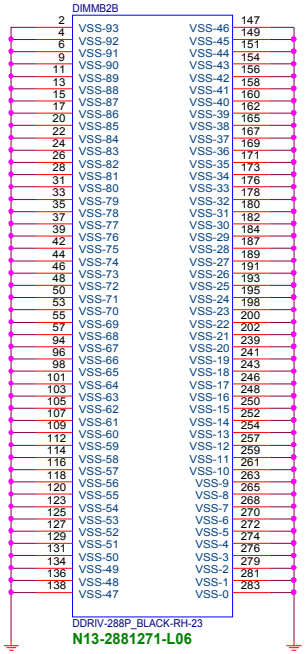
(place resistors close to DIMMs)











MICRO-STAR INT'L CO.,LTD

MS-7C95

Size	Document Description	Rev
Custom	14 DDR4 - POWER/GND-2	10

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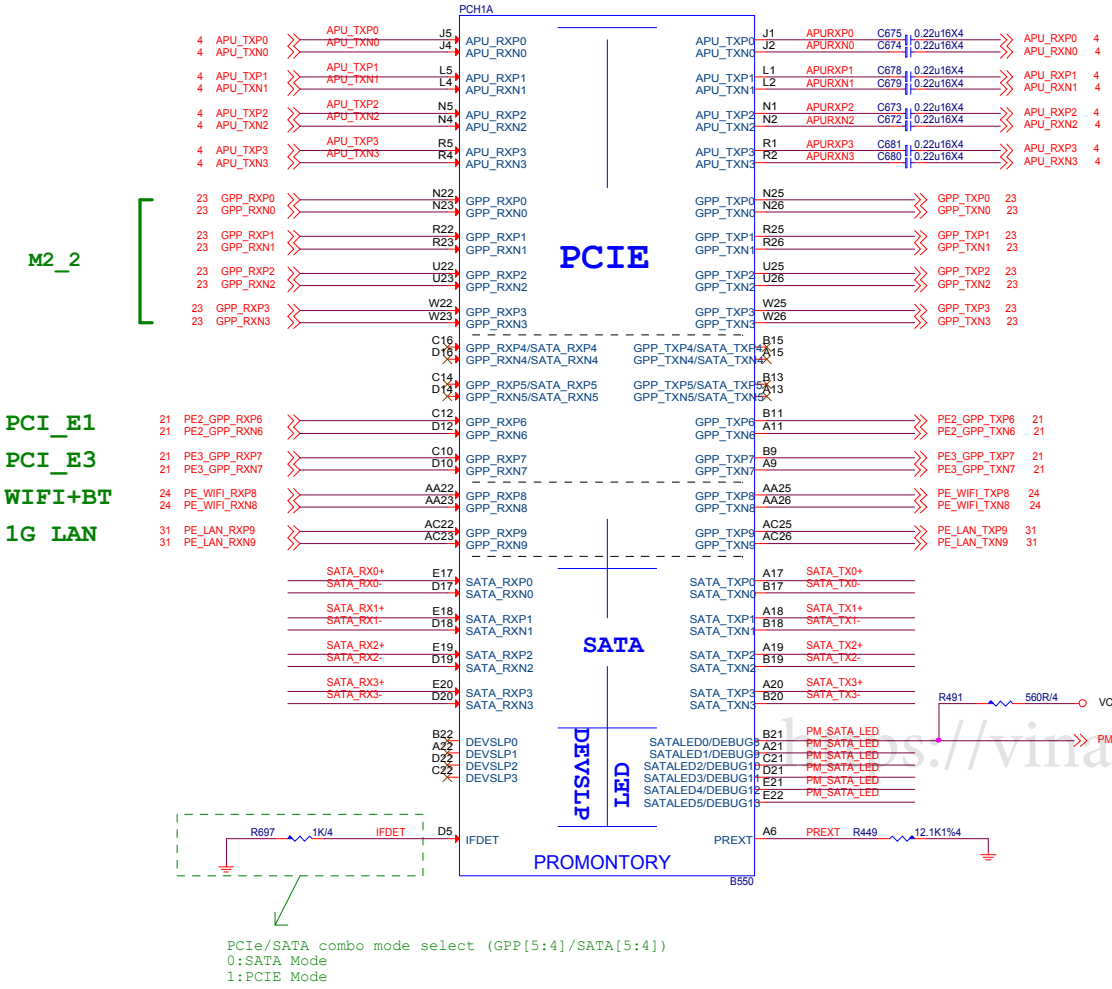
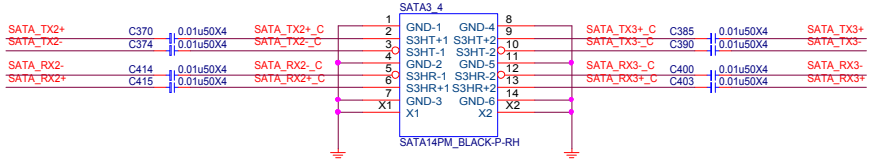


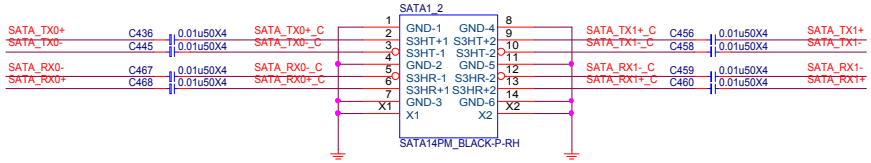
SATA Connector

SATA3_4



AVL:N5N-14M0201-L06

SATA1_2



AVL:N5N-14M0201-L06

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MS-7C95	
Size: Custom	Document Description: 15 PROM19 - PCIE/SATA
Rev: 10	
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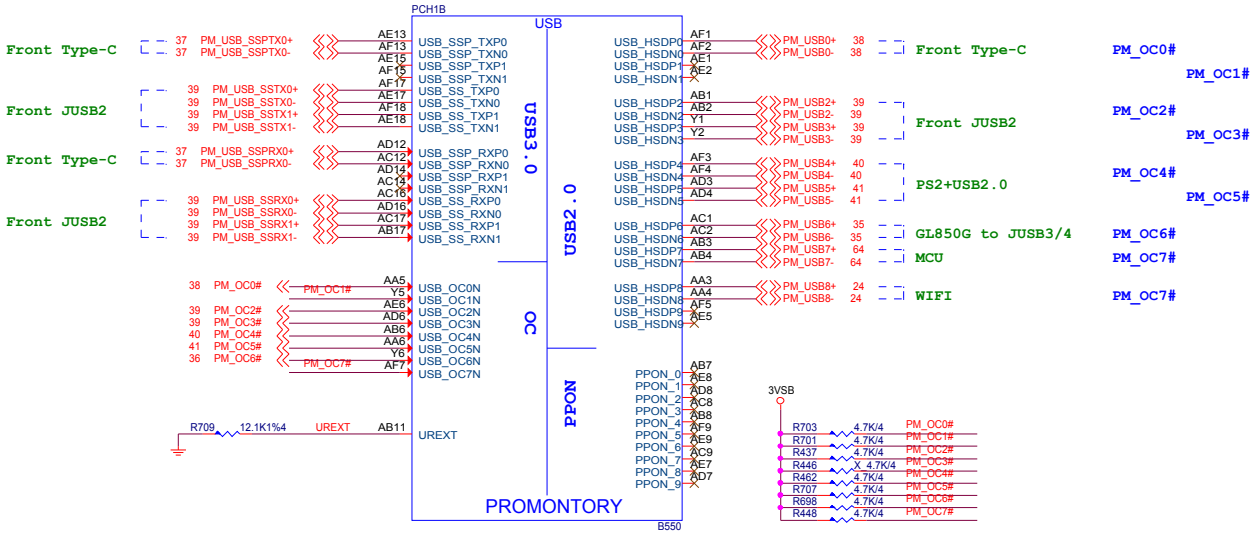
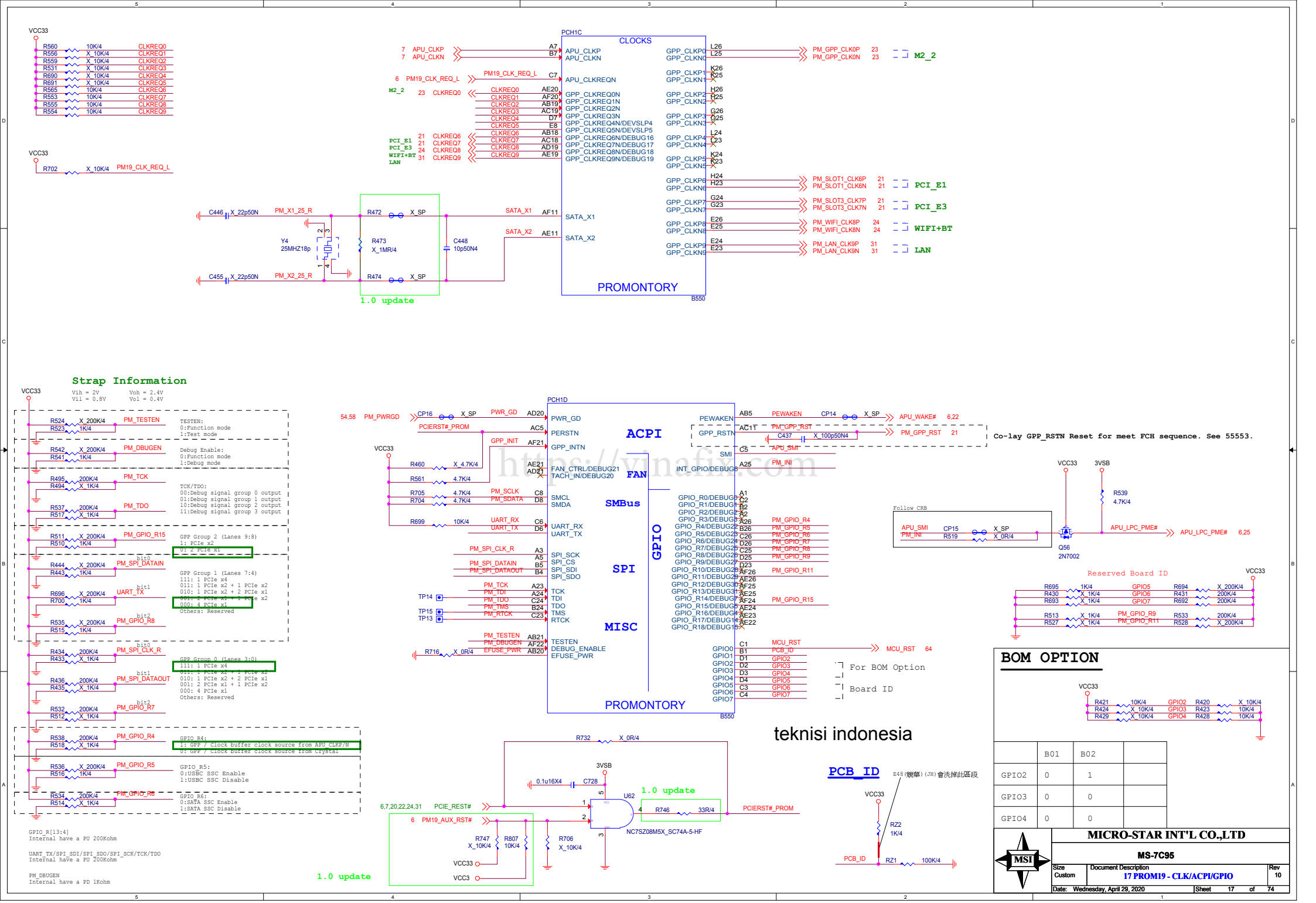


USB mapping

```
USB_SSP_TX/RX[0] + USB_HSDP/N[0] + USB_OC0N
USB_SSP_TX/RX[1] + USB_HSDP/N[1] + USB_OC1N

USB_SS_TX/RX[0] + USB_HSDP/N[2] + USB_OC2N
USB_SS_TX/RX[1] + USB_HSDP/N[3] + USB_OC3N
                  USB_HSDP/N[4] + USB_OC4N
                  USB_HSDP/N[5] + USB_OC5N
                  USB_HSDP/N[6] + USB_OC6N
                  USB_HSDP/N[7] + USB_OC7N
                  USB_HSDP/N[8] + USB_OC7N
                  USB_HSDP/N[9] + USB_OC7N
```


MICRO-STAR INT'L CO.,LTD		
MS-7C95		
Size: Custom	Document Description: 16 PROM19 - USB/OC	Rev: 10
Date: Wednesday, April 29, 2020	Sheet 16 of 74	



	B01	B02	
GPIO2	0	1	
GPIO3	0	0	
GPIO4	0	0	

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	17 PROM19 - CLK/ACPI/GPIO	10

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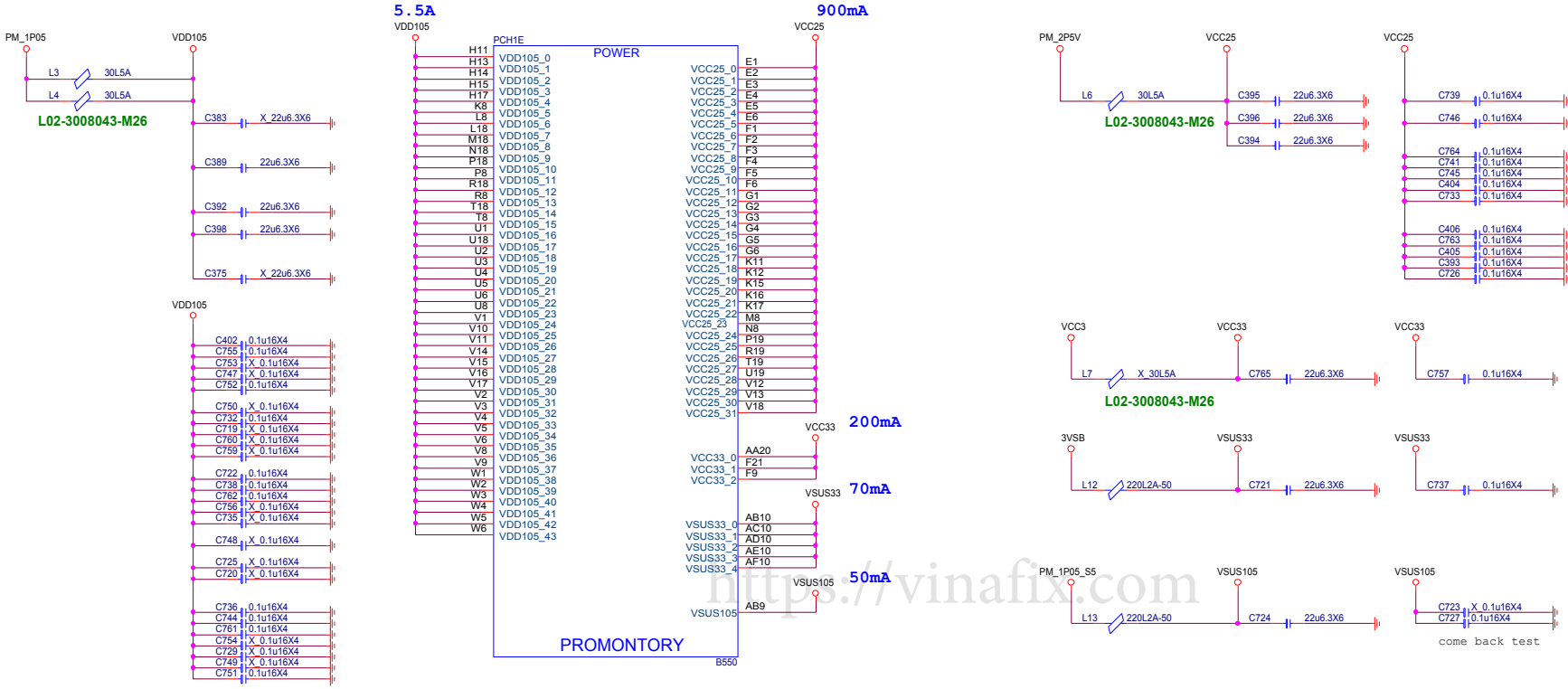

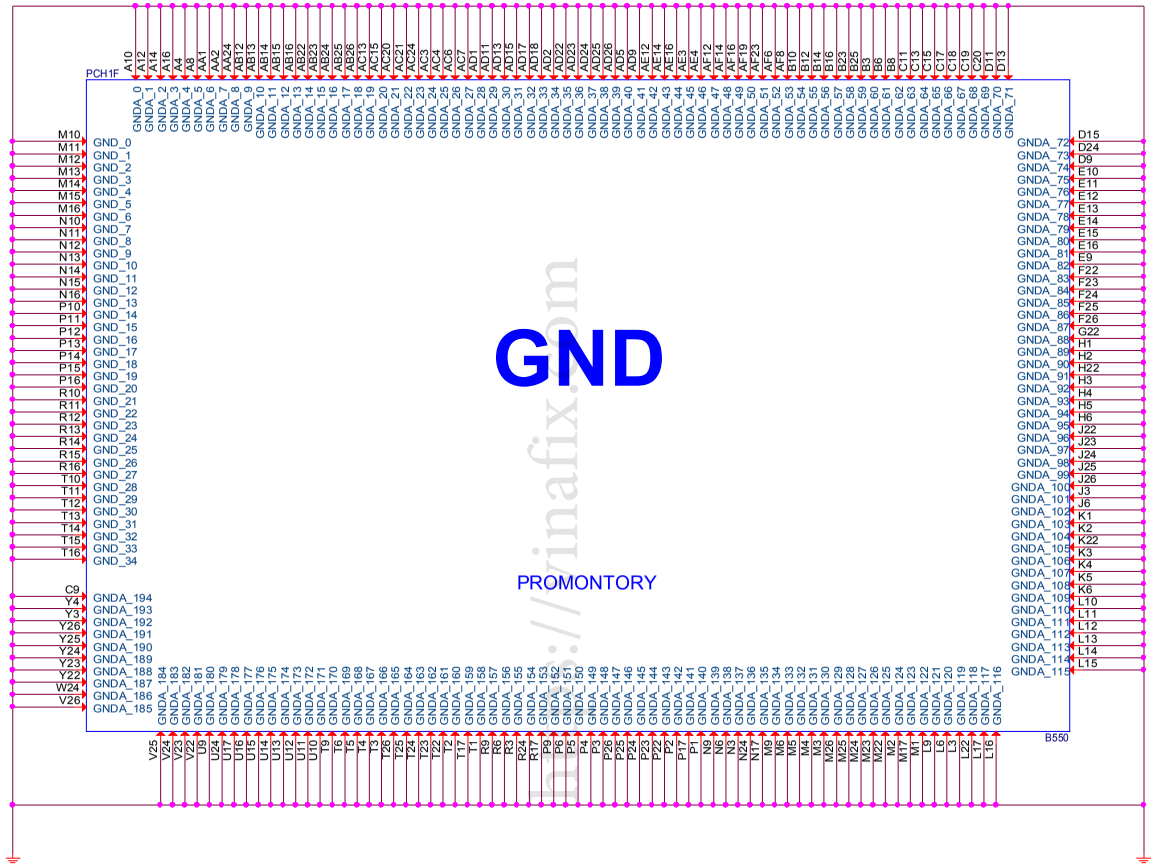

MICRO-STAR INT'L CO.,LTD		
MS-7C95		
Size: Custom	Document Description: 19 PROM19 - GND	Rev: 10
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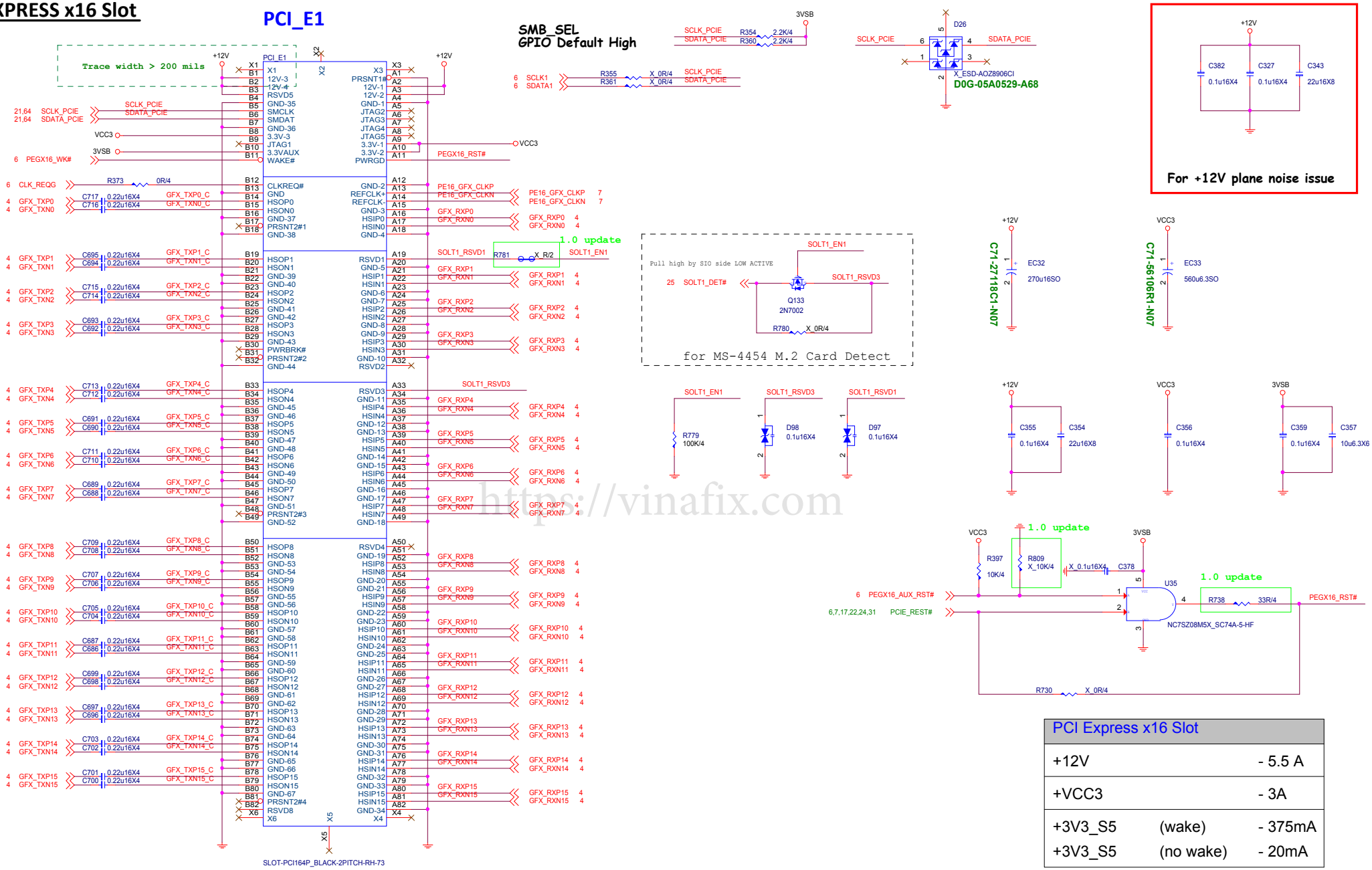
PCI EXPRESS x16 Slot



PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD	
MS-7C95	
Size: Custom	Document Description: 20 PCI_E1 (X16)
Rev: 10	
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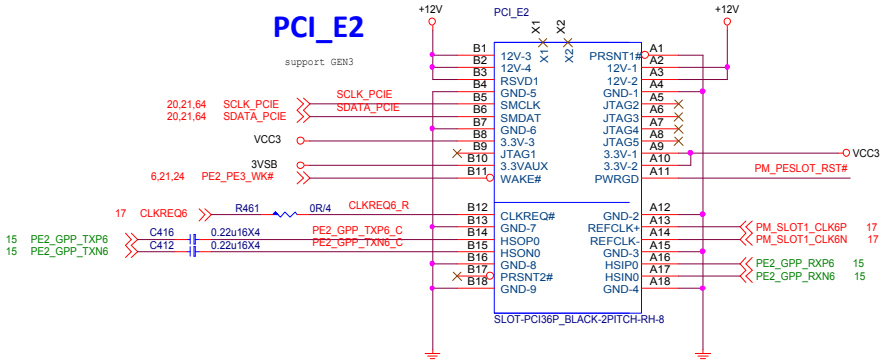
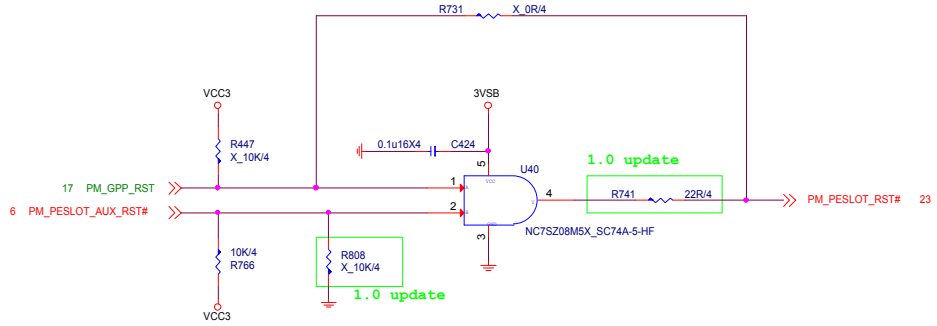
PCI EXPRESS X1 SLOT

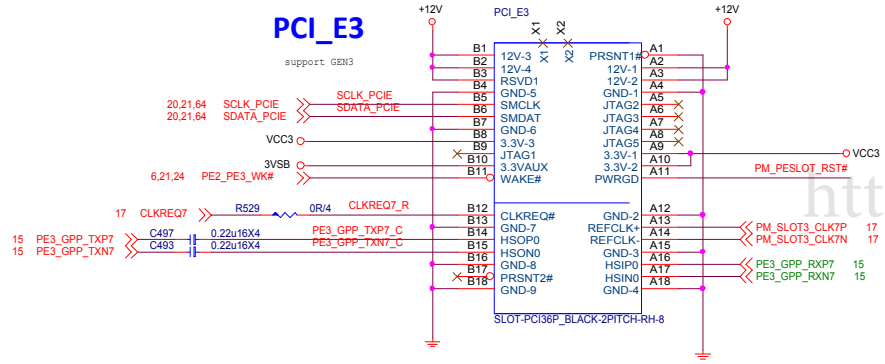


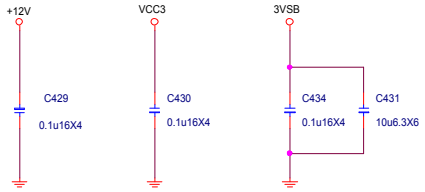
12V - 0.5A

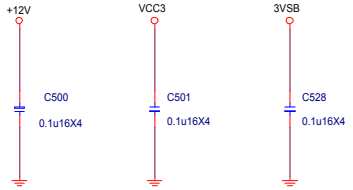
VCC3 - 3A

3VSBV - 375mA









PCI Express x1 Slot *3		
+12V		- 1.5 A
+VCC3		- 9A
+3V3_S5	(wake)	- 1125mA
+3V3_S5	(no wake)	- 20mA

MICRO-STAR INT'L CO.,LTD

MS-7C95

Size	Document Description	Rev
Custom	21 PCI_E2 (X1) / PCI_E3 (X1)	10

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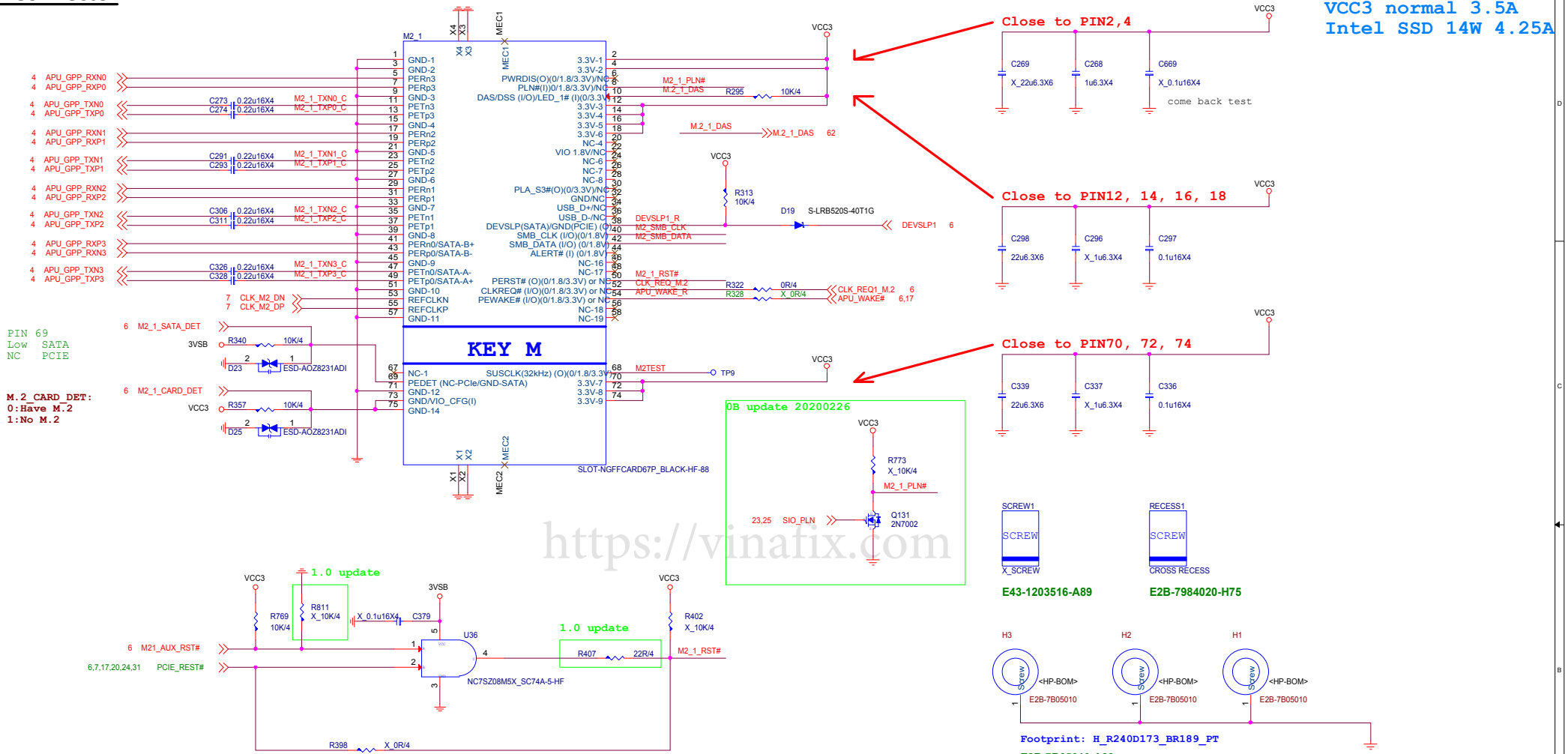
M.2_1 Connector

M2下方零件擺放限高要小於0.9mm的零件

VCC3 peak 7A
VCC3 normal 3.5A
Intel SSD 14W 4.25A



MICRO-STAR INT'L CO.,LTD	
MS-7C95	
Size: Custom	Document Description: 22 M2_1 PCIE / SATA
Rev: 10	
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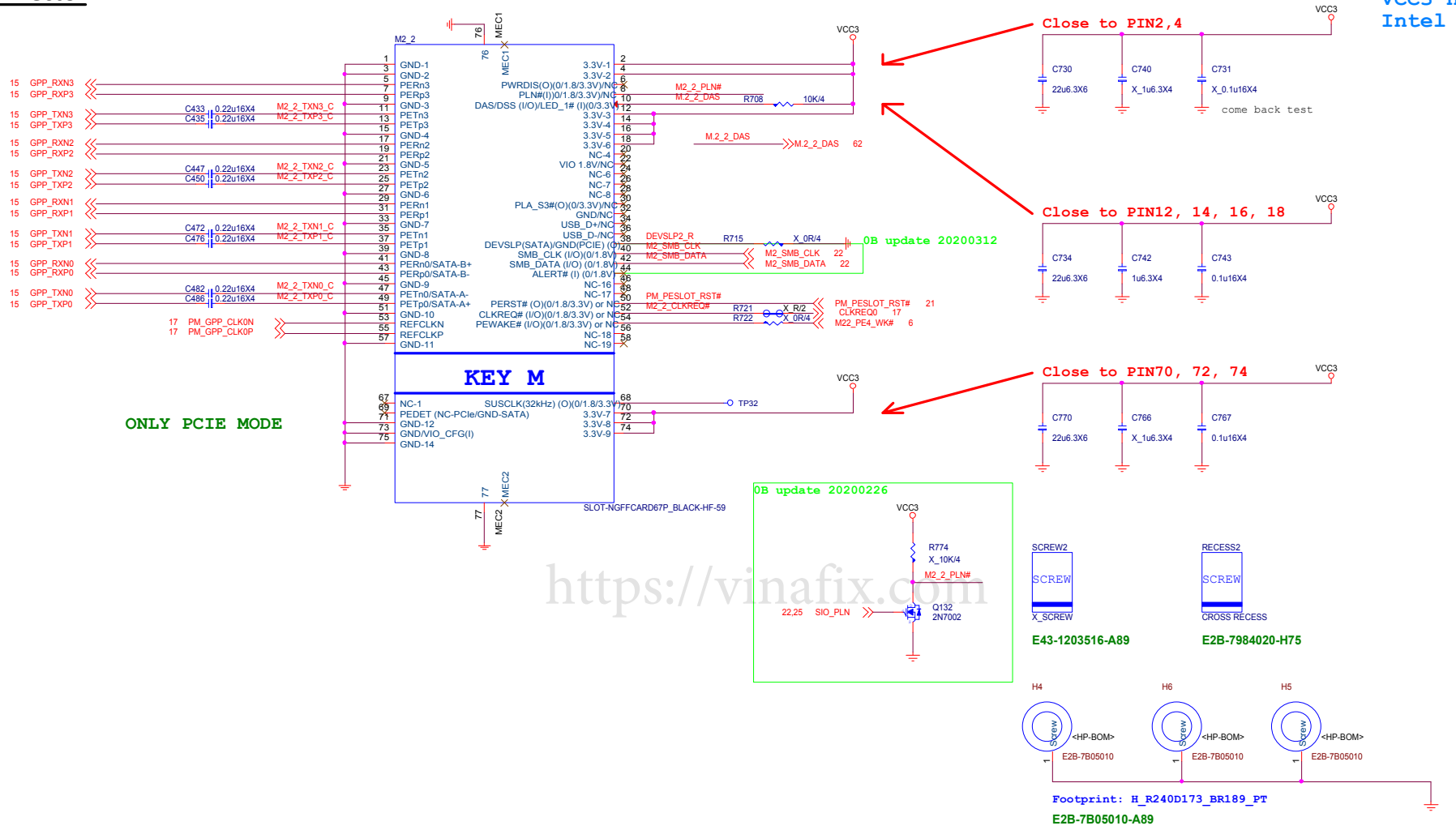
M.2_2 Connector

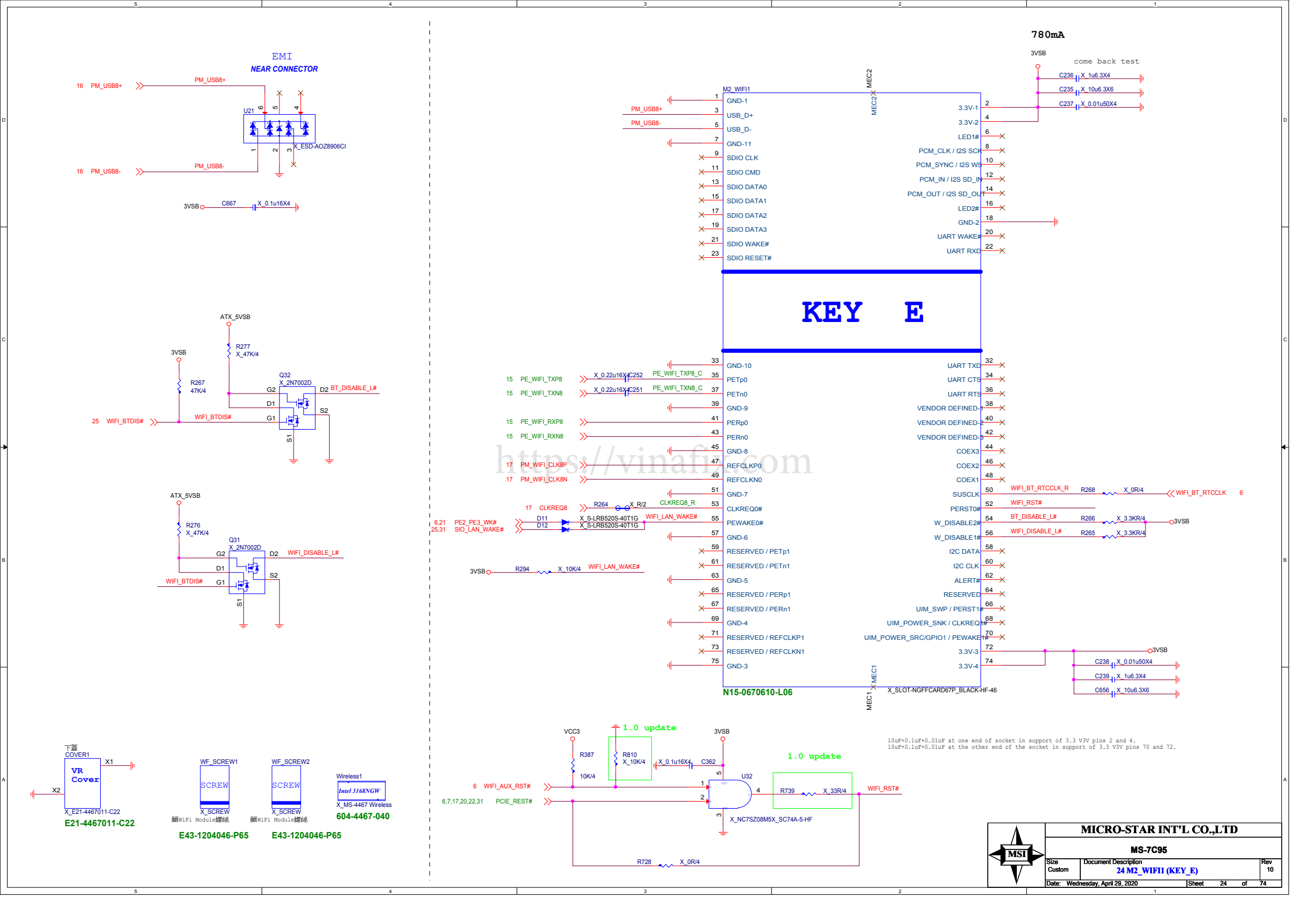
M2下方零件擺放限高要小於0.9mm的零件

VCC3 peak 7A
VCC3 normal 3.5A
Intel SSD 14W 4.25A



Vinafix.com

MICRO-STAR INT'L CO.,LTD		
MS-7C95		
Size: Custom	Document Description: 23 M2_2 PCIE	Rev: 10
Date: Wednesday, April 29, 2020	Sheet 23 of 74	


EMI
NEAR CONNECTOR
16 PM_USB8+
PM_USB8+
U21
X_ESD-AOZ8906CI
16 PM_USB8-
PM_USB8-
3VSB
C667
X_0.1u16X4
ATX_5VSB
R277
X_47K/4
3VSB
R267
47K/4
Q32
X_2N7002D
G2
D1
G1
S2
S1
D2
BT_DISABLE_L#
25 WIFI_BTDIS#
WIFI_BTDIS#
ATX_5VSB
R276
X_47K/4
Q31
X_2N7002D
G2
D1
G1
S2
S1
D2
WIFI_DISABLE_L#
WIFI_BTDIS#
下蓋
COVER1
VR Cover
X1
X2
X_E21-4467011-C22
E21-4467011-C22
WF_SCREW1
SCREW
X_SCREW
鎖WiFi Module螺絲
WF_SCREW2
SCREW
X_SCREW
鎖WiFi Module螺絲
E43-1204046-P65
E43-1204046-P65
Wireless1
Intel 3168NGW
X_MS-4467 Wireless
604-4467-040
780mA
3VSB
come back test
C236
X_1u6.3X4
C235
X_10u6.3X6
C237
X_0.01u50X4
M2_WIFI1
MEC2
GND-1
USB_D+
USB_D-
GND-11
SDIO CLK
SDIO CMD
SDIO DATA0
SDIO DATA1
SDIO DATA2
SDIO DATA3
SDIO WAKE#
SDIO RESET#
PM_USB8+
PM_USB8-
3.3V-1
3.3V-2
LED1#
PCM_CLK / I2S SCK
PCM_SYNC / I2S WS
PCM_IN / I2S SD_IN
PCM_OUT / I2S SD_OUT
LED2#
GND-2
UART WAKE#
UART RXD
KEY E
GND-10
PETp0
PETn0
GND-9
PERp0
PERn0
GND-8
REFCLKP0
REFCLKN0
GND-7
CLKREQ0#
PEWAKE0#
GND-6
RESERVED / PETp1
RESERVED / PETn1
GND-5
RESERVED / PERp1
RESERVED / PERn1
GND-4
RESERVED / REFCLKP1
RESERVED / REFCLKN1
GND-3
15 PE_WIFI_TXP8
15 PE_WIFI_TXN8
X_0.22u16X
C252
C251
PE_WIFI_TXP8_C
PE_WIFI_TXN8_C
15 PE_WIFI_RXP8
15 PE_WIFI_RXN8
17 PM_WIFI_CLK8P
17 PM_WIFI_CLK8N
17 CLKREQ8
R264
X_R/2
CLKREQ8_R
6,21 PE2_PE3_WK#
25,31 SIO_LAN_WAKE#
D11
D12
X_S-LRB520S-40T1G
X_S-LRB520S-40T1G
WIFI_LAN_WAKE#
3VSB
R294
X_10K/4
WIFI_LAN_WAKE#
UART TXD
UART CTS
UART RTS
VENDOR DEFINED-1
VENDOR DEFINED-2
VENDOR DEFINED-3
COEX3
COEX2
COEX1
SUSCLK
PERST0#
W_DISABLE2#
W_DISABLE1#
I2C DATA
I2C CLK
ALERT#
RESERVED
UIM_SWP / PERST1#
UIM_POWER_SNK / CLKREQ1#
UIM_POWER_SRC/GPIO1 / PEWAKE1#
3.3V-3
3.3V-4
WIFI_BT_RTCCLK_R
R268
X_0R/4
WIFI_BT_RTCCLK
6
WIFI_RST#
BT_DISABLE_L#
R266
X_3.3KR/4
3VSB
WIFI_DISABLE_L#
R265
X_3.3KR/4
C238
X_0.01u50X4
C239
X_1u6.3X4
C656
X_10u6.3X6
MEC1
X_SLOT-NGFFCARD67P_BLACK-HF-46
N15-0670610-L06
https://vinafix.com
VCC3
1.0 update
R387
10K/4
R810
X_10K/4
X_0.1u16X4
C362
3VSB
1.0 update
6 WIFI_AUX_RST#
6,7,17,20,22,31 PCIE_REST#
U32
R739
X_33R/4
WIFI_RST#
X_NC7SZ08M5X_SC74A-5-HF
R728
X_0R/4
10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.
10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 70 and 72.
MICRO-STAR INT'L CO.,LTD
MS-7C95
Size
Custom
Document Description
24 M2_WIFI1 (KEY_E)
Rev
10
Date: Wednesday, April 29, 2020
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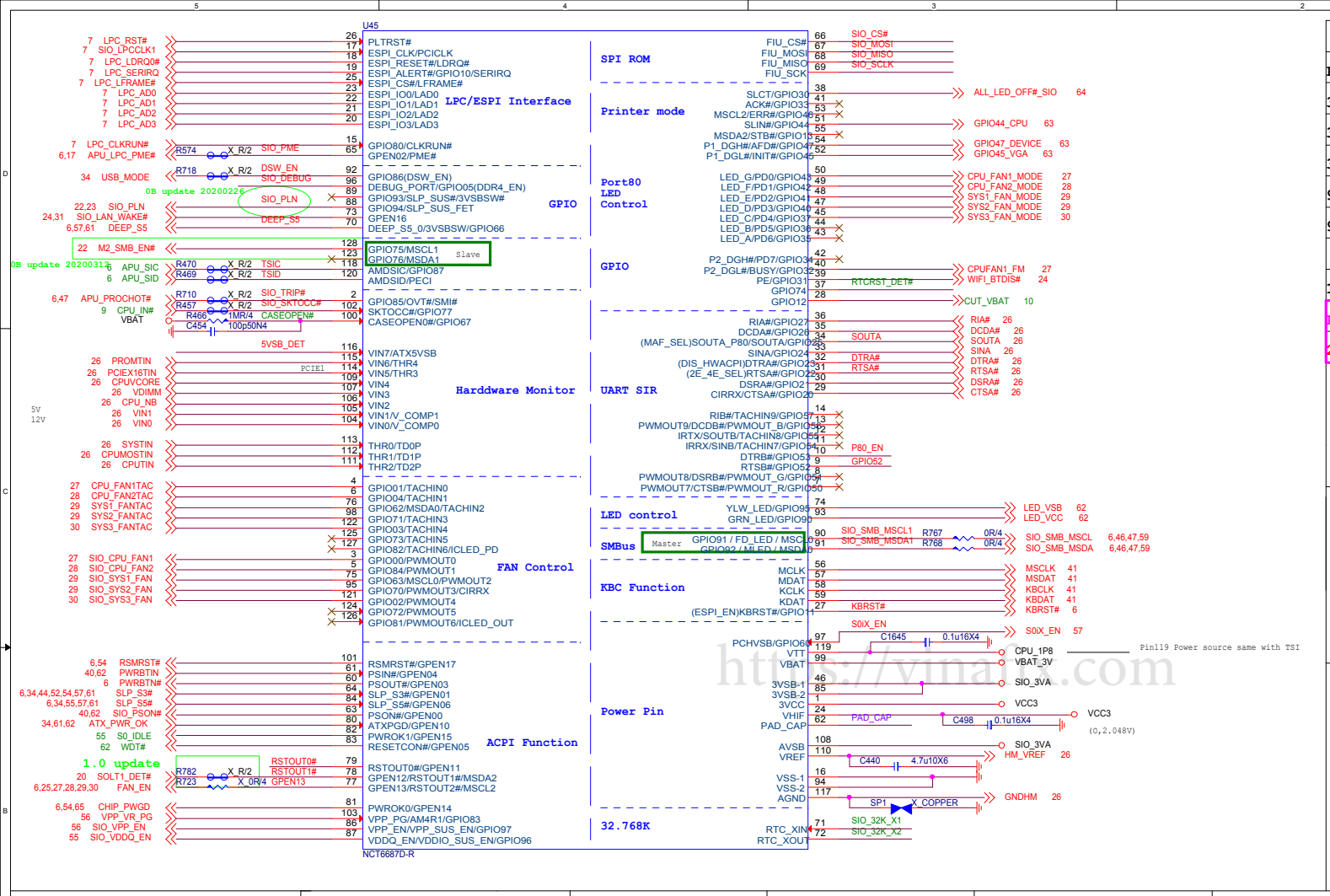
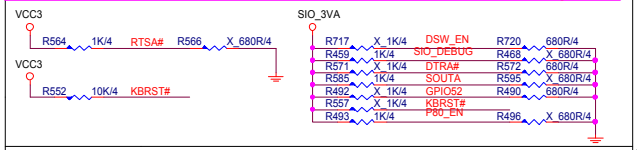
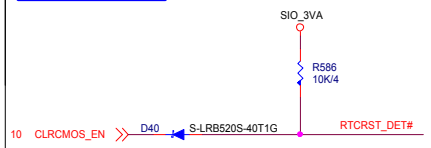


POWER ON STRAPPING PIN FOR NCT6687D-R

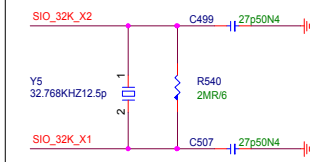
PIN	NAME	Circuit NAME	0	1	Strap Point
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	3VCC
32	DIS_HWACPI	DTRA#	HW ACPI enable	HW ACPI disable	3VA
34	MAF_SEL	SOUTA	MAF enable	MAF disable	3VA
92	DSW_EN	DSW_EN	DSW disable	DSW enable	3VA
96	DDR4_EN	SIO_DEBUG	DDR4 control disable	DDR4 control enable	3VA
9	FAN789_EN (FW setting)	GPIO52	FAN789 disable	FAN789 enable	3VA
10	P80_EN	GPIO46	Port80 LED	GPIO	3VA
PIN	NAME	Circuit NAME	VCC3	3VA	Strap Point
27	ESPI_EN	KBRST#	LPC	ESPI	VCC3 or 3VA



RTCRST_DET



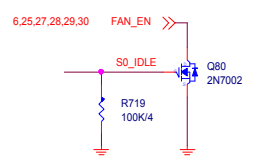
RTC_32K

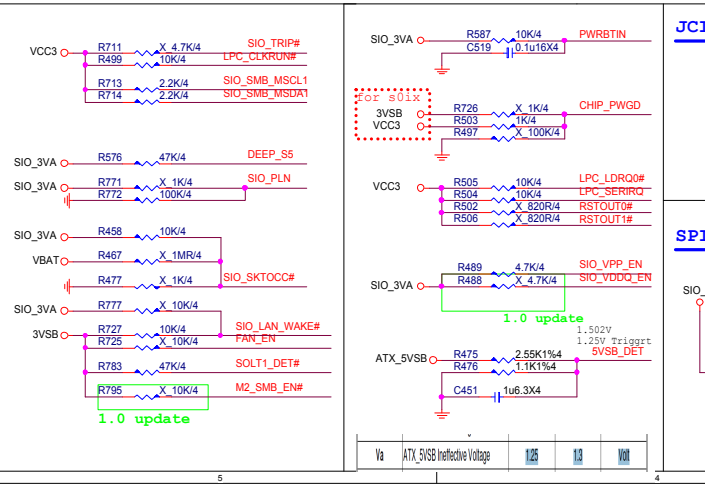


S0_IDLE

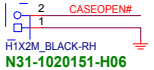
1.0 update

Closed FAN , by S0i3.



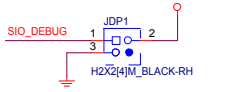


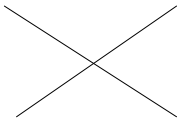
JCI1



N31-1020151-H06

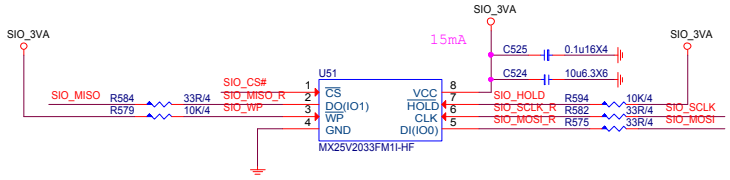
DEBUG PORT



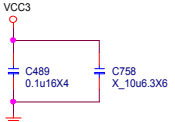


Use JBD1 for BIOS DEBUG.
If no comp port or JTPM.

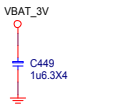
SPI ROM



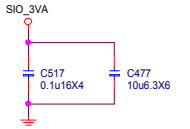
Closed PIN1,24



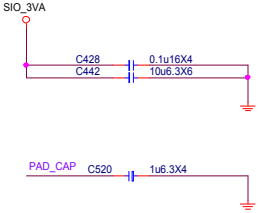
Closed PIN99



Closed PIN46,85



3V Analog Power



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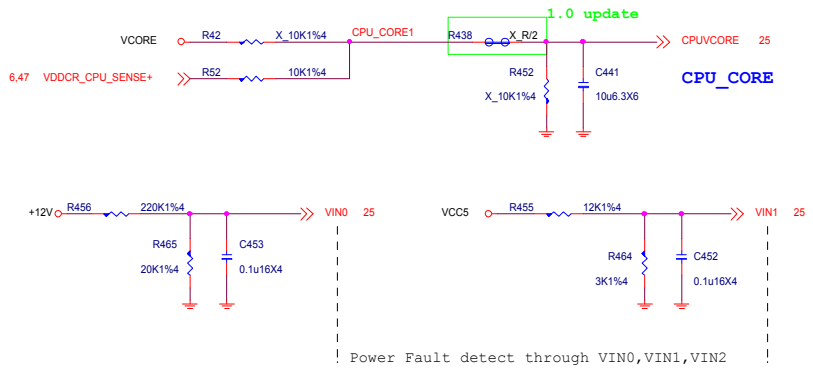
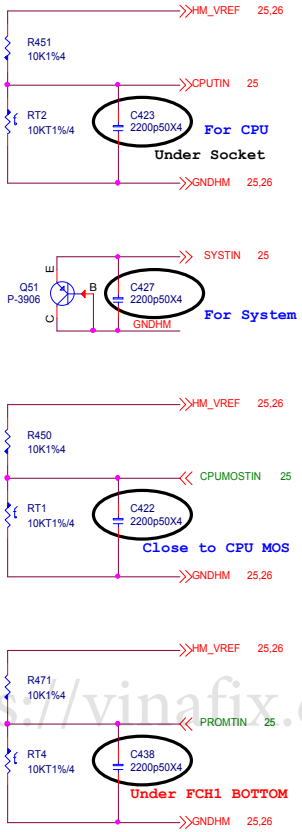
HW Monitor - Voltage

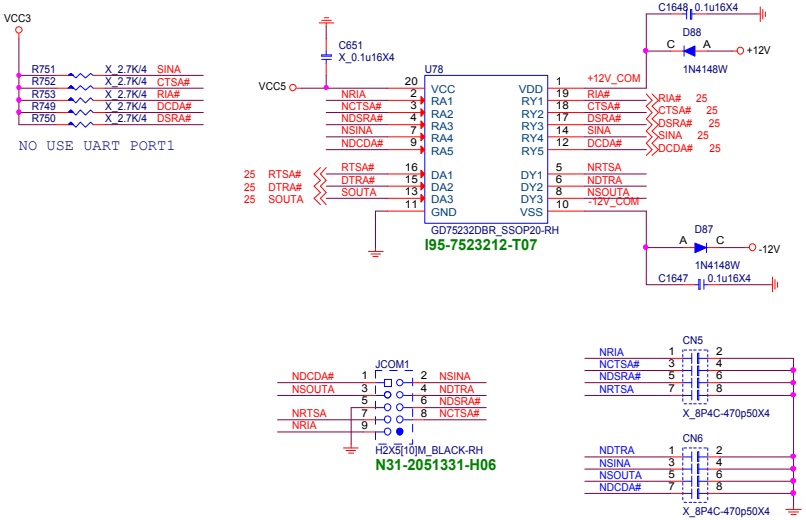
SIO HM Voltage over 2.048V will not detect



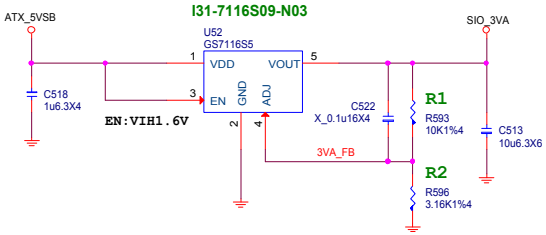
TEMP SENSOR



COM PORT



SIO_3VA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

MSI	MICRO-STAR INT'L CO.,LTD	
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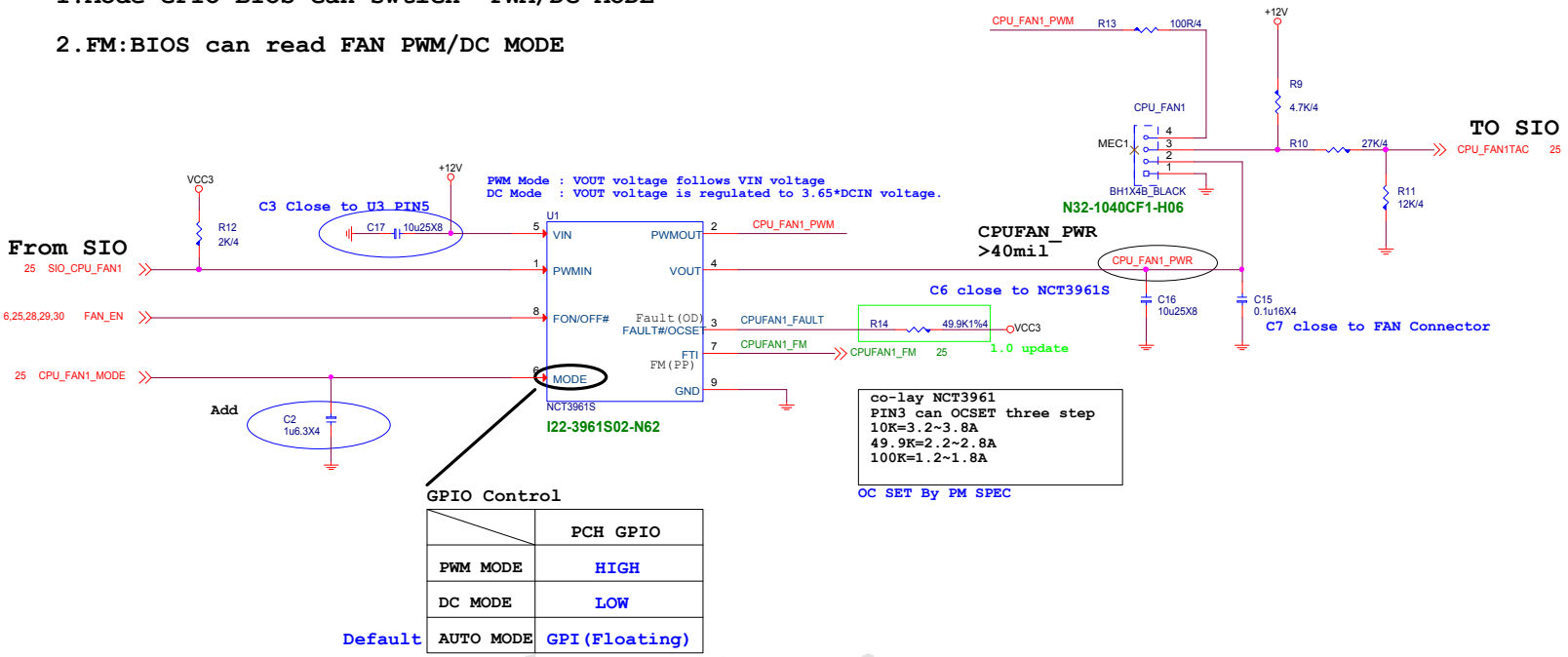
CPUFAN1 TYPE N : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

2.FM:BIOS can read FAN PWM/DC MODE



co-lay NCT3961
PIN3 can OCSET three step
10K=3.2~3.8A
49.9K=2.2~2.8A
100K=1.2~1.8A

OC SET By PM SPEC

GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

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Size: Custom | Document Description: 27 FAN TYPE-N CPUFAN1 | Rev: 10

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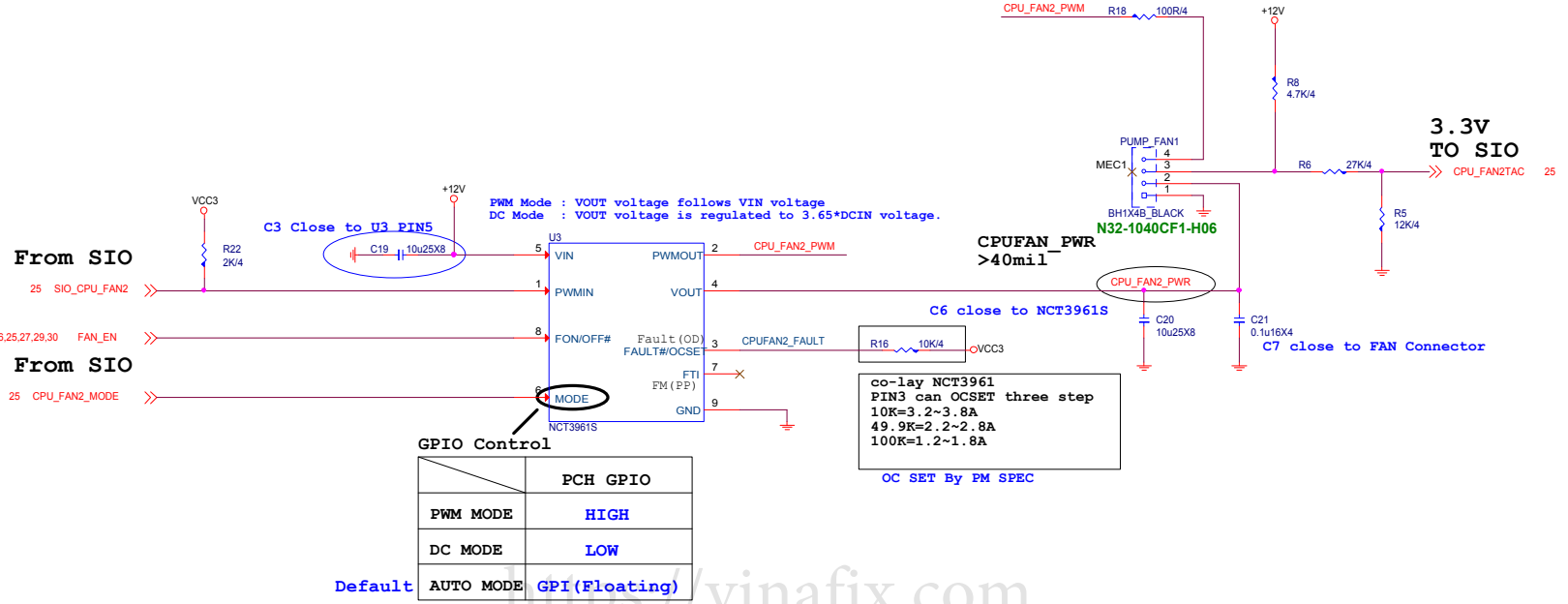
PUMPFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

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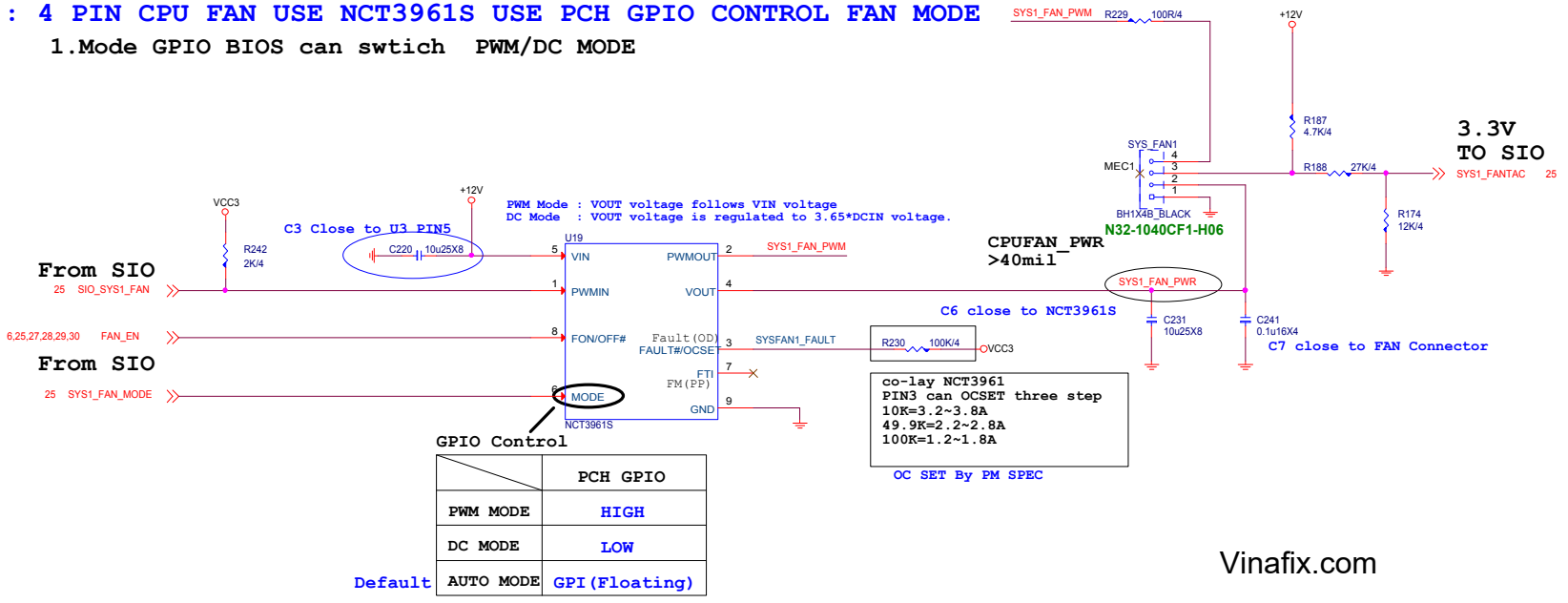
SYSFAN1

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



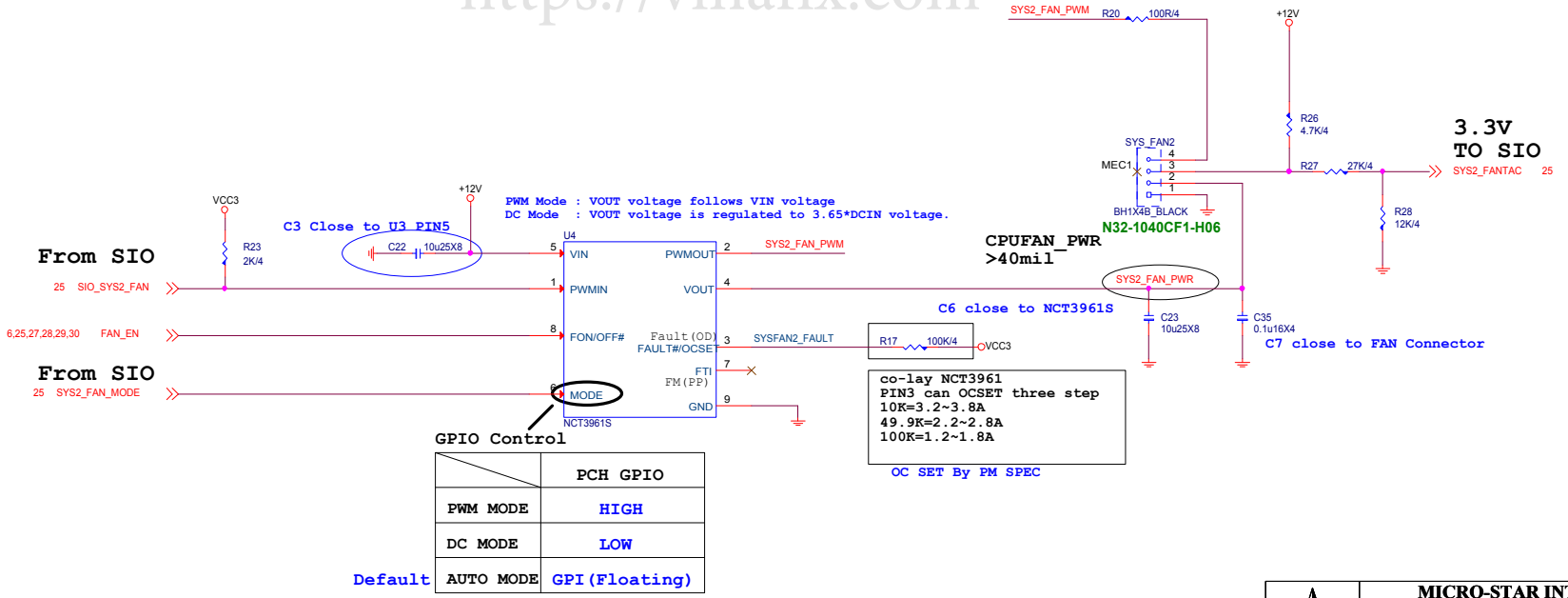
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Vinafix.com

SYSFAN2

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

MS-7C95

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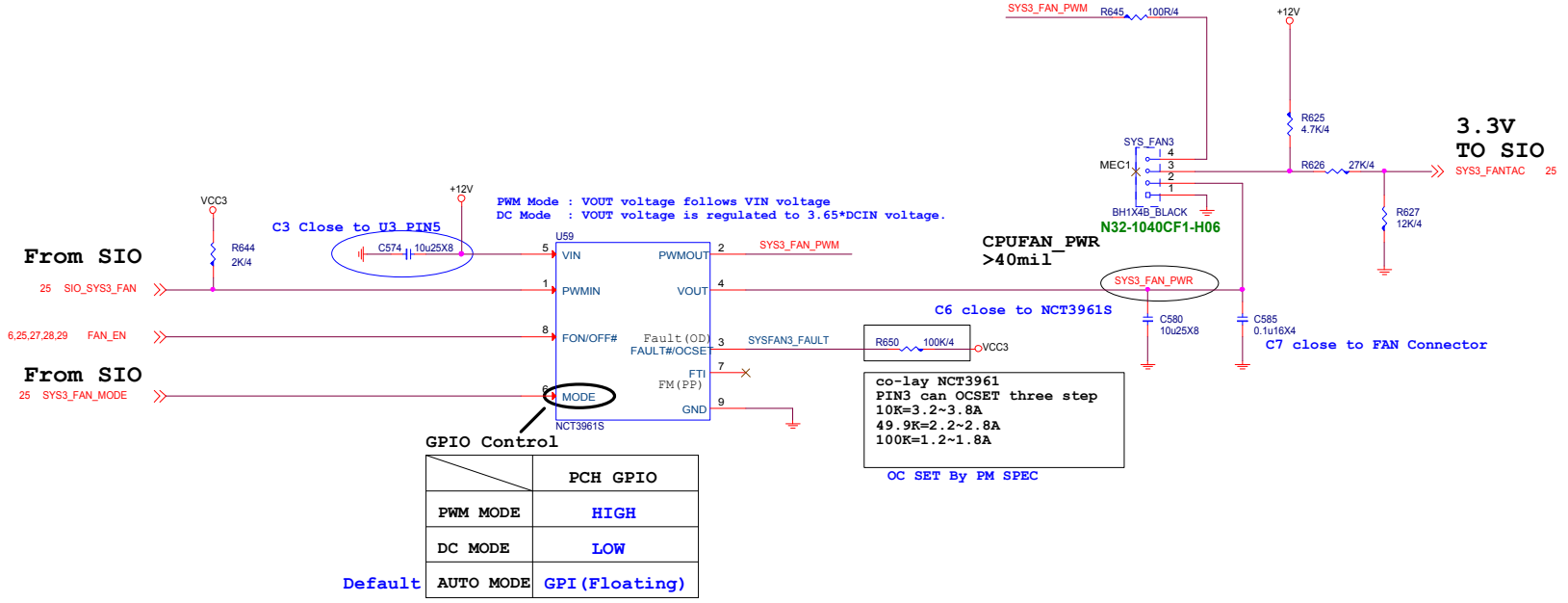
SYSFAN3

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

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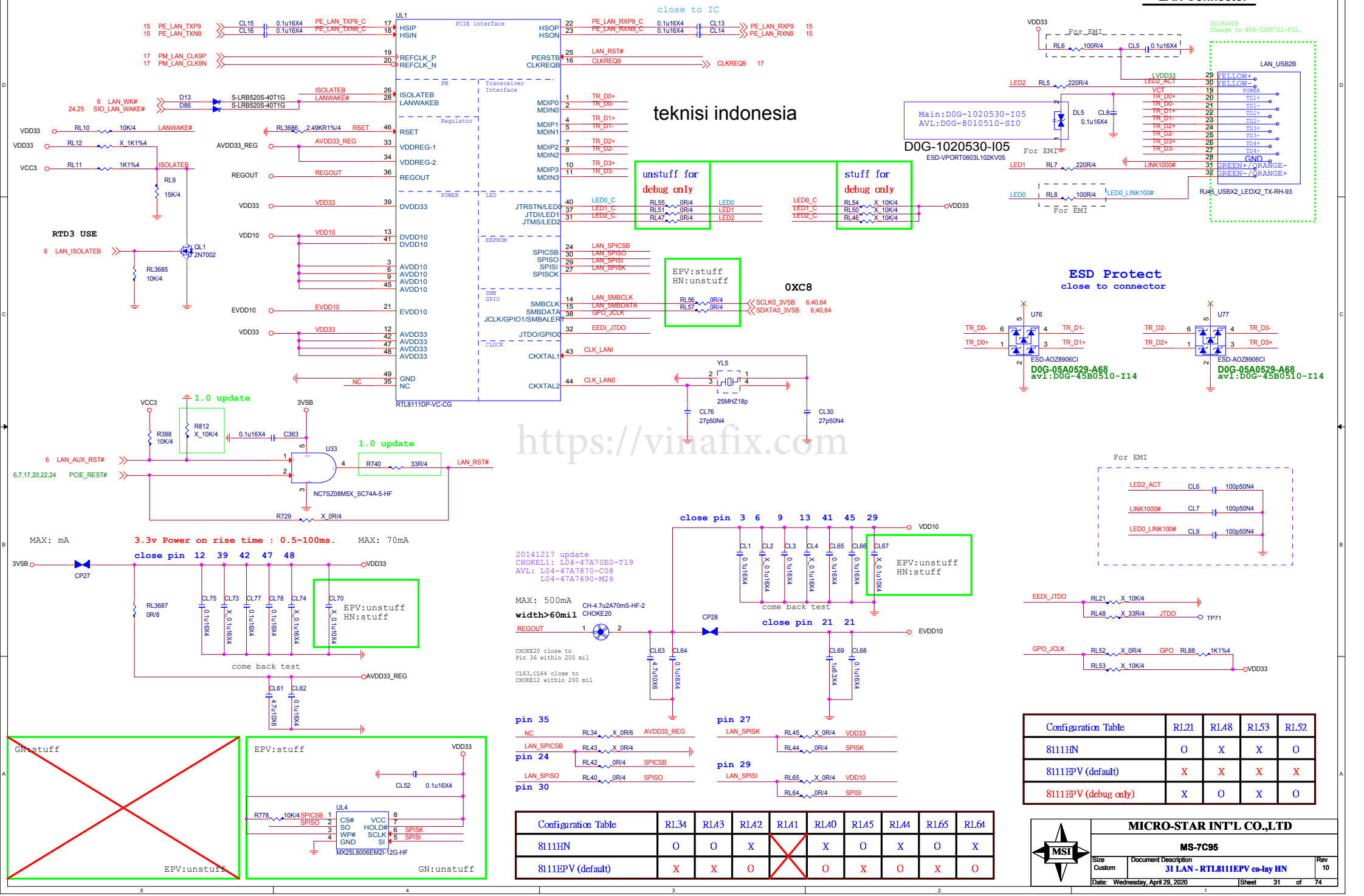
RTL8111EPV(default) coly RTL8111HN Giga LAN



Configuration Table	RL21	RL48	RL53	RL52
8111HN	O	X	X	O
8111EPV (default)	X	X	X	X
8111EPV (debug only)	X	O	X	O

Configuration Table	RL34	RL43	RL42	RL41	RL40	RL45	RL44	RL65	RL64
8111HN	O	O	X	X	X	O	X	O	X
8111EPV (default)	X	X	O	X	O	X	O	X	O

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ALC892

Follow APU power well

CPU_1P8_S5

11mA

Closed Codec

VCC3

LDOOUT

SMD CAP: Fail to test THD+N
EL/SOLID cap: Test THD+N will Pass

Closed pin9

CA15 X_10u6.3X6 CA18 0.1u16X4

CA24 10u6.3X6 CA23 0.1u16X4

CA25 0.1u16X4 CA26 10u6.3X6

closed PIN38

CA14 22u6.3X6 closed PIN25

C91-1011051-N07

UA5

EAPD/SPDIFI, SPDIF-OUT, SDATA-OUT, SDATA-IN, SYNC, RESET#, BCLK, GPIO0/DMIC-CLK/SPDIF-OUT2, REGREF, SENSE A, SENSE B, MIC1-VREFO-R, MIC2-VREFO, MIC1-VREFO-L, PIN37-VREFO, LDO-IN, LINE2-VREFO, VREF, SENSE C, JDREF, BEEP, DVDD, DVDD-IO, LDO-OUT1, LDO-OUT2, GPIO1/DMIC-DATA, DVSS, AVSS, AVSS

FRONT-R/L, SURR-R/L, CENTER/LFE, SIDE-R/L, LINE1-R/L, LINE2-R/L, MIC1-R/L, MIC2-R/L, CD-R, CD-GND, CD-L

ALC892-CG-RH

B05-LC89214-R09

892,887/4.7uF: Test THD+N will Pass
898/10uF: Test THD+N will Pass

45.8mA

LDOVDD

CA17 X_0.1u16X4 CA16 10u6.3X6 RA63 20K1%4

Closed Codec Pin 27

EMI

CA7 X_0.1u16X4 CA32 X_1000p50X4

CPA5 X_COPPER CPA6 X_COPPER

Closed Codec

SENSE_A RA26 5.1K1%4 FRONT_JD

RA64 10K1%4 LINE1_JD

RA27 20K1%4 MIC1_JD

Digital *Analog*

5VDUAL LA5 0R/8 45.8mA LDOVDD

ATX_5VSB LA1 X_0R/8

DA5 X_TVS

CA58 10u6.3X6 CA57 0.1u16X4

CA58,CA57 close to LA1,LA5

AUDIO1A

LINE_IN_L RA5 75R/4 LINE_IN_LA

LINE_IN_R RA6 75R/4 LINE1_JD LINE_IN_RA

CA29 100p50N4 CA30 100p50N4

JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH

LIN_IN

AUDIO1B

LOUT_L RA13 75R/4 LOUT_LA

LOUT_R RA17 75R/4 FRONT_JD LOUT_RA

DA12 ESD-MLVS0402L04-HF DA13 ESD-MLVS0402L04-HF

D0G-2710510-I05

JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH

LIN_OUT

AUDIO1C

MIC1-VREFO-L RA30 2.2K/4 MIC1_LA

MIC1-VREFO-R RA68 2.2K/4 MIC1_RA

MIC1_L RA29 75R/4 MIC1_LA

MIC1_R RA67 75R/4 MIC1_JD MIC1_RA

CA33 100p50N4 CA34 100p50N4

JACK-AUDIOX3F_PK/LIME/LIGHT/BU-RH

MIC1

LOUT_LA LOUT_RA RA14 22K/4 RA18 22K/4

D LIN_IN

E LIN_OUT

F MIC1

N54-13P0271-K06

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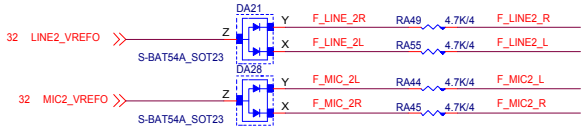
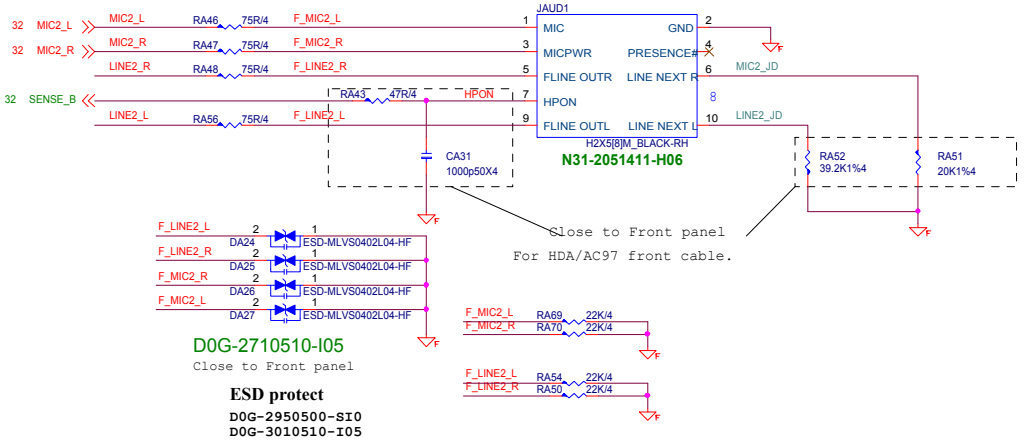
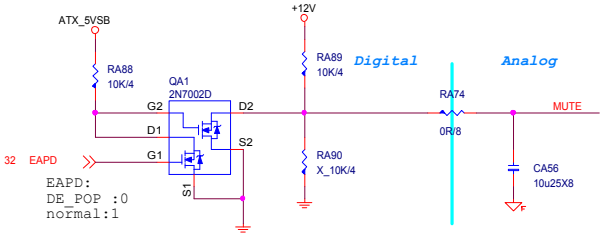
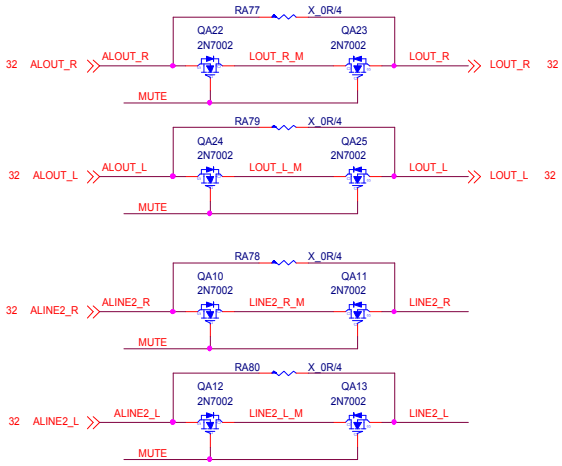




Rear Line OUT De-POP circuit

(De-pop circuit for Rear Line out & Front Headphone out)





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MS-7C95	
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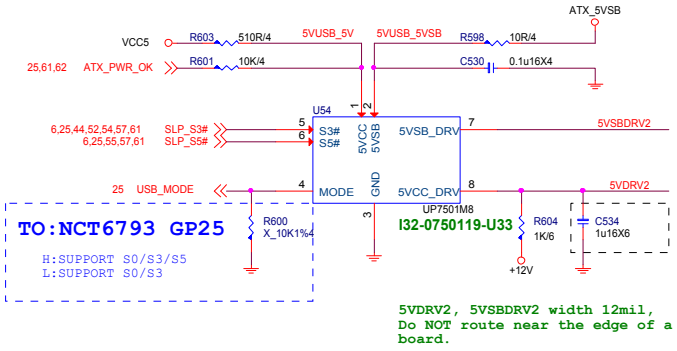
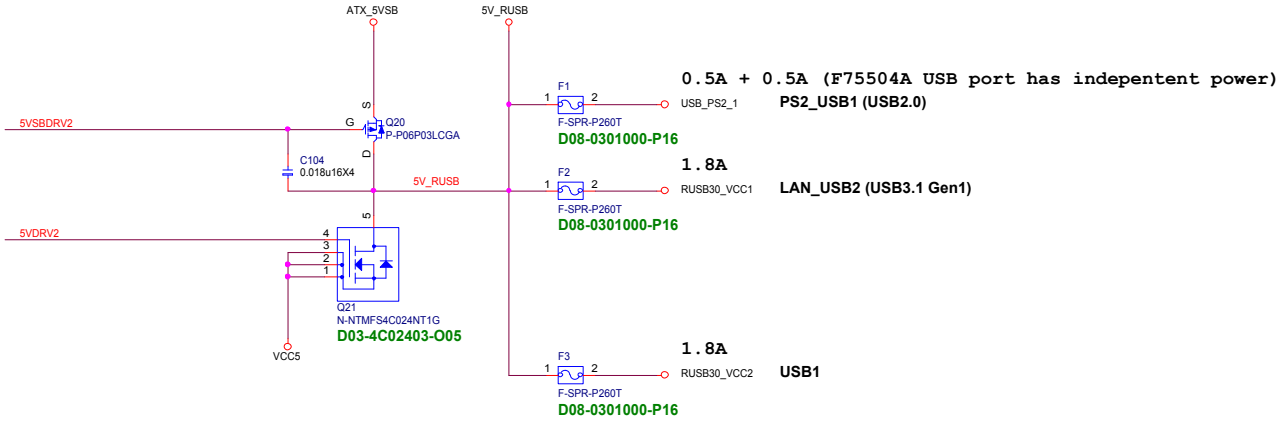
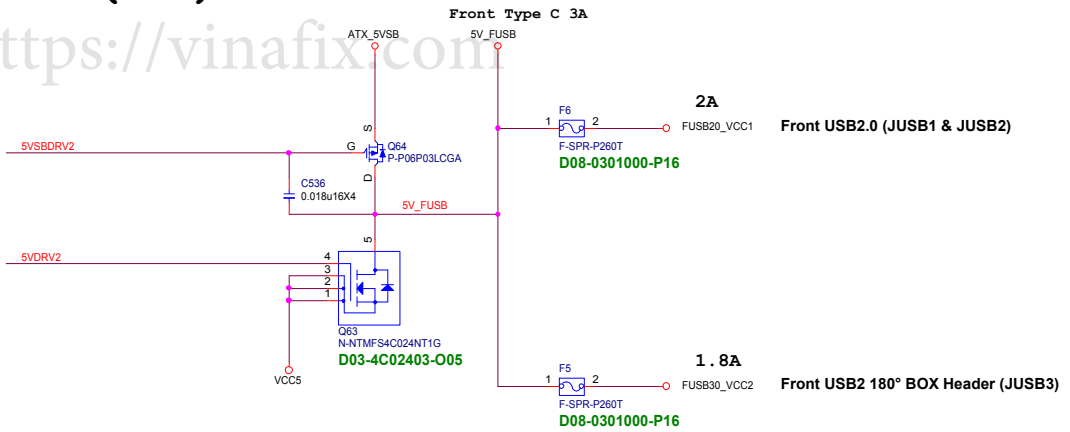
USB Power





Rear (4.6A)

Front (6.8A)



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MS-7C95		
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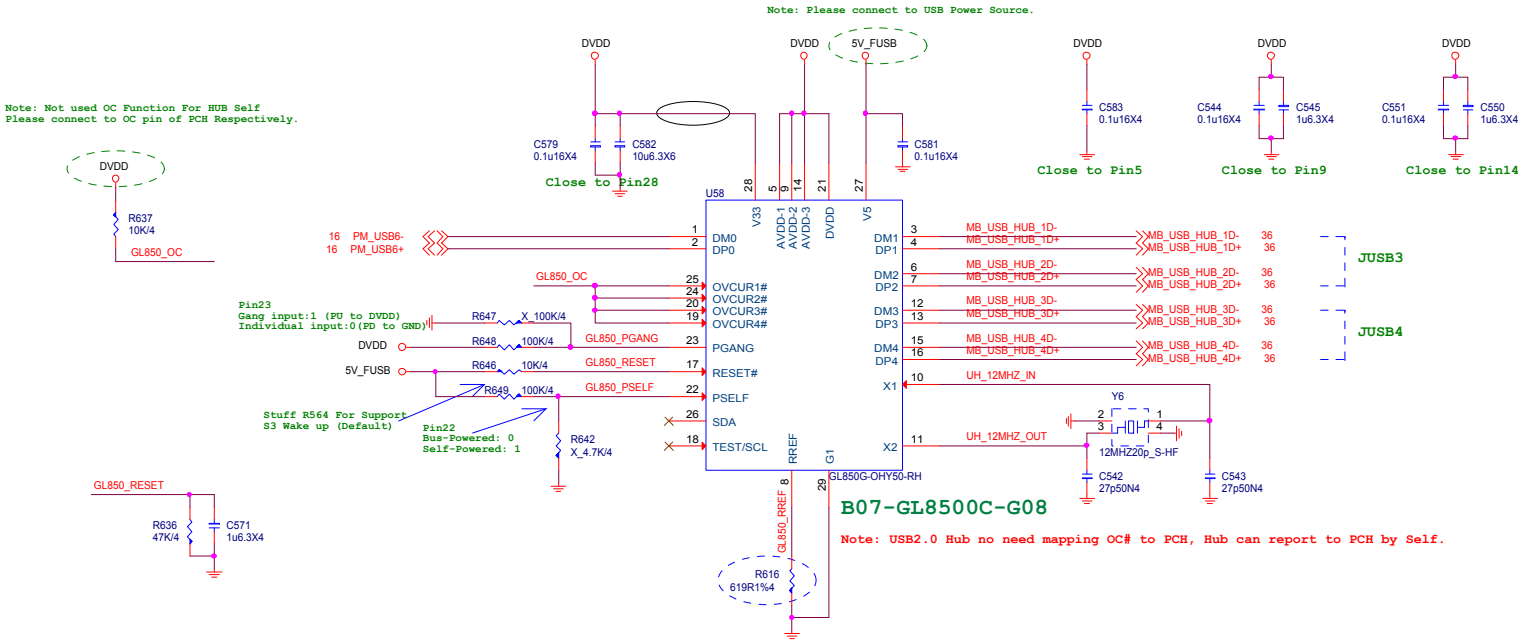
GL850G USB2.0 HUB



MICRO-STAR INT'L CO.,LTD		
MS-7C95		
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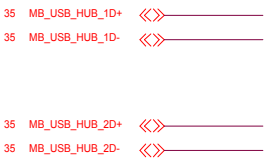
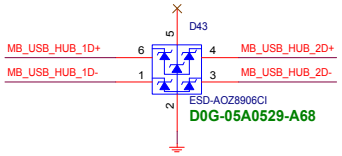
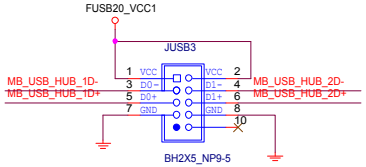
Front USB2.0(JUSB1)

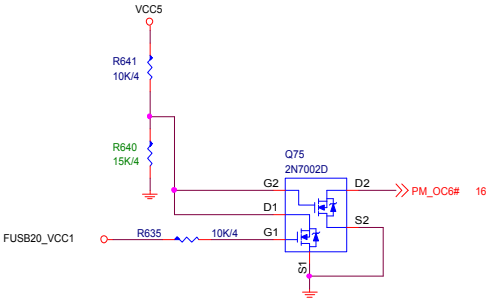
Form GL850G USB2.0 HUB

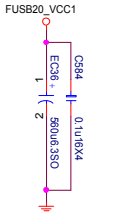
5V@1A









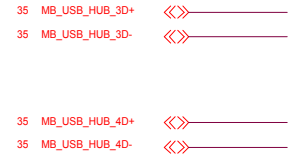


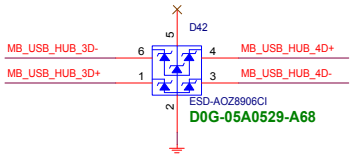
C71-56106R1-N07

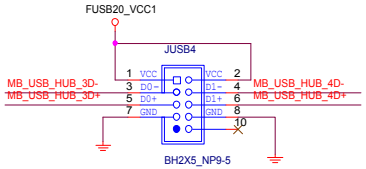
Front USB2.0(JUSB2)

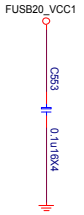
Form GL850G USB2.0 HUB

5V@1A









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MS-7C95		
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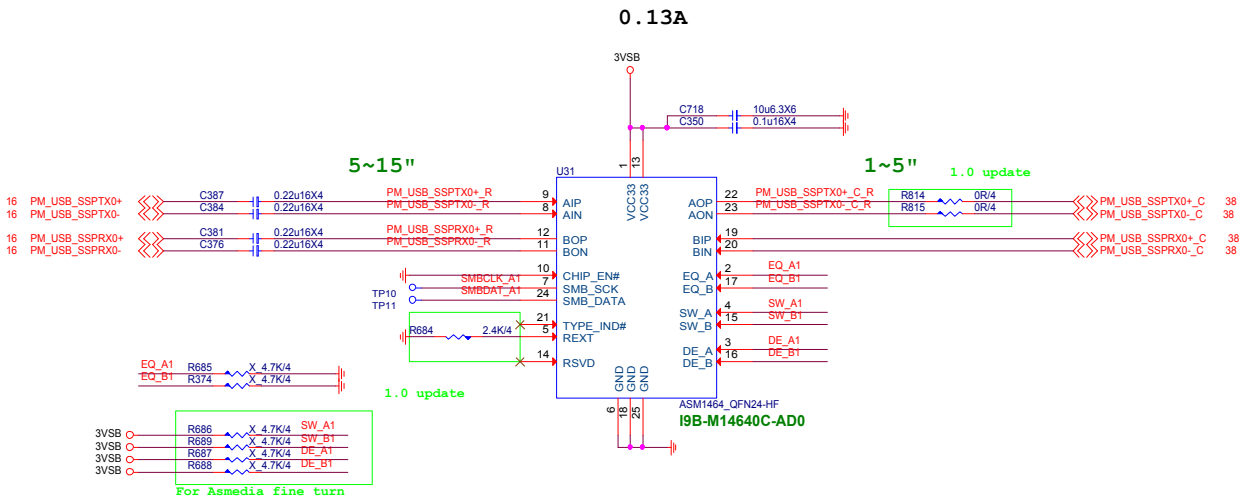
USB3.1 Gen1 Redriver for Type-C



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MS-7C95	
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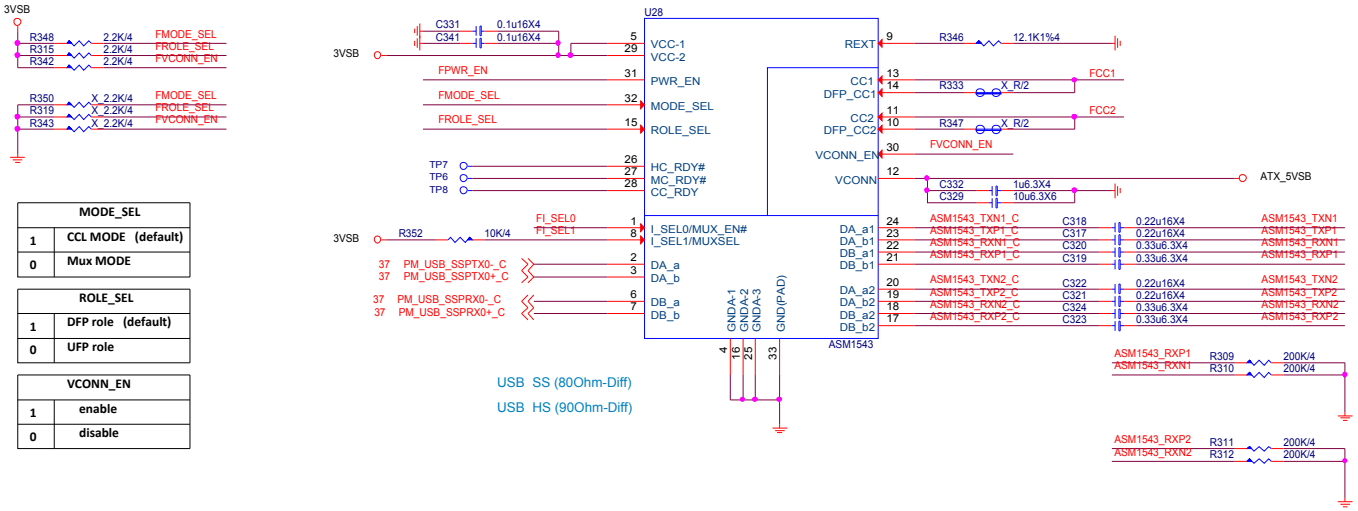
USB 3.1-Type-C

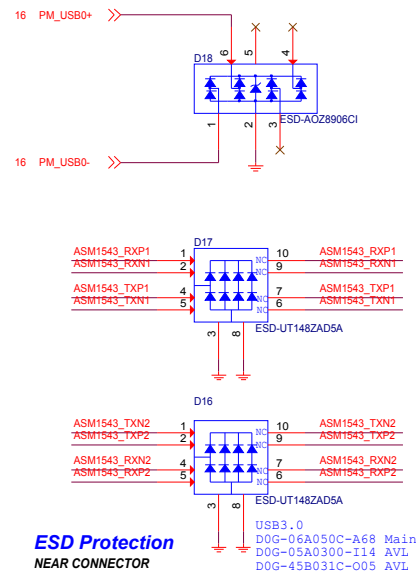
USB Type-C MUX with Configuration Channel (CC)



MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

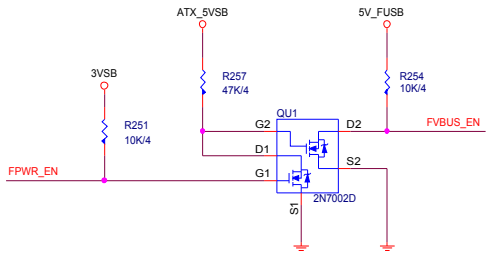
VCONN_EN	
1	enable
0	disable

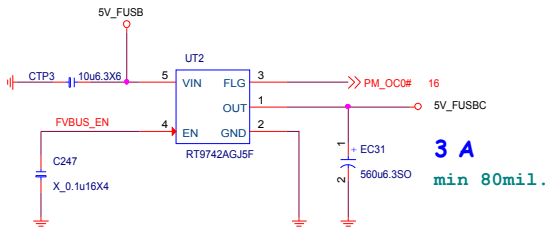


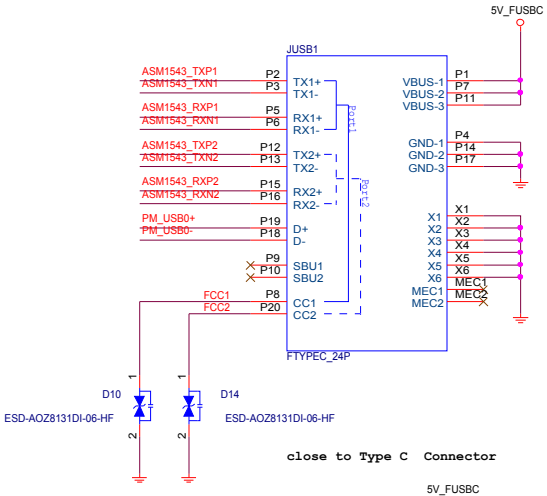
VBUS OC# LEVEL SHIFT

VBUS EN

VCOM OC#



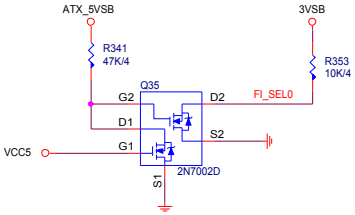




Current Mode

I_SEL0	I_SEL1	
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode



teknisi indonesia

MICRO-STAR INT'L CO.,LTD			
MS-7C95			
Size: Custom	Document Description: 38 Front USB3.0 Type C		Rev: 10
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Front USB3 180° BOX Header(JUSB3)

5V@1.8A

16 PM_USB2+
16 PM_USB2-
16 PM_USB3+
16 PM_USB3-

U47
PM_USB3+ / PM_USB3- → PM_USB3+ / PM_USB3-
PM_USB2+ / PM_USB2- → PM_USB2+ / PM_USB2-
ESD-UT148ZAD5A
D0G-28B030C-U33

16 PM_USB_SSTX0+ — C514 0.22u16X4 — PM_SSTX0+
16 PM_USB_SSTX0- — C523 0.22u16X4 — PM_SSTX0-
16 PM_USB_SSRX0+ — C532 0.33u6.3X4 — PM_SSRX0+
16 PM_USB_SSRX0- — C533 0.33u6.3X4 — PM_SSRX0-

U50
PM_SSTX0- / PM_SSTX0+ → PM_SSTX0- / PM_SSTX0+
PM_SSTX1- / PM_SSTX1+ → PM_SSTX1- / PM_SSTX1+
ESD-UT148ZAD5A
D0G-28B030C-U33

16 PM_USB_SSTX1+ — C510 0.22u16X4 — PM_SSTX1+
16 PM_USB_SSTX1- — C512 0.22u16X4 — PM_SSTX1-
16 PM_USB_SSRX1+ — C529 0.33u6.3X4 — PM_SSRX1+
16 PM_USB_SSRX1- — C531 0.33u6.3X4 — PM_SSRX1-

U53
PM_SSRX0- / PM_SSRX0+ → PM_SSRX0- / PM_SSRX0+
PM_SSRX1- / PM_SSRX1+ → PM_SSRX1- / PM_SSRX1+
ESD-UT148ZAD5A
D0G-28B030C-U33

VCC5
R602 10K/4
R599 15K/4
Q62 2N7002D
G2, D1, G1, D2, S2, S1
R760 X R/2
R761 X R/2
PM_OC2# 16
PM_OC3# 16
FUSB30_VCC2
R605 10K/4

FUSB30_VCC2
EC35 100u16SO
C535 0.1u16X4
C71-1011761-N07

JUSB2
PM_USB3+ 11 D2+
PM_USB3- 12 D2-
PM_SSTX1+ 14 TX2+
PM_SSTX1- 15 TX2-
PM_SSRX1+ 17 RX2+
PM_SSRX1- 18 RX2-
FUSB30_VCC2 19 VBUS2
16 GND
13 GND
PM_USB2+ 9 D1+
PM_USB2- 8 D1-
PM_SSTX0+ 6 TX1+
PM_SSTX0- 5 TX1-
PM_SSRX0+ 3 RX1+
PM_SSRX0- 2 RX1-
7 GND
FUSB30_VCC2 1 VBUS1
4 GND
10 NC
2X10_CONNECTOR
BH2X10[20]#-2PITCH_BLACK-RH-2
N32-2101581-H06

GEN1
1.8A
90 degree

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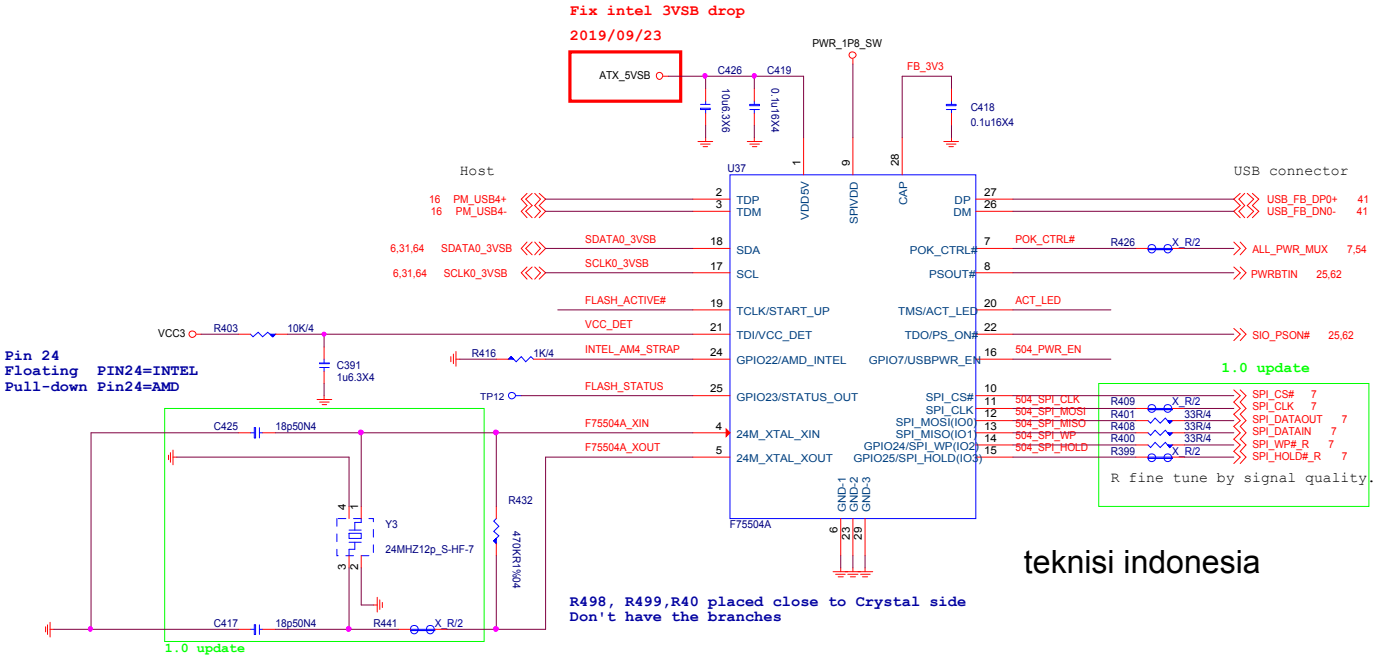
F75504A

F75504A/F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.



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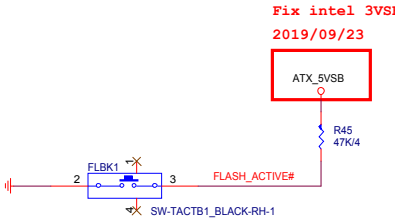

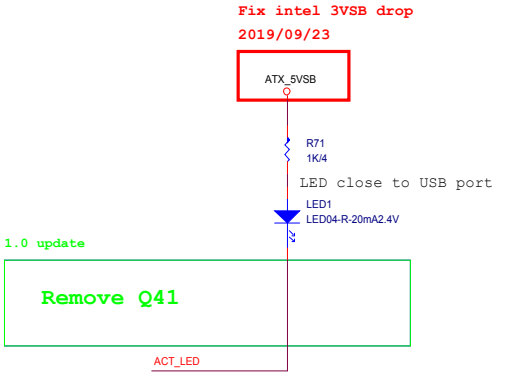

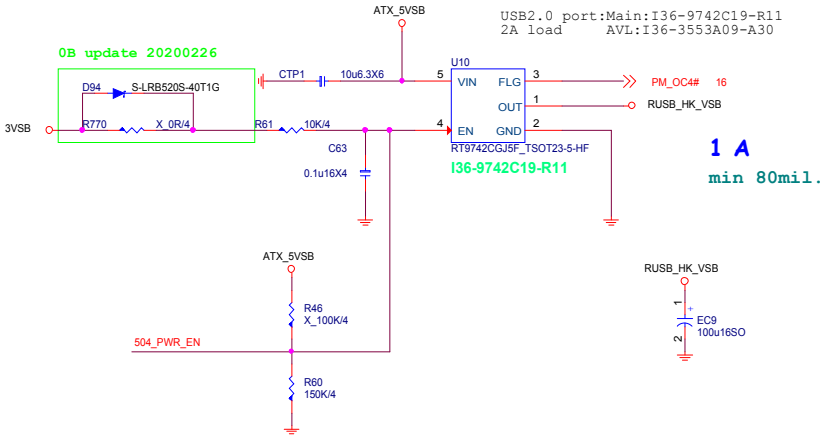

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MS-7C95		
Size: Custom	Document Description: 40 USB HOTKEY F75504A	Rev: 10
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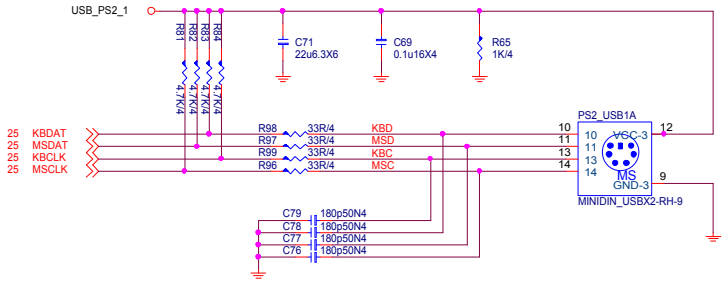
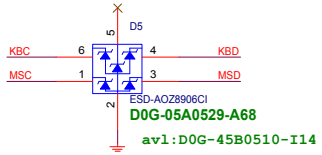
PS2+USB (USB2.0)

5V@1A

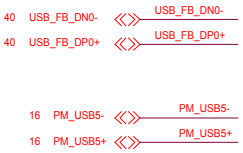
layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch



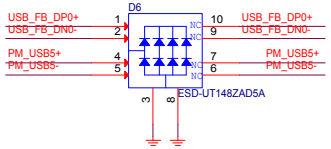


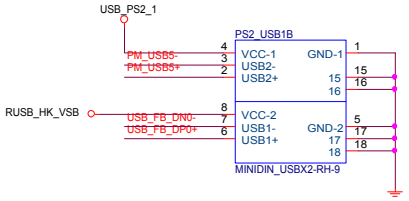
D0G-05A0529-A68

avl:D0G-45B0510-I14

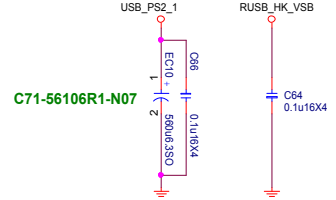


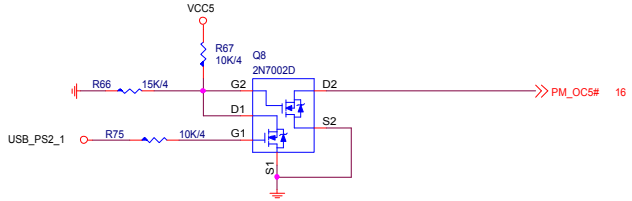
ESD close to connector.





1A **USB Flash BIOS**





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MS-7C95		
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Rear USB3.1 GEN2 5V@1.8A

TYPE A+C from CPU PI3EQX1004 Redriver

APU_USB2+ 7,42
APU_USB2- 7,42

APU_USB3+ 7,42
APU_USB3- 7,42

7 APU_USB_SSTX2+ — C224 0.22u16X4 — SSTX2+
7 APU_USB_SSTX2- — C218 0.22u16X4 — SSTX2-

7 APU_USB_SSRX2+ — C215 0.33u6.3X4 — SSRX2+
7 APU_USB_SSRX2- — C211 0.33u6.3X4 — SSRX2-

7 APU_USB_SSTX3- — C209 0.22u16X4 — SSTX3-
7 APU_USB_SSTX3+ — C203 0.22u16X4 — SSTX3+

7 APU_USB_SSRX3- — C200 0.33u6.3X4 — SSRX3-
7 APU_USB_SSRX3+ — C198 0.33u6.3X4 — SSRX3+

U66
7,42 APU_USB3+ — 1 — 10 — APU_USB3+
7,42 APU_USB3- — 2 — 9 — APU_USB3-
7,42 APU_USB2+ — 4 — 7 — APU_USB2+
7,42 APU_USB2- — 5 — 6 — APU_USB2-
3, 8 — ESD-UT148ZAD5A
D0G-28B030C-U33

U65
SSTX3+ — 1 — 10 — SSTX3+
SSTX3- — 2 — 9 — SSTX3-
SSTX2+ — 4 — 7 — SSTX2+
SSTX2- — 5 — 6 — SSTX2-
3, 8 — ESD-UT148ZAD5A
D0G-28B030C-U33

U64
SSRX2+ — 1 — 10 — SSRX2+
SSRX2- — 2 — 9 — SSRX2-
SSRX3+ — 4 — 7 — SSRX3+
SSRX3- — 5 — 6 — SSRX3-
3, 8 — ESD-UT148ZAD5A
D0G-28B030C-U33

1.8A
RUSB30_VCC2

HDMI_USB1B
APU_USB3+ — 31 D1+ — VBUS-1 — 20
APU_USB3- — 30 D1- — 26
SSTX3+ — 37 STAD_SSTX1+ — GND_DRAIN-1
SSTX3- — 36 STAD_SSTX1- — GND-1 — 23
UP
SSRX3+ — 34 STAD_SSRX1+ — SHELL-5 — X5
SSRX3- — 33 STAD_SSRX1- — SHELL-6 — X6
APU_USB2+ — 22 D0+ — VBUS-2 — 29
APU_USB2- — 21 D0- — 35
SSTX2+ — 28 STAD_SSTX0+ — GND_DRAIN-2
SSTX2- — 27 STAD_SSTX0- — GND-2 — 32
DOWN
SSRX2+ — 25 STAD_SSRX0+ — SHELL-7 — X7
SSRX2- — 24 STAD_SSRX0- — SHELL-8 — X8
USB3.0X2_HDMI_BRASS-RH

RUSB30_VCC2
EC25 560u6.3SO — C180 0.1u16X4 — C181 1u6.3X4
C71-56106R1-N07

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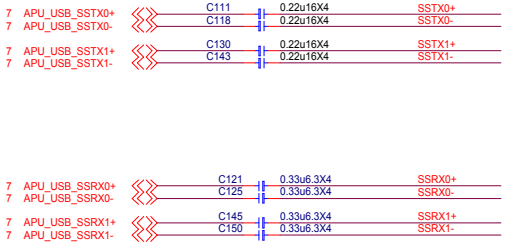
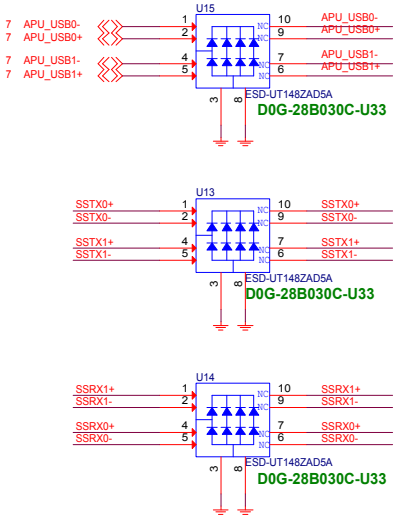
Rear USB3.1 GEN1 5V@1.8A

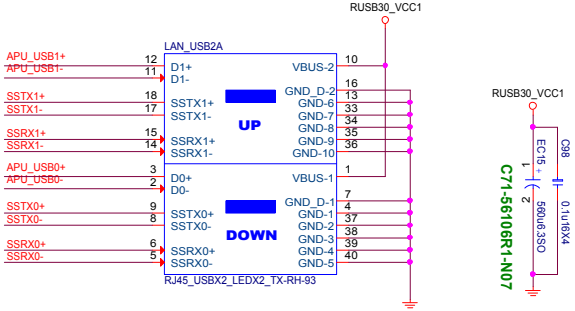
TYPE-A X2 from CPU



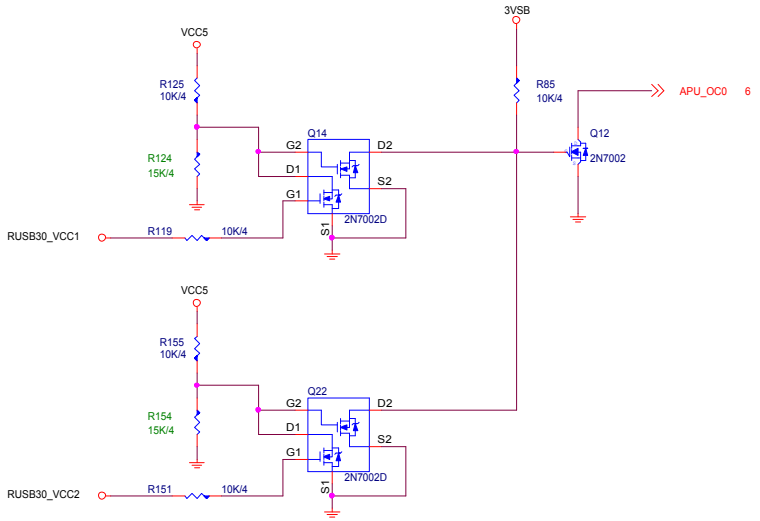


LAN下方

GEN1 1.8A



CPU OC Logic



Type1/2/3/4 High Active

	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

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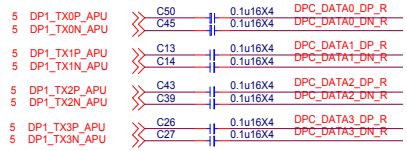
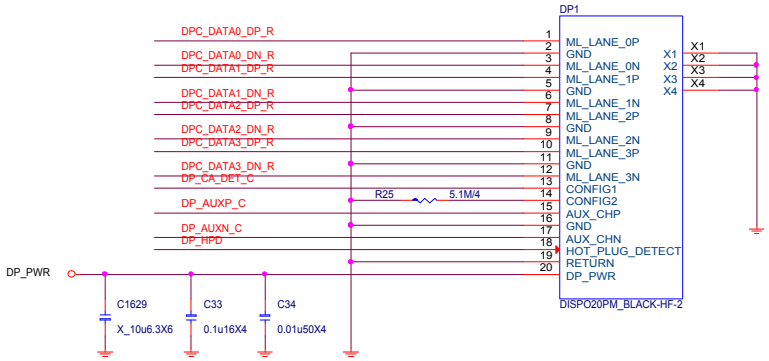
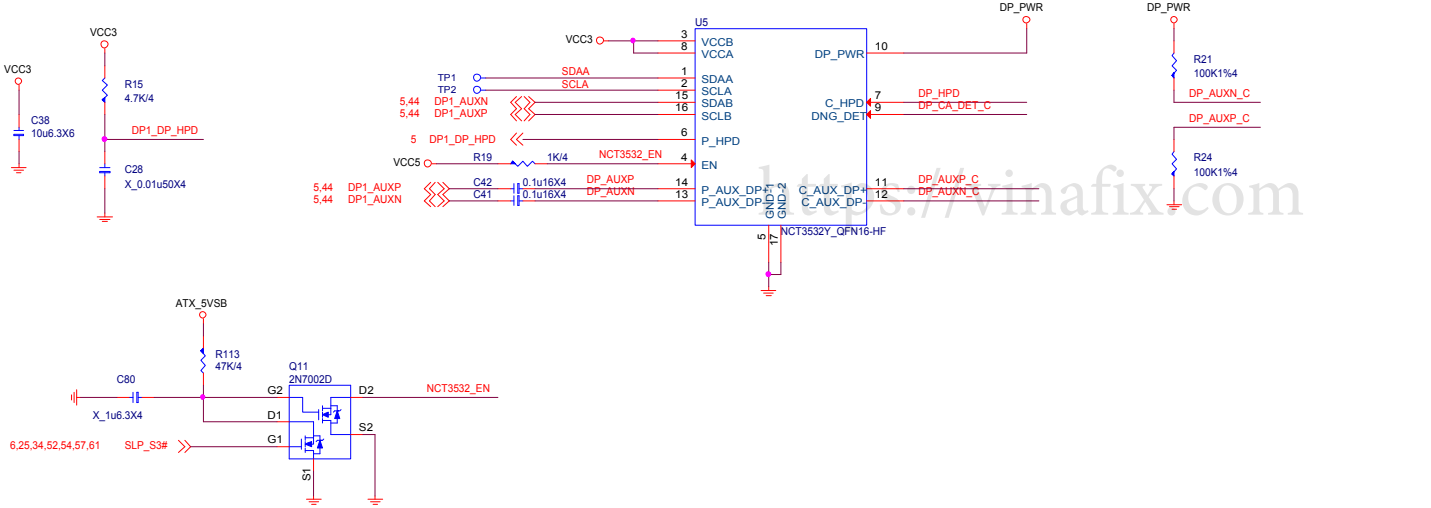
DP CONNECTOR



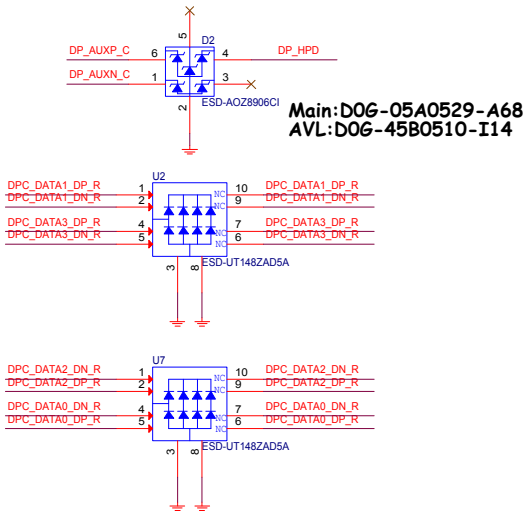


DP AUX & HPD Circuit

Support HDMI Dongle



ESD



Vinafix.com

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Custom	44 DP	10

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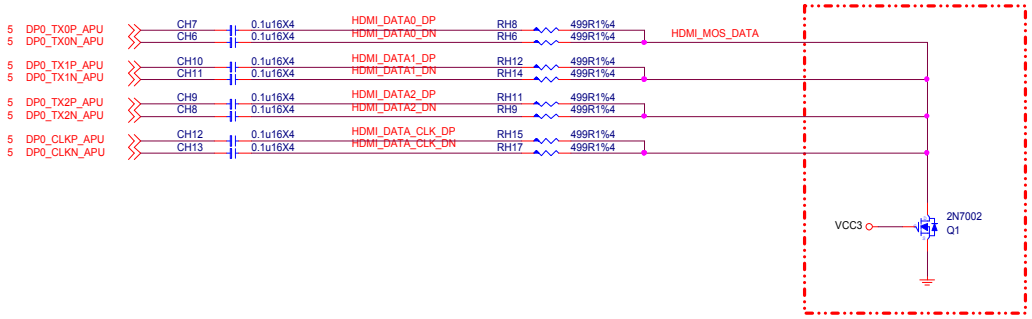
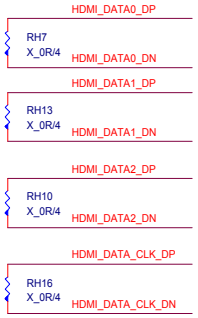
HDMI CONNECTOR

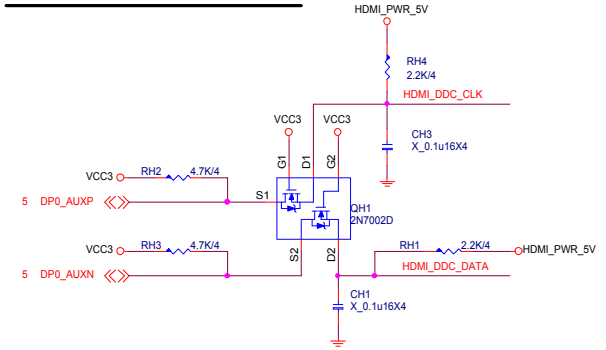
For HDMI 1.4



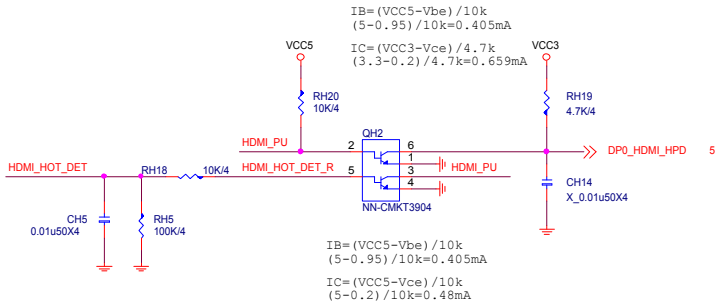


HDMI_MOS_DATA trace length <500mil
other platform please check design guide

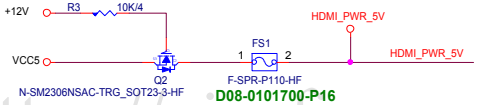
AUX Level Shifter



HPD Circuit

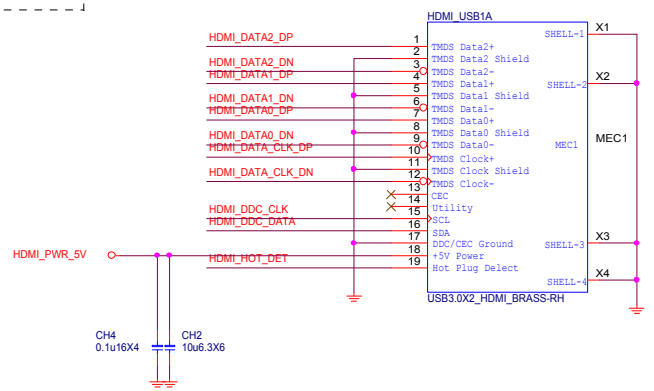


Connector Power

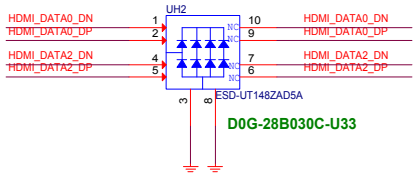


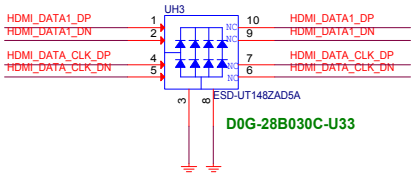
如果用DIODE SA測試電壓會不過

Connector

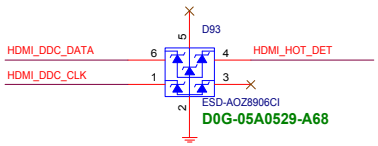


For EMI





注意:耐壓5V零件



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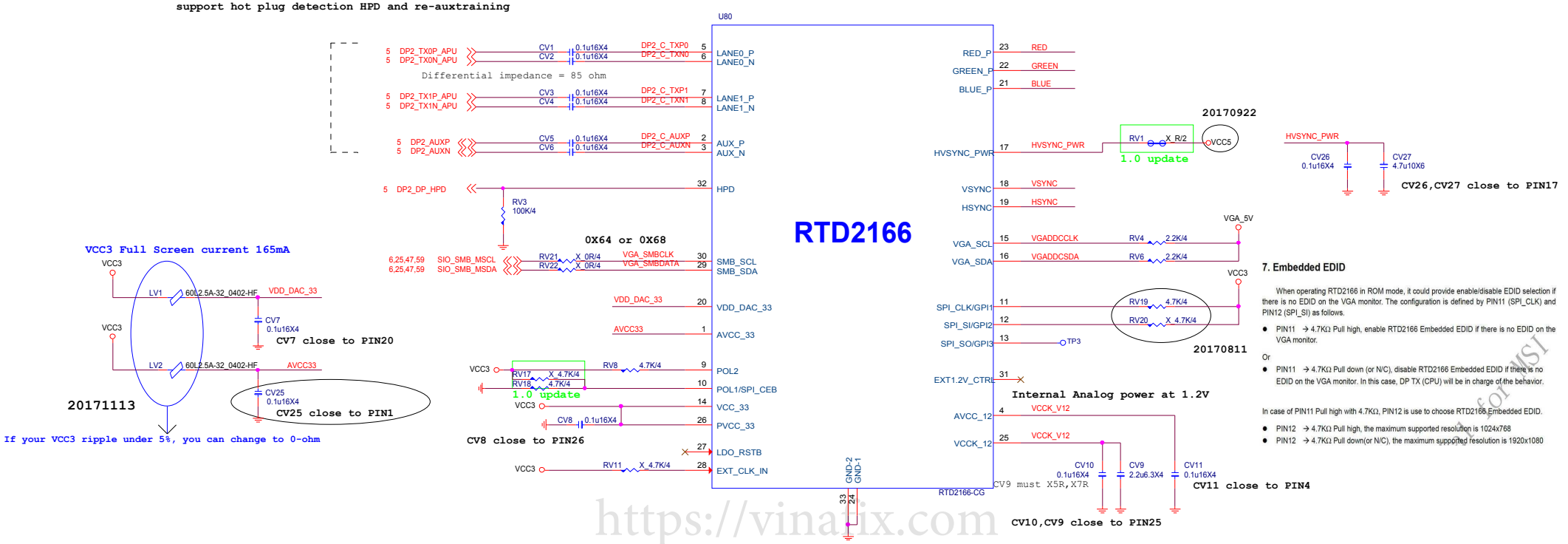
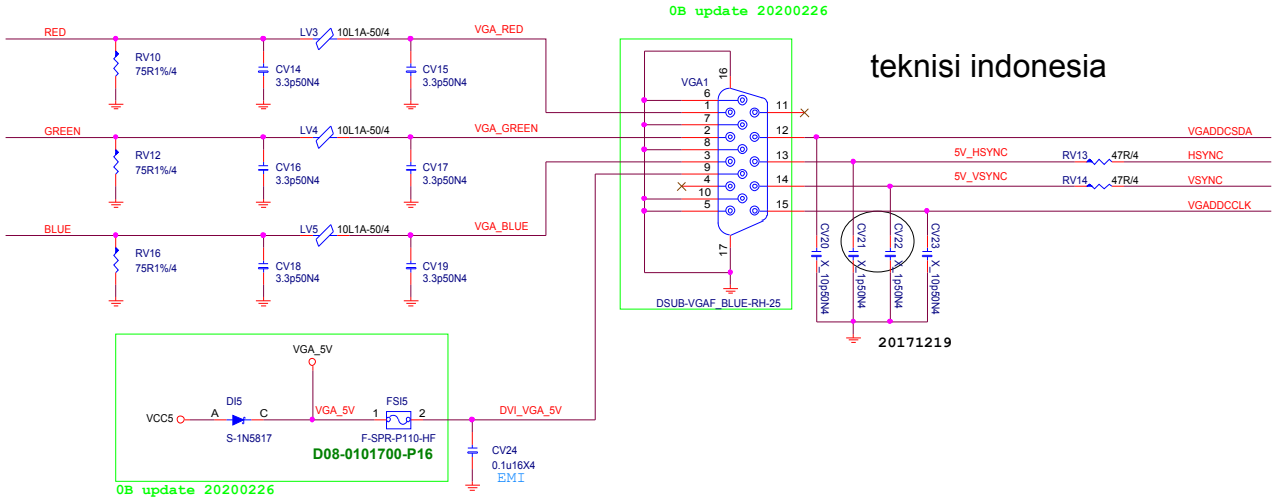
Note:

If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining





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MS-7C95	
Size: Custom	Document Description: 45 HDMI
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Vcore GROUP G TDC:95A,EDC:140A
NB GROUP C TDC:50A,EDC75A

Note: VID Override Circuit

SVC	SVD	BOOT VOLTAGE Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

0X40

VR87,VR84change LL R↑ LL↓

VR18,VR27 change LL R↑ LL↓

RT8894AGQW_WQFN56-HF

I32-8894J0C-R11

SET1 control ICCMAX,OCP setting
SET2 control Internal compensation

VCORE IccMAX: 140A =>OCP=>180A (4 x 45A)
LL=1.3m ohm
VCC_NB IccMAX: 75A =>OCP=> 90A
LL 2.1m ohm
FSK:250K

1.0 update

VRHOT=150 degree, 115 degree reset
Close to PWM
Close to MOSFET

VRHOT=125 degree, 90 degree reset
Close to PWM
Close to MOSFET

close to PWM
close to phase1 CHOKE

close to PWM
close to phase1 CHOKE

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MS-7C95	
Size: Custom	Document Description: 46 CPU Power RT8894J 4+2
Rev: 10	
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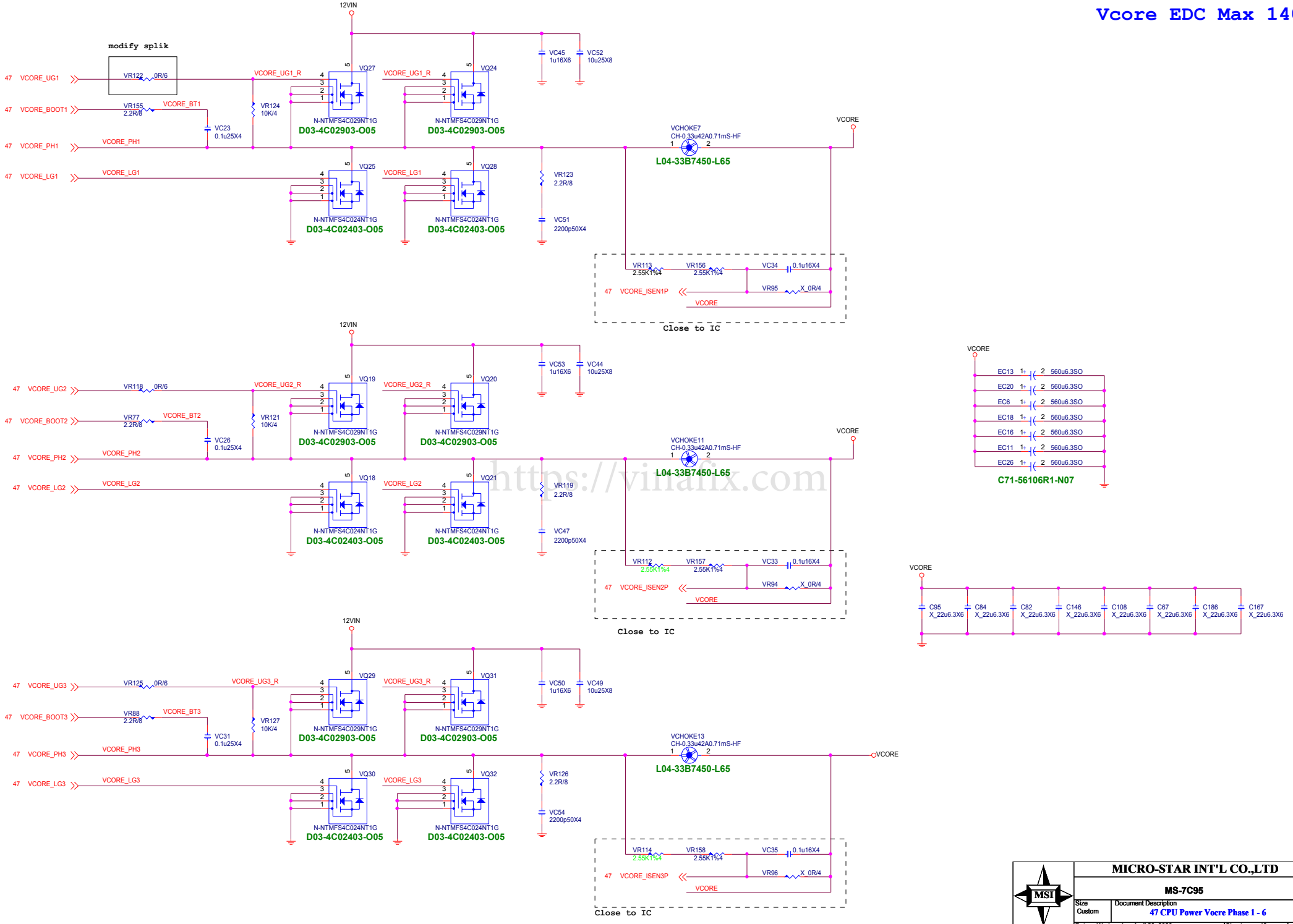
Vcore EDC Max 140A



MICRO-STAR INT'L CO.,LTD

MS-7C95

Size	Document Description	Rev
Custom	47 CPU Power Vocre Phase 1 - 6	10

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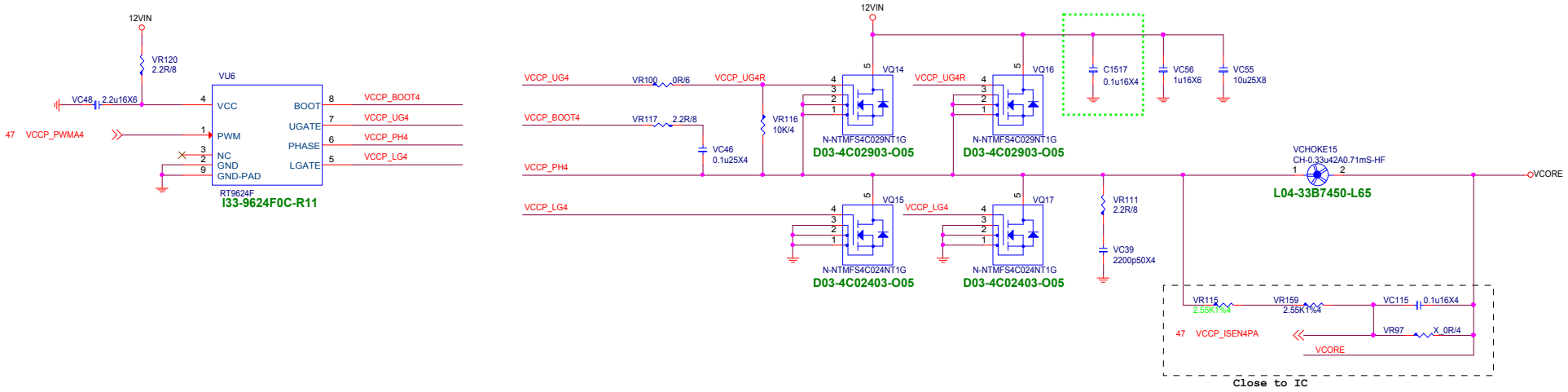

MICRO-STAR INT'L CO.,LTD		
MS-7C95		
Size: Custom	Document Description: 48 CPU Power Vcore Phase 7 - 8	Rev: 10
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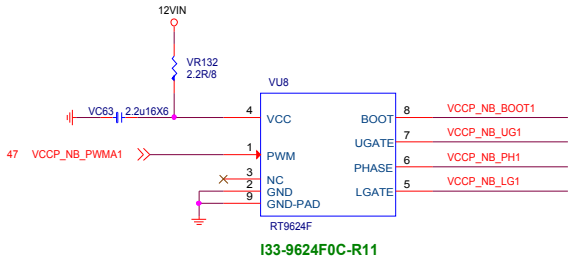
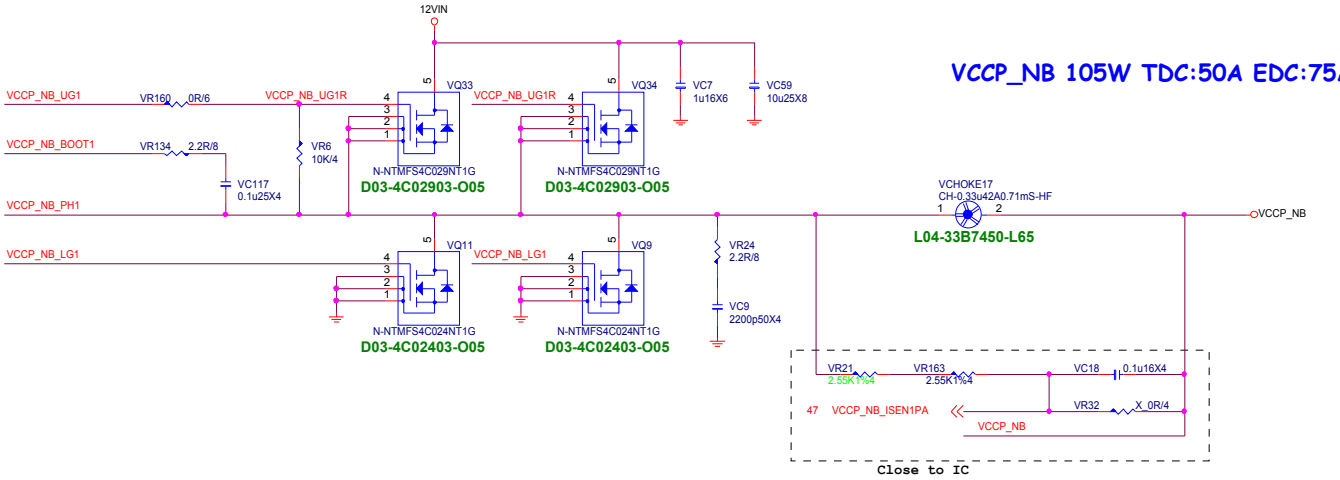
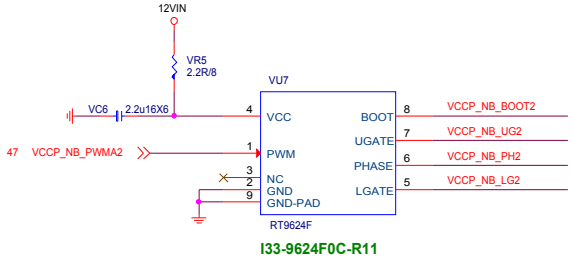
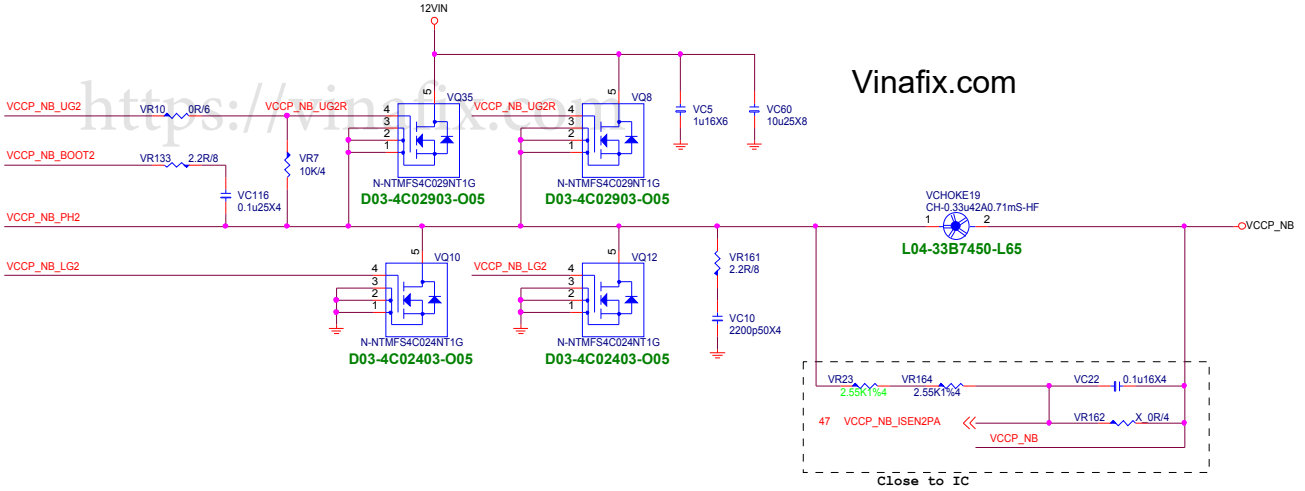
SOC EDC Max 75A

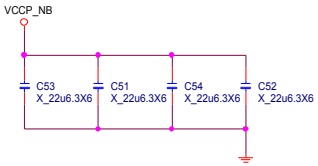
VCCP_NB 105W TDC:50A EDC:75A

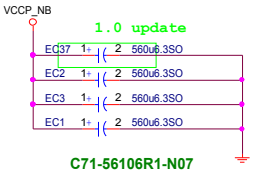




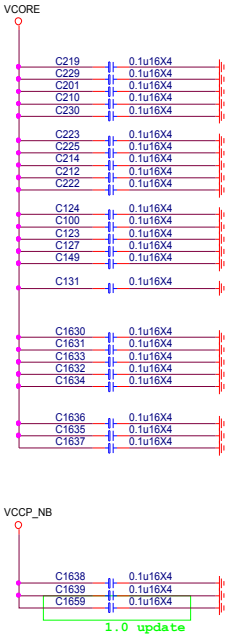








MICRO-STAR INT'L CO.,LTD		
MS-7C95		
Size: Custom	Document Description: 49 CPU Power NB Phase 1-2	Rev: 10
Date: Wednesday, April 29, 2020	Sheet 50 of 74	



MICRO-STAR INT'L CO.,LTD

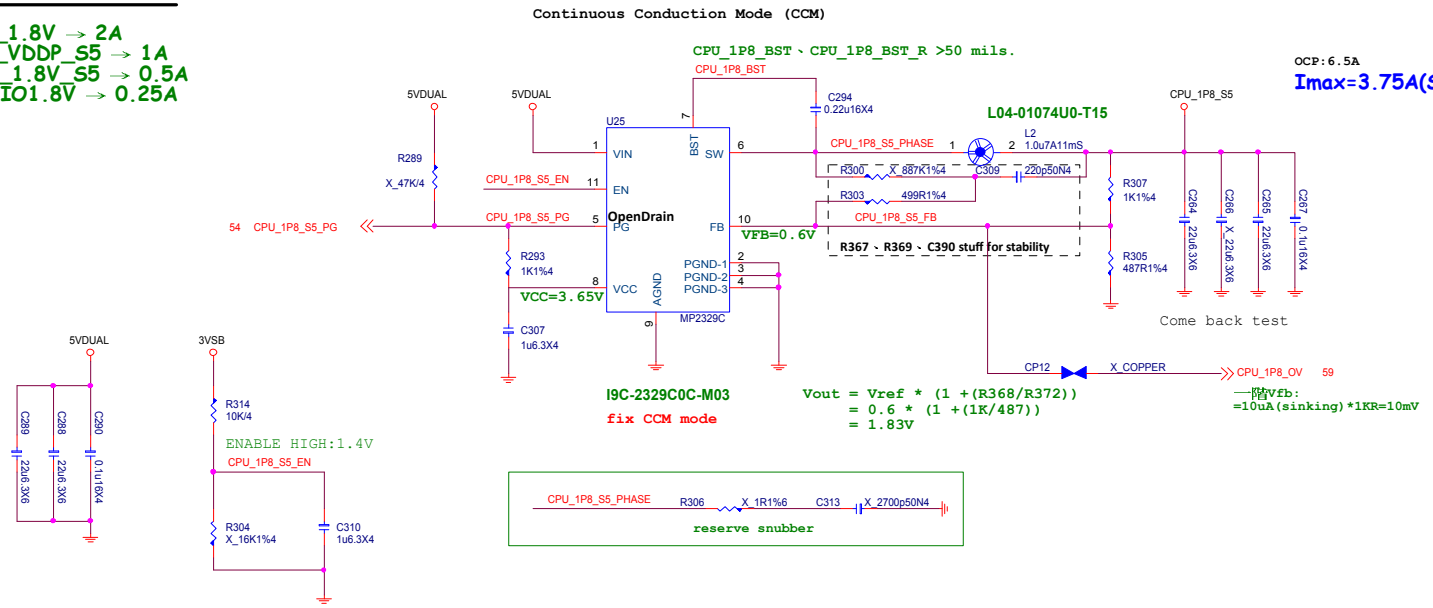
MS-7C95

Size	Document Description	Rev
Custom	50 Decoupling Capacitance	10

Date: Wednesday, April 29, 2020 Sheet 51 of 74

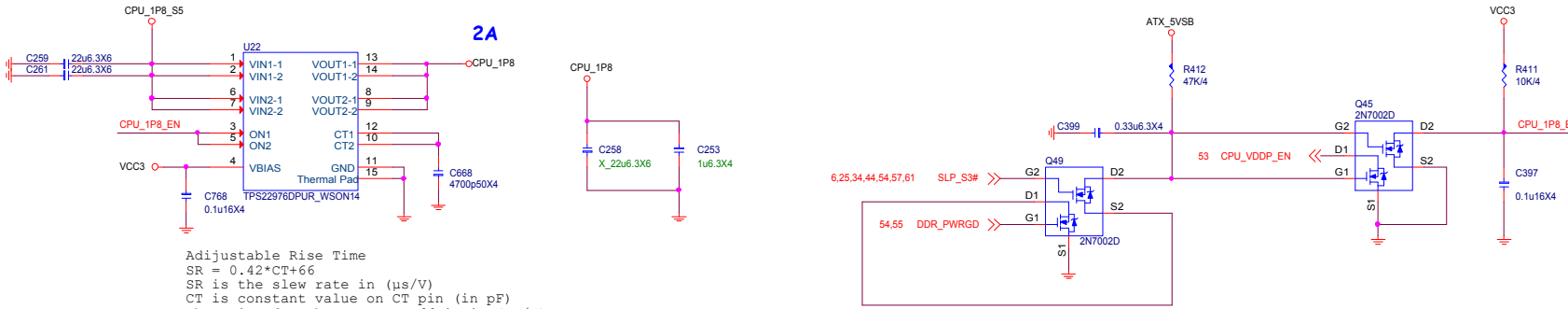
CPU 1.8V S5

CPU_1.8V → 2A
CPU_VDDP_S5 → 1A
VDD_1.8V_S5 → 0.5A
AUDIO1.8V → 0.25A



CPU 1.8V S0

CPU 1.8V_S0@2A



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Size: Custom	Document Description: 51 CPU Power 1.8_S0 / S5
Rev: 10	
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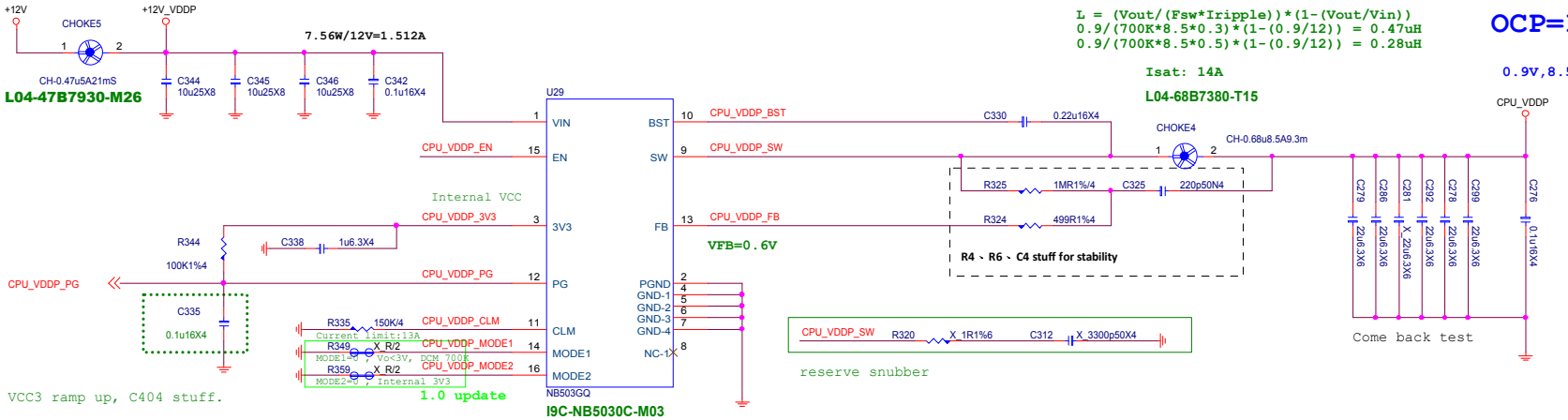
CPU_VDDP_S0

0.9V@S0:8.5A

S0:8.5A

```
Input Current = (13A*0.9V)/12V/0.8 = 1.22A
Choke Isat = 8A
Irms=Iout*SQRT((Vo/Vi)*(1-(Vo/Vi)))
=13*SQRT((0.9/12)*(1-(0.9/12))) = 3.42A
Choke Irms =5 A
```




```
L = (Vout/(Fsw*Iripple))*(1-(Vout/Vin))
0.9/(700K*8.5*0.3)*(1-(0.9/12)) = 0.47uH
0.9/(700K*8.5*0.5)*(1-(0.9/12)) = 0.28uH
```

OCP=13A

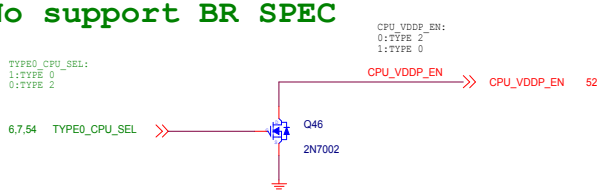
Isat: 14A

L04-68B7380-T15

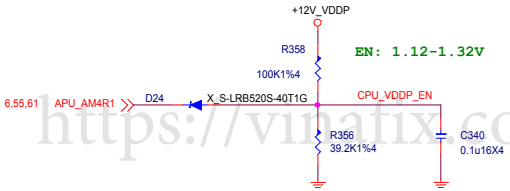
0.9V,8.5A,7.65W

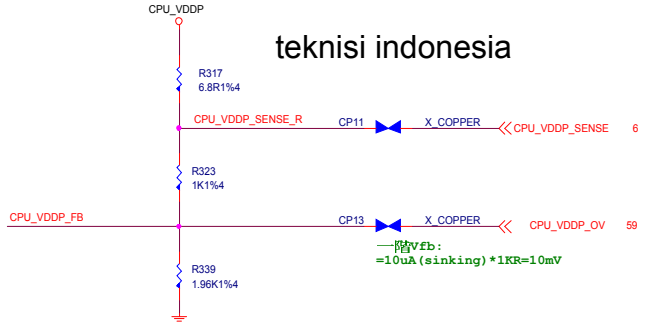
```
20180822
fix PG glitch when VCC3 ramp up, C404 stuff.
```

No support BR SPEC



CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN	
BR	0	1	0	1	SPEC no Support
NA	X	0	0	0	
SR	2	1	1	0	NOT SUPPORT TYPE2
RV/ZP	3	0	1	1	
MTS	4	1	1	1	NOT SUPPORT TYPE4



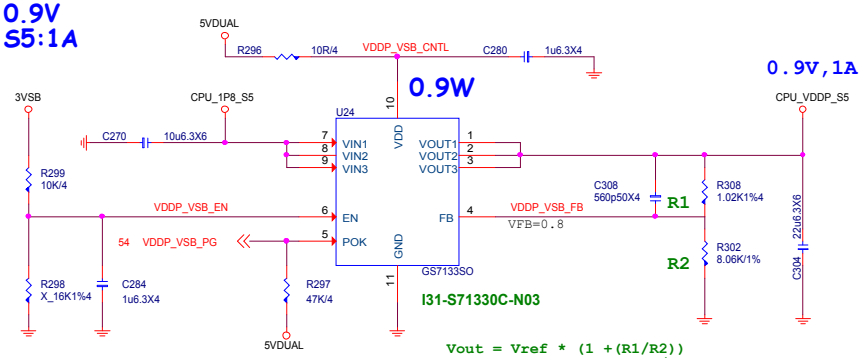



```
Vout = Vref + (R1*R4*Vref)/(R2*(R1+R4))
     = 0.6+(1k*1000k*0.6)/(1.96K*(1k+1000k))
     = 0.9058V
```

CPU_VDDP_S5

0.9V

S5:1A




```
Vout = Vref * (1 +(R1/R2))
     = 0.8 * (1 +(1.02K/8.06K))
     = 0.9V
```

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Custom	52 CPU Power VDDP-NB503/GS7133	10
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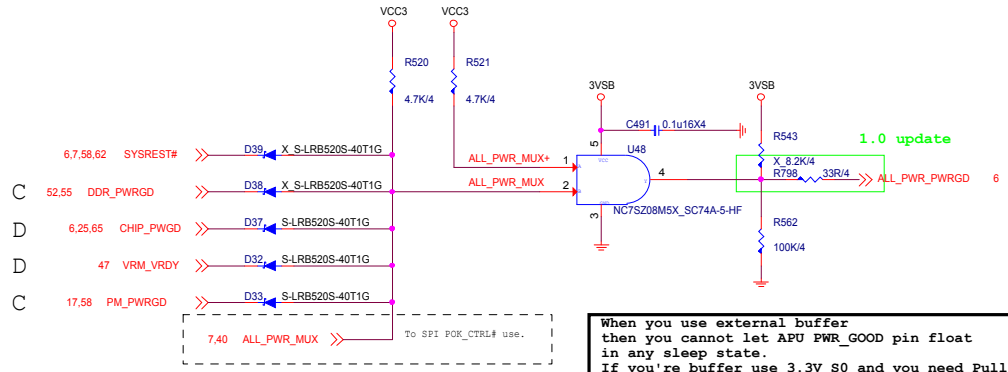
ALL POWER GOOD MUX

S0 PG

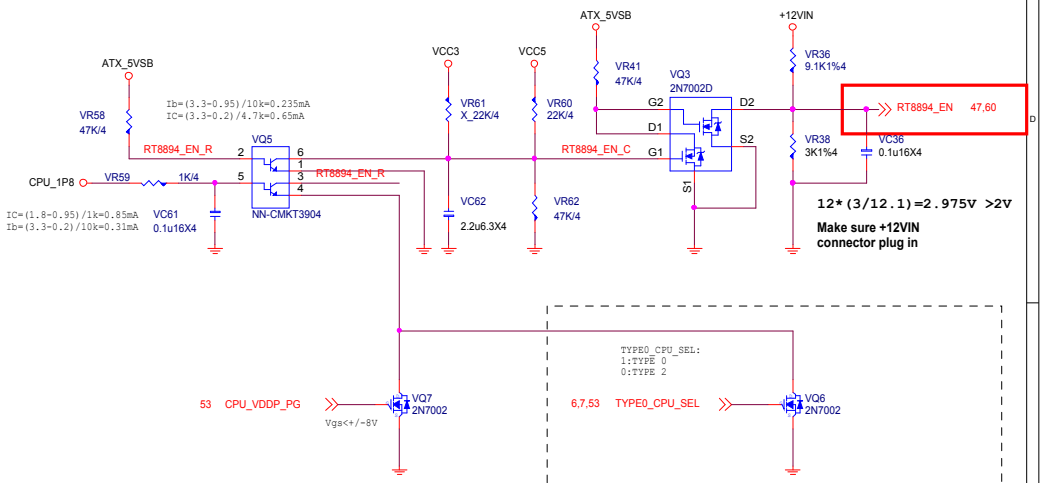


When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

VRM_Enable circuit

1.0 update

remove D3



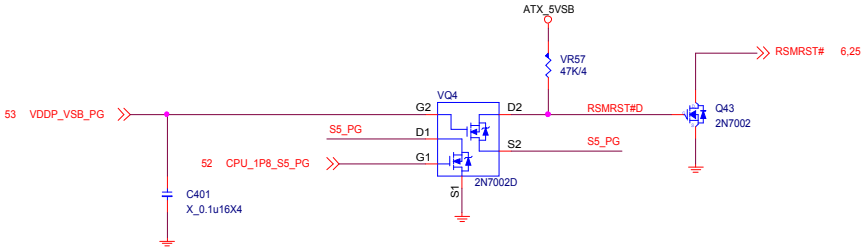
SPEC no Support

CPU VDDP NOT SUPPORT TYPE2

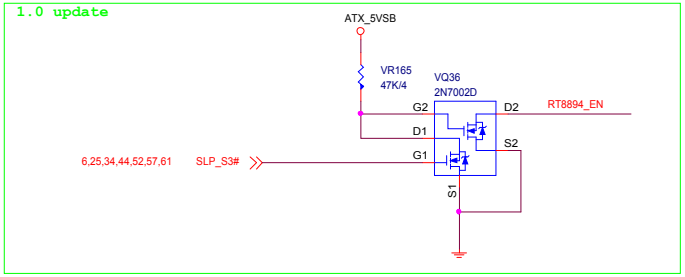
CPU VDDP NOT SUPPORT TYPE4

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0
MTS	4	1	1

S5 PG



1.0 update



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MS-7C95	
Size: Custom	Document Description: 53 VRM PWRGD
Rev: 10	
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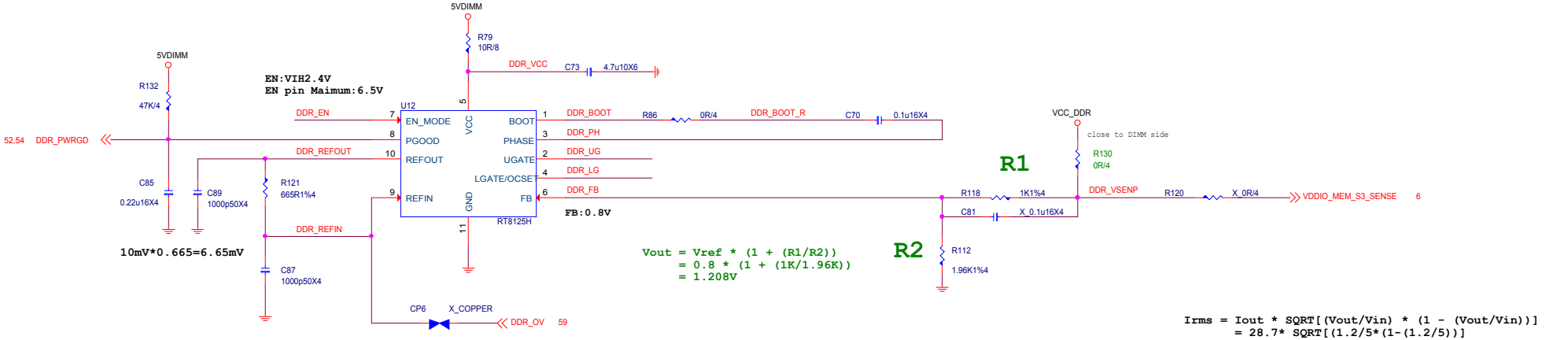
DDR4_1.2V@28.7A

18A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

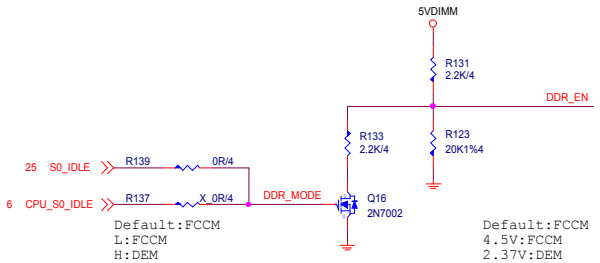
OCP = 35A; Choke Isat=42A

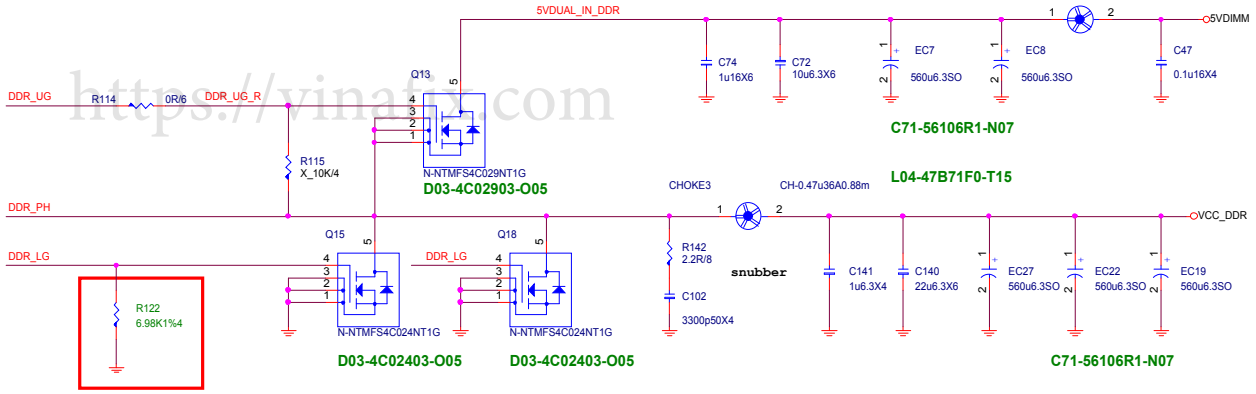
Rocset = 1.5 * Imax * Rdson(low) / Iocset
R649 = 1.5 * 28.7 * 2mohm / 10uA
R649 = 8.61K

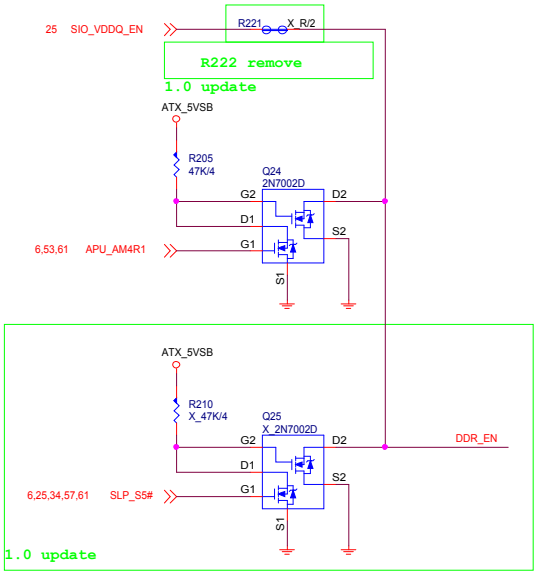
Rdson(Low Side) 5V
D03-4C02403-005:3.3 ~ 4mohm



Irms = Iout * SQRT[(Vout/Vin) * (1 - (Vout/Vin))]
= 28.7* SQRT[(1.2/5*(1-(1.2/5))]
= 11.15A







MICRO-STAR INT'L CO.,LTD

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Custom	54 DDR PWR - RT8125E	10

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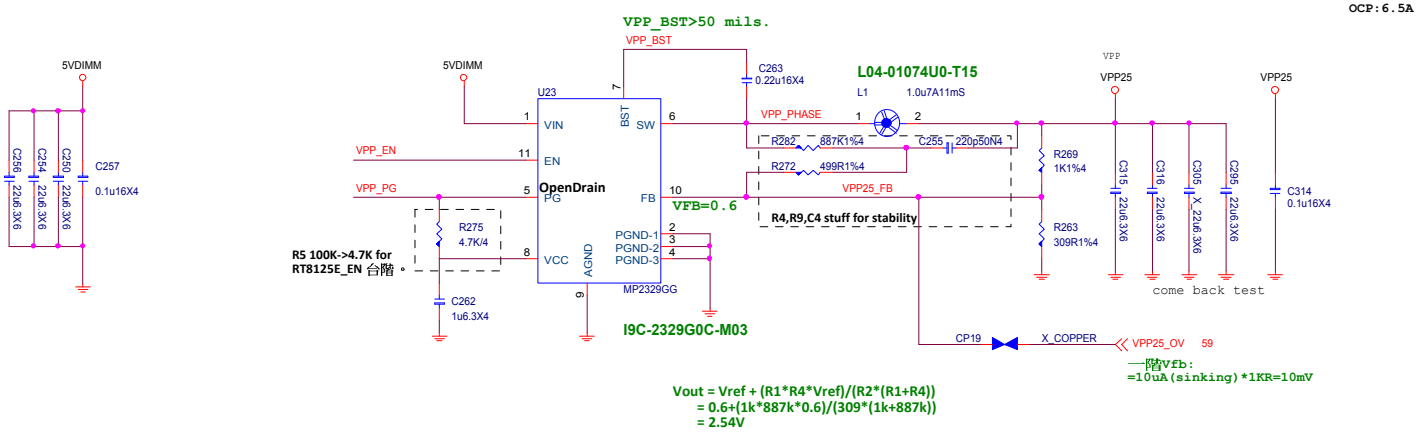
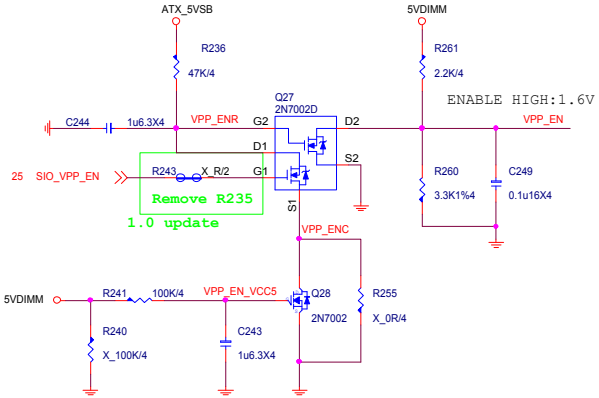
4DIMM : VPP25

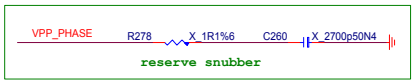
2.5V@2.24A

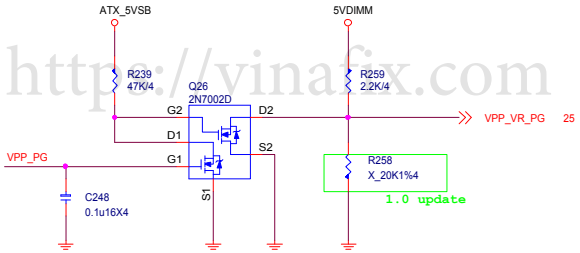
OCP:6.5A



Vout = Vref + (R1*R4*Vref)/(R2*(R1+R4))
= 0.6+(1k*887k*0.6)/(309*(1k+887k))
= 2.54V

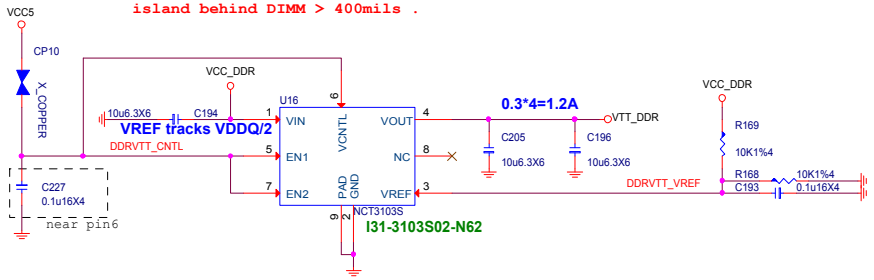


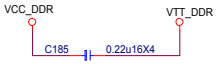


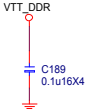


DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .







MICRO-STAR INT'L CO.,LTD

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Custom	55 DDR PWR - VPP25 / VTT	10

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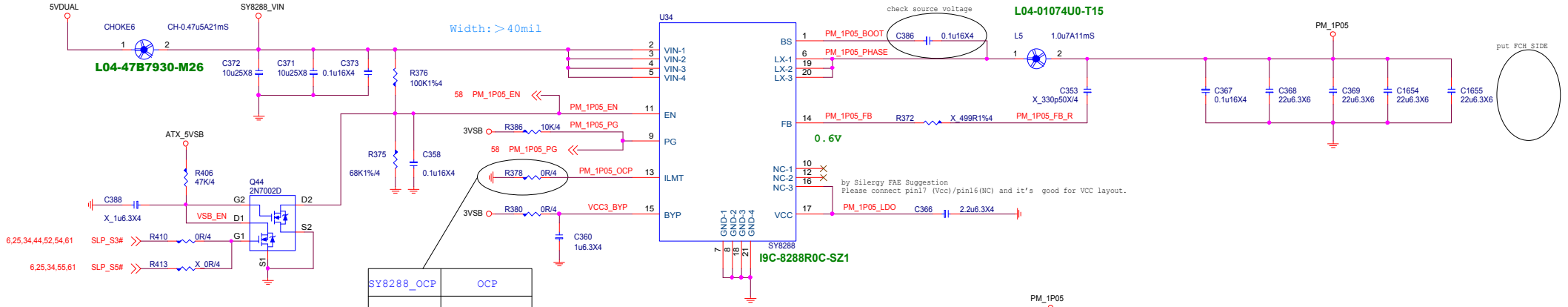
FOR Promontory 1.05V_S0

1.05V
S0:5.5A

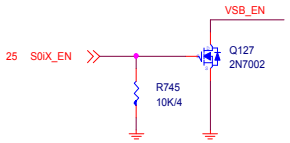
Input Current= (8A*1.05V)/5V/0.85=1.976A

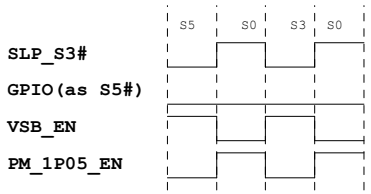
OCP=8A

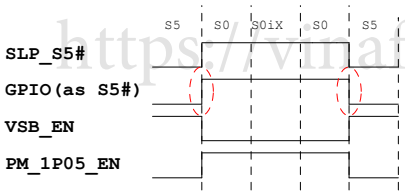
1.05V@5.5A



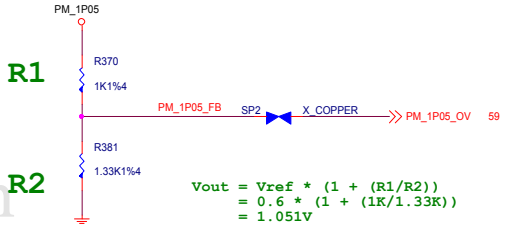
SY8288_OCP	OCP
0	8A
floating	12A
1	16A







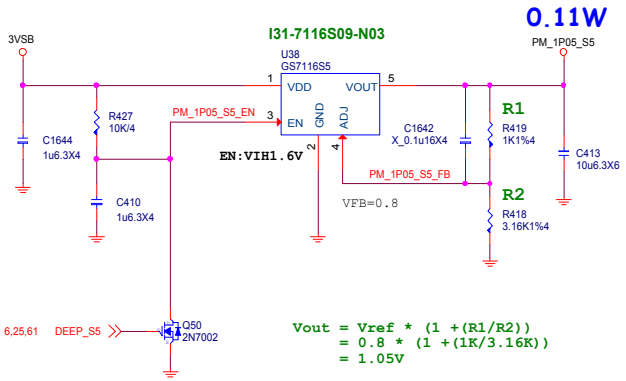
teknisi indonesia



Vout = Vref * (1 + (R1/R2))
= 0.6 * (1 + (1K/1.33K))
= 1.051v

FOR PROM PM_1P05_S5

1.05V@0.05A



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(1K/3.16K))
= 1.05V

MICRO-STAR INT'L CO.,LTD

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Custom	56 PM - SY8288/PM_1P05	10

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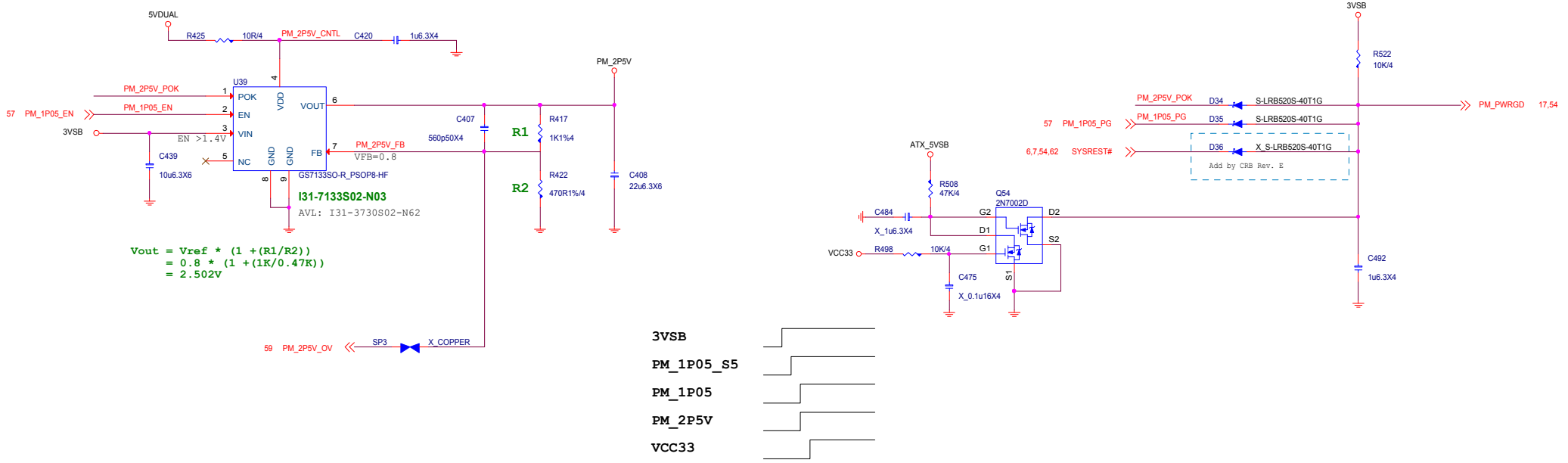
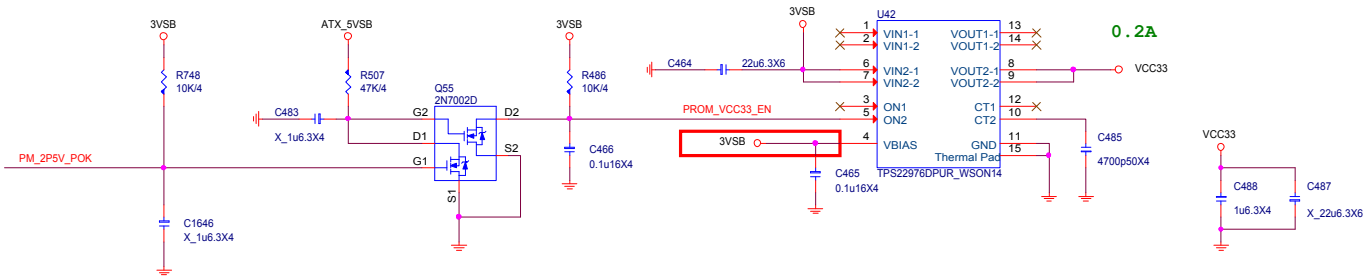
Promontory-2.5V

2.5V@900mA



VCC33 VCC33@0.2A



Adijustable Rise Time
SR = 0.42*CT+66
SR is the slew rate in (μs/V)
CT is constant value on CT pin (in pF)
The units for the constant 66 is in (μs/V)

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MS-7C95			
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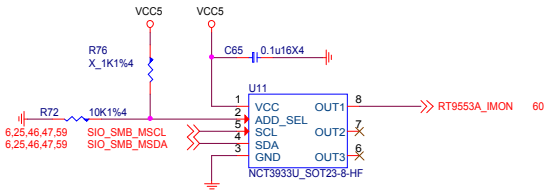
Over Voltage Control IC

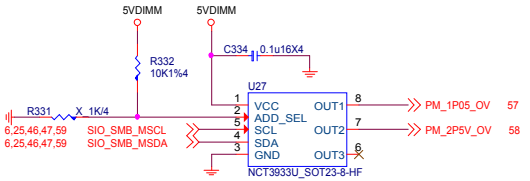
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

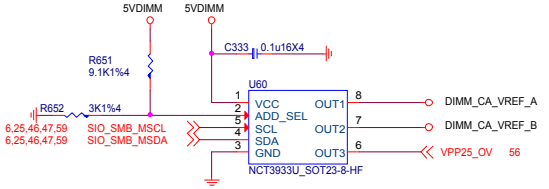
0x2A:RH=OPEN,RL=10K



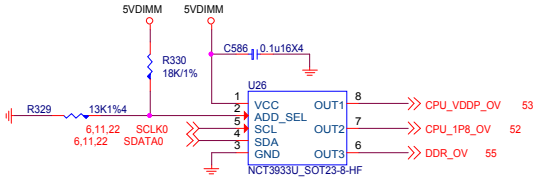
0x20:RH=10K,RL=OPEN



0x28:RH=9.1K,RL=3K



0x26:RH=18K,RL=13K



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	58 OV Control - NCT3933	10

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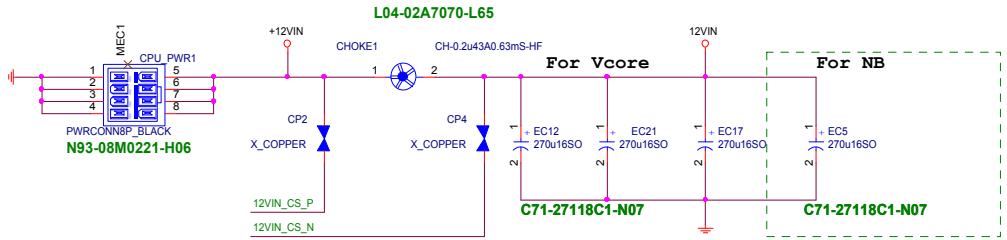
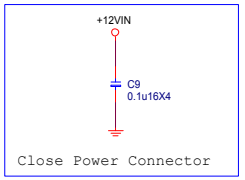
CPU POWER CONNECTOR

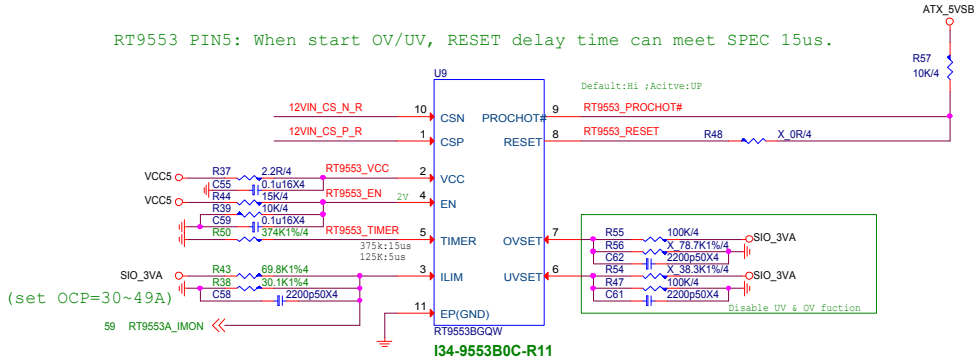


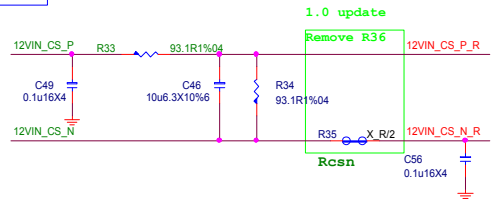


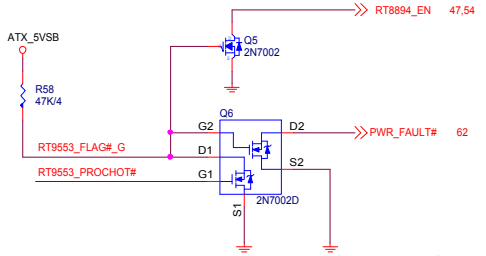
Vcore			
D=Vout/Vin			
Vin	= 12		> input voltage
Vout	= 2		> output Vcore
D	= 0.166667		
I o = Icore(max)*0.8			
I core(max)	= 200		> Vcore current
I avg.	= 160	A	
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	= 10	phase	
I ripple	= 5.962848	A	
How many pcs. Of Cap.			
I ripple(cap)	= 4700	m A	
COE TEMP	= 1		
Input Cap.	= 2	pcs.	

SOC			
D=Vout/Vin			
Vin	= 12		> input voltage
Vout	= 1.55		> output Vcore
D	= 0.129167		
I o = Icore(max)*0.8			
I core(max)	= 75		> Vcore current
I avg.	= 60	A	
I ripple={ Io*√D*√(1-D)} / Phase			
Phase	= 2	phase	
I ripple	= 10.06153	A	
How many pcs. Of Cap.			
I ripple(cap)	= 4700	m A	
COE TEMP	= 1		
Input Cap.	= 3	pcs.	

RT9553B CURRENT SENSE







ΔVILIM=10uA*[(69.8K*30.1K)/(69.8K+30.1K)]
=210mV

Isense = VILIM / 100*Rsense
ΔIsense=210mV/(100*0.63m)=3.3333A

DCR Network				
Parameter	Value	Unit	Note	
C_real (Effective capacitance)	7	uF	Please note the effective capacitance must to consider de-rating.	
L_select	0.2	uH		
DCR_real	0.63	mΩ	Tolerance (±)	20
Current sense signal ratio (τ)	0.5			
R1_cal	90.70	Ω		
R2_cal	90.70	Ω		
R1_select	93.1	Ω	"R1_select" must > "R1_cal"	
R1_select range is ok or not	PASS			
R2_select	93.1	Ω		
R2_select range is ok or not	PASS			
Real current sense signal ratio (τ)	0.5			
Real time constant	1.0264275			
Temperature of L	25.00	℃	Consider DCR variation with temperatur	
DCR with Temperature	0.63	mΩ		
VCC	3.3	V		

OCP Trigger Level (Consider the external component variation)				
Parameter	Min	TYP	Max	Unit
VCC	NA	3.3	NA	V
OCP Trigger Level_set	30.21465202	38	49.70597583	A
ILIM_cal	NA	996.84	NA	mv
OCP error band_cal	-20.48775783	0	30.80519955	%
Roc1_cal	NA	69.79	NA	KΩ
Roc2_cal	NA	30.21	NA	KΩ
Roc1_select	NA	69.8	NA	KΩ
Roc2_select	NA	30.1	NA	KΩ
ILIM_real	NA	994.29	NA	mV
OCP Trigger Level_real	30.15	37.92	49.60	A
OCP error band_real	-20.49	0.00	30.81	%

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MS-7C95

Size	Document Description	Rev
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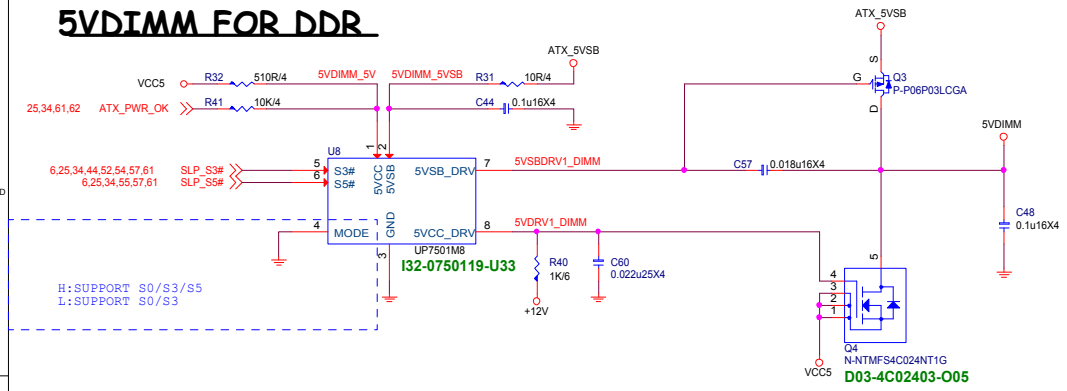
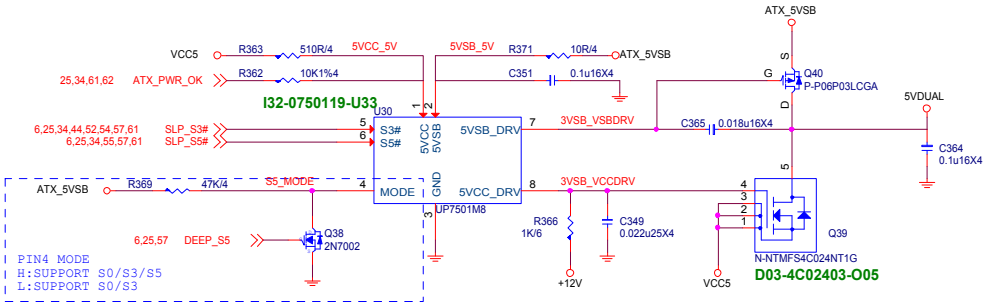
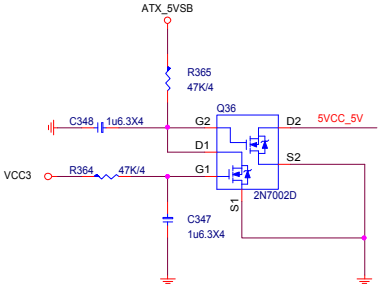
5VDIMM FOR DDR



S0IX

5VDUAL For 3VSB/CPU1.8V/VDDP



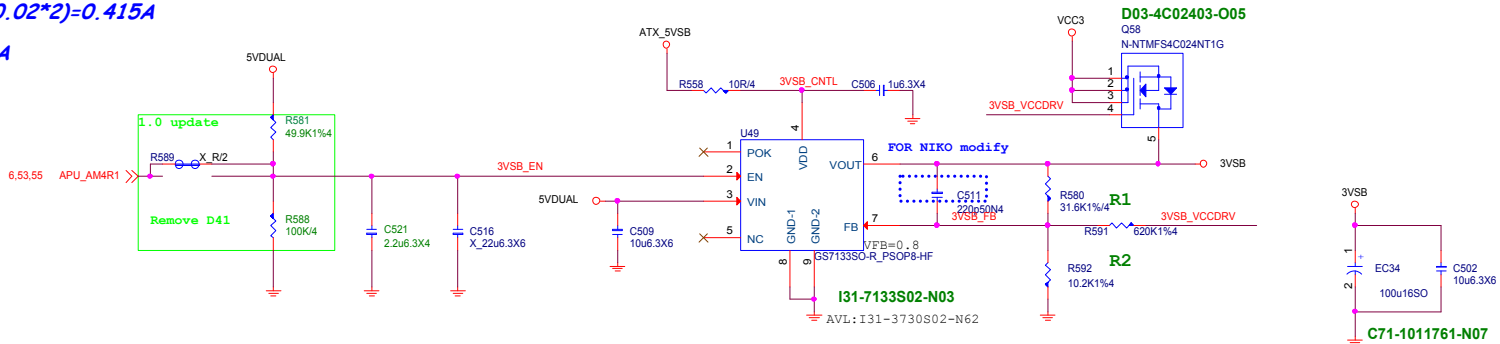


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

3VSB cost down

3.3V@1.61A

CPU:VDD_33_S5=0.25A
CHIP:VDD_33_S5=0.1A
*PCIE=(375mA*1+0.02*2)=0.415A*
M.2WIFI= 0.78A
RTL8111H=0.065A



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(31.6K/10.2K))
= 3.328V

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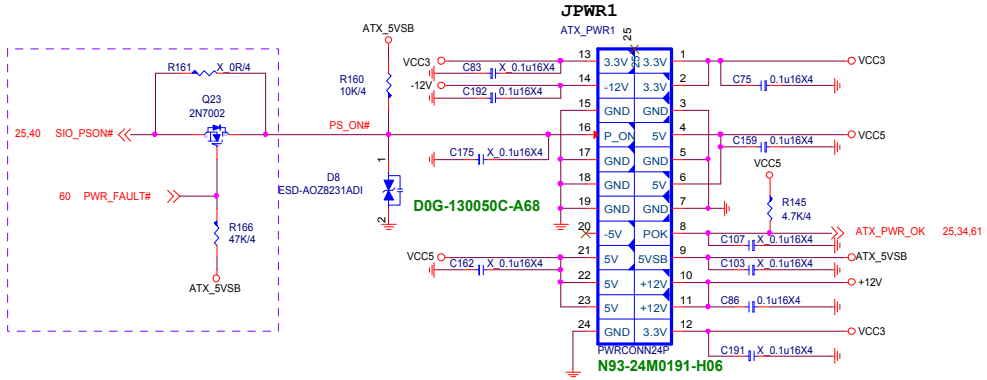
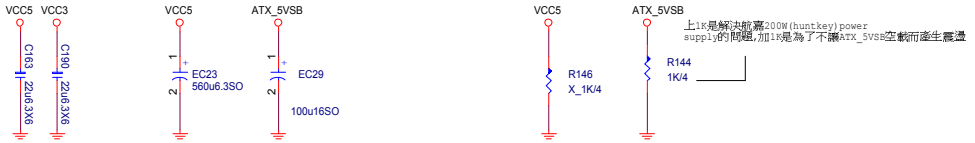
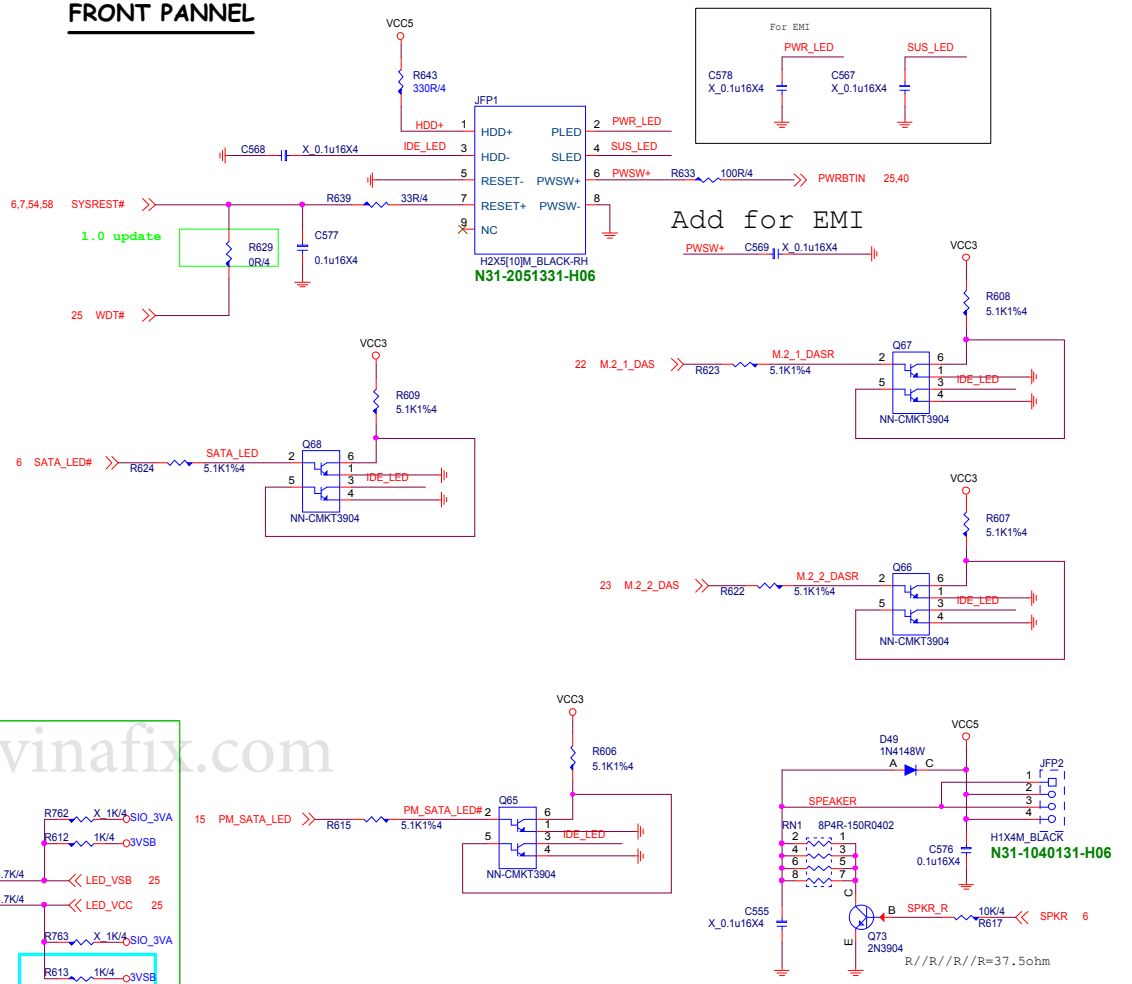
ATX POWER CONNECTOR



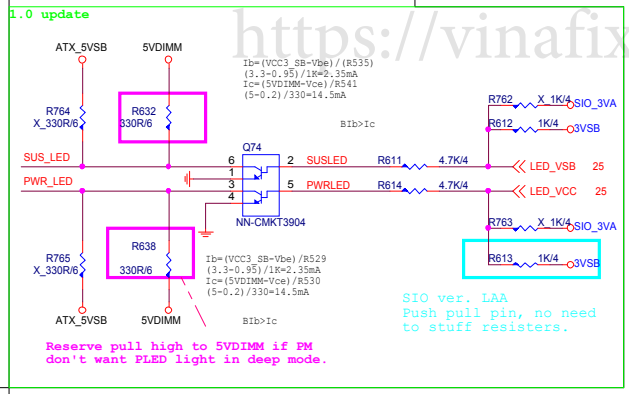


FRONT PANNEL



TPM

LED (for ESIO)



Voltage Mearsure Point

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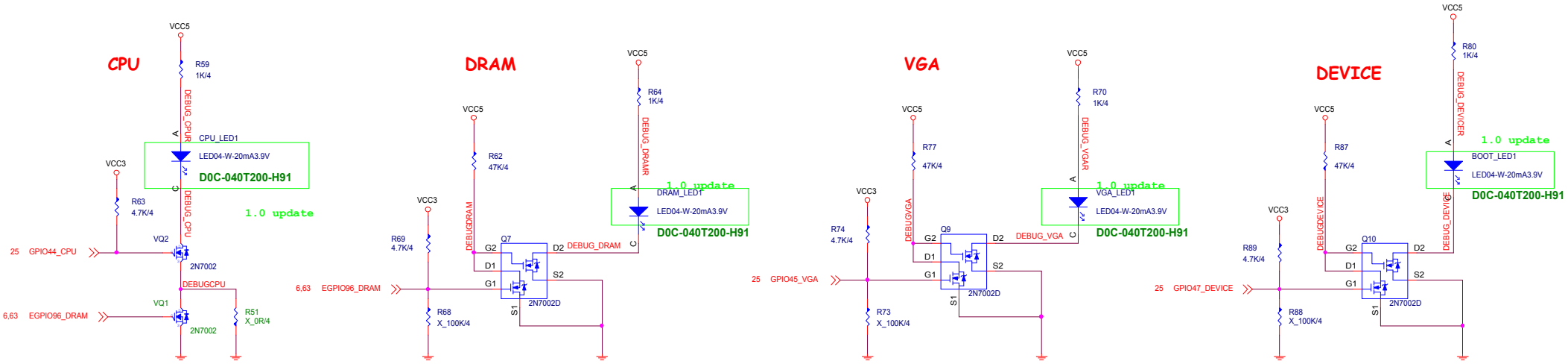
EZ Debug LED



LEDGPIO	GPIO46	EGPIO96	GPIO44	GPIO13
亮	OPEN-Drain	GPO LOW	GPO LOW	GPO LOW
滅	GPO LOW	GPO HIGH	OPEN-Drain	OPEN-Drain

default Input

LED亮燈時同時將CPU LED關掉

DIMM_SLOT FORM SIO

D0C-040P100-H91/D0C-040S500-E07

AMD AMP Detect LED

MICRO-STAR INT'L CO.,LTD

MS-7C95

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Custom	62 LED - EZ DEBUG / AMP	10

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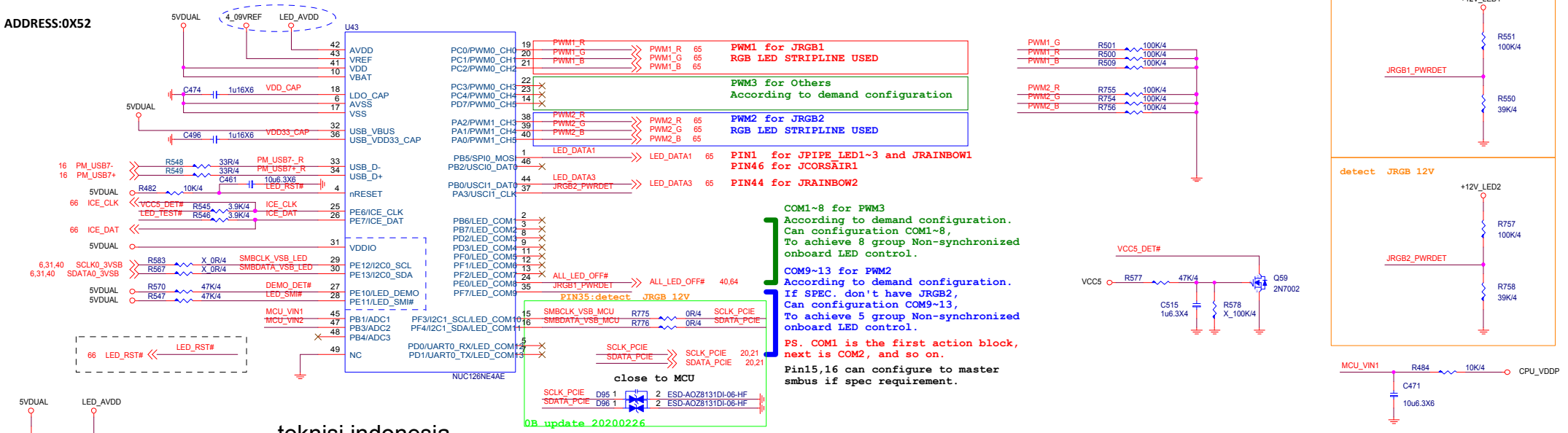
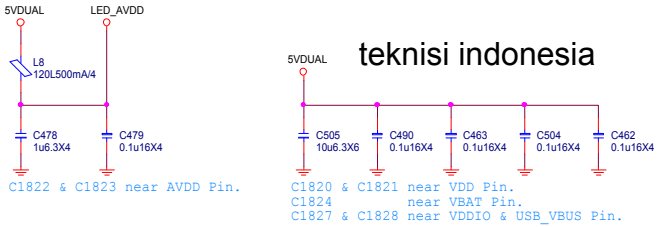
48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.

ADDRESS:0X52

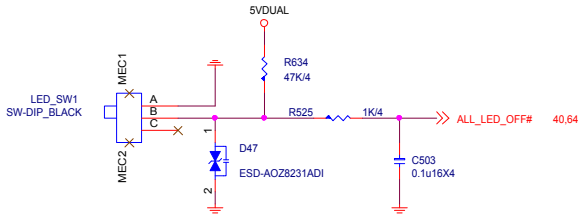


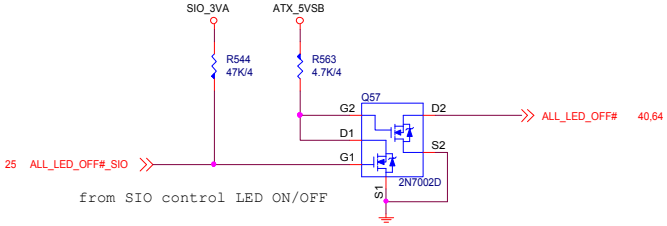


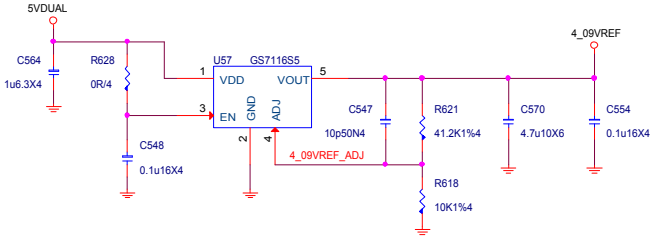
teknisi indonesia

LED_SW1 for ALL LED OFF

B-C: LED ON(default)
B-A: LED OFF







Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~13	PWM2

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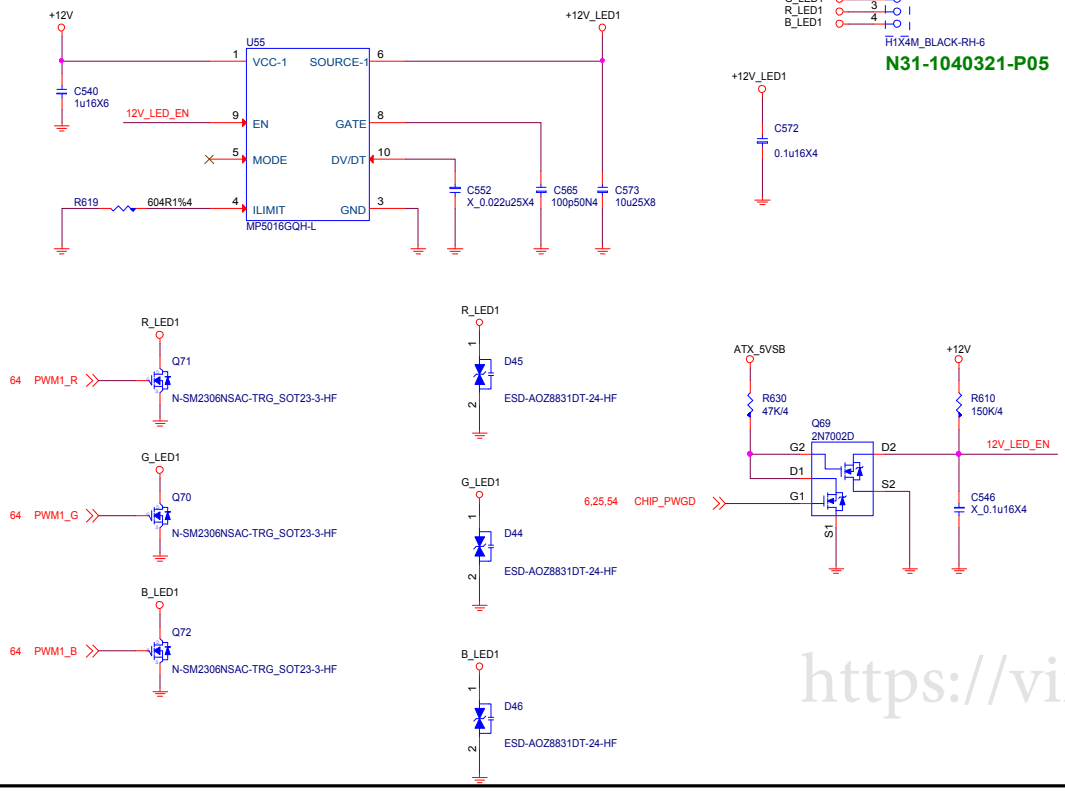
JRGB1

Trip@3.6A

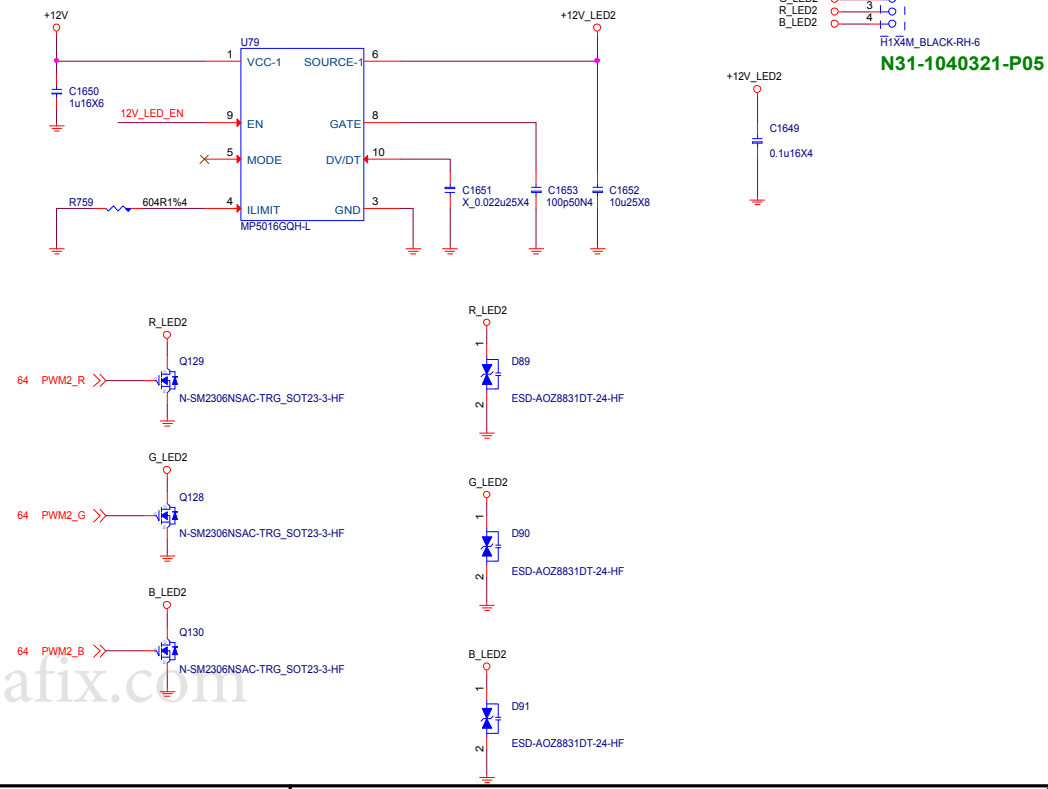
>60mil >60mil



JRGB2

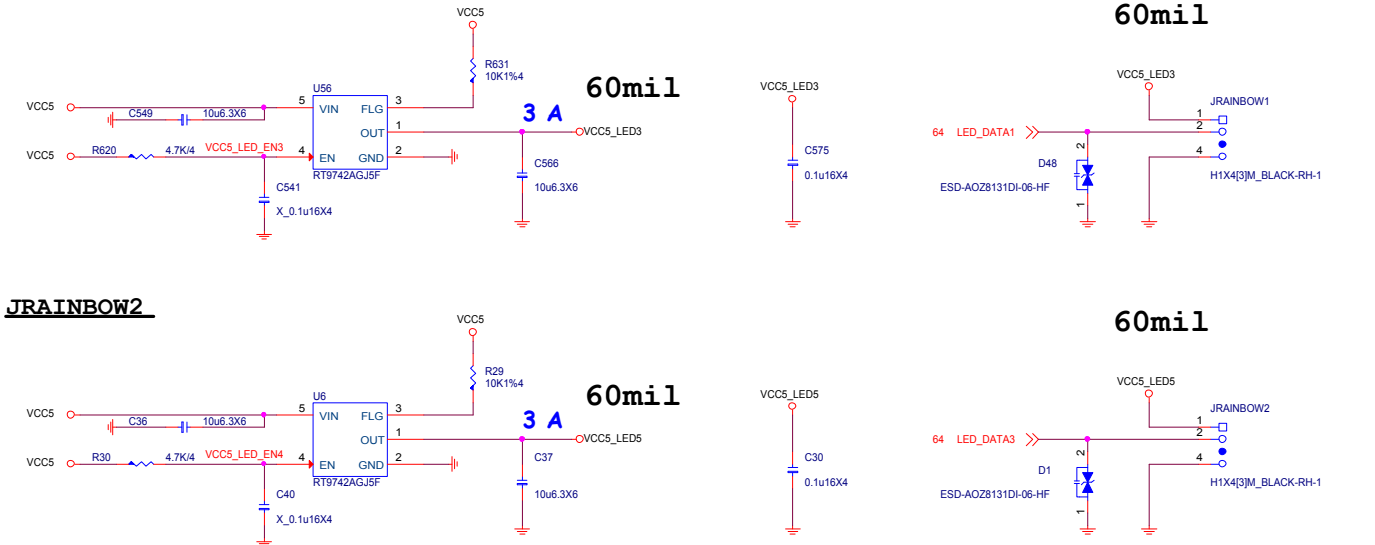
Trip@3.6A

>60mil >60mil



JRAINBOW1

60mil 60mil



JRAINBOW2

60mil 60mil

JCORSAIR1

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C95	
Size: Custom	Document Description: 64 LED - JRGB1/2 JRAINBO1/2	Rev: 10
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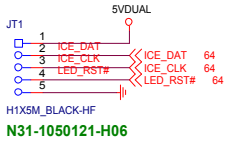
JT1 for FW update



EXTERNAL POWER INPUT

IF no JPWRLED1 & JPIPE_LED spec

MCU can powered by 5VDUAL directly.
LED_VCC5 replace with 5VDUAL.

JF1 for Factory test

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Size: Custom	Document Description: 66 BOM Option
Rev: 10	
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CPU Socket

CPU2

E95-0000022-A91

E95-0000022-A91

Simulation

X_JS2

SIM1

X_PIN1*2

X_JS1

SIM2

X_PIN1*2

FM6 FM8 FM5

X_FM120 X_FM120 X_FM120

FM2 FM1 FM3

X_FM120 X_FM120 X_FM120

FM4 FM7

X_FM120 X_FM120

Optics Orientation Holes

MH1 MH2 MH3

X_MH001 X_MH001 X_MH001

MH5 MH6

X_MH001 X_MH001

MH4 MH8 MH7

X_MH001 X_MH001 X_MH001

C508 0.1u16X4

C481 0.1u16X4

MANUAL PART

UEFI1

G51-M1SPXXA-A09

G51-M1SPXXA-A09

HDMI_LA1

Label

HDMI

HDMI LABEL

Y01-RHDMI03-000

BAT1_X1

BAT-BCR2032P

MARKET1

X_G51-M1SPP79-Q13

G51-M1SPQ02-Q13

WIFI

MARKET2

G51-M1SPP79-Q13

G51-M1SPQ01-Q13

DASH

PCB

PCB

PCB1

7C95_10

2020/03/172020/03/26PD0-07C950B-E48,昱鑫(競華)_蘇州,23,寶安恩斯邁廠(MSIS)4,black
2020/03/172020/03/26PD0-07C950B-G37,精成-深圳,39,寶安恩斯邁廠(MSIS)4,black

PCH HEATSINK

1.0 update

HS_PCH1

MEC1 MEC1

MEC2 MEC2

HS-0410620-RH

MOS HEATSINK

HS_W1

MEC1 MEC1

MEC2 MEC2

HS-0507040-RH

DASH BOM

LAN99

LAN

X_RTL8111HN-CG-RH

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