MU-820RA
MU-820RJ
MU-820RK

QM-800P

CENTRAL MONITOR MAIN UNIT

MU-820R

CNS-8200 SYSTEM

0634-000103F

0634-000103F

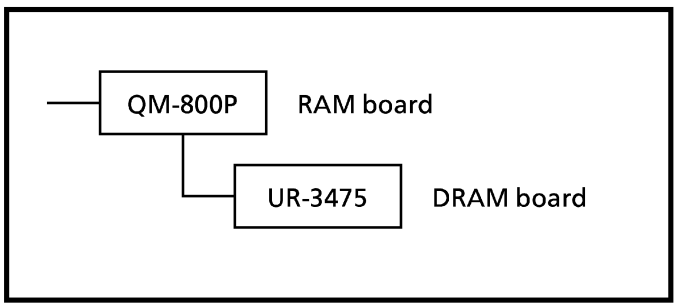
MANUAL CHANGE INFORMATION

April 24,1998

The QM-800P RAM board has been changed beginning with the serial number 1341.

In accordance with the change of the QM-800P RAM board, the composition of the RAM board and information on the following pages in MANUAL CHANGE INFORMATION (0634-000103A) are changed:

Composition of RAM Board



Circuit Descriptions

Old	New
MANUAL CHANGE INFORMATION 0634-000103A	
Section 3.11.1 General (page 7/44) and Section 3.11.2 Block Diagram Explanation (page 8/44)	Replace with page 3/9
Sections 3.11.3 to 3.11.8 (pages 8/44, 9/44, 10/44, 11/44, 12/44 and 13/44)	Delete

Electrical Parts List

Old	New
MANUAL CHANGE INFORMATION 0634-000103A (Pages 20/44 and 21/44)	UR-3475 DRAM Board Replace with pages 4/9 and 5/9

Circuit Diagrams

Old	New
MANUAL CHANGE INFORMATION 0634-000103A (Pages 41/44, 42/44, 43/44 and 44/44)	UR-3475 DRAM 1/4, 2/4, 3/4 and 4/4 Replace with pages 6/9, 7/9, 8/9 and 9/9

Circuit Descriptions

3.11 DRAM Board (QM-800P)

3.11.1 General

Main Function

1) Stores the full disclosure ECG data of up to 60 hours (8 MB), recall waveforms of up to 992 episodes and morphology data for all beds in memory.
2) Backs up the above data for at least 5 minutes after power is off.

3.11.2 Block Diagram Explanation

1) System interface
   The system interface block is an interface to communicate with the main unit. Refer to the UR-3475 DRAM board circuit diagram (1/4) in Section 11.

2) Power source for memory backup
   The power source block for backup detects power off when the XIORST signal from the CPU board is applied or the voltage of the +5 V line on the DRAM board falls to less than 4.25 V. After detecting power off, the power source for memory backup changes from the +5 V line to the backup battery which consists of four capacitors (C224 to C227). Refer to the UR-3475 DRAM board circuit diagram (2/4) in Section 11.

3) DRAM control
   The DRAM control block generates the following control signals:
   - 16 MHz clock signals for reading data from the DRAM
   - 16 MHz clock signals for writing data to the DRAM
   - 455 kHz clock signals for maintaining the data stored in the DRAM (XWEA to XWED, XOEA to XOED, XRAS-0, XRAS-1, XCAS-0 and XCAS-1)

   Refer to the UR-3475 DRAM board circuit diagram (2/4 and 3/4) in Section 11.

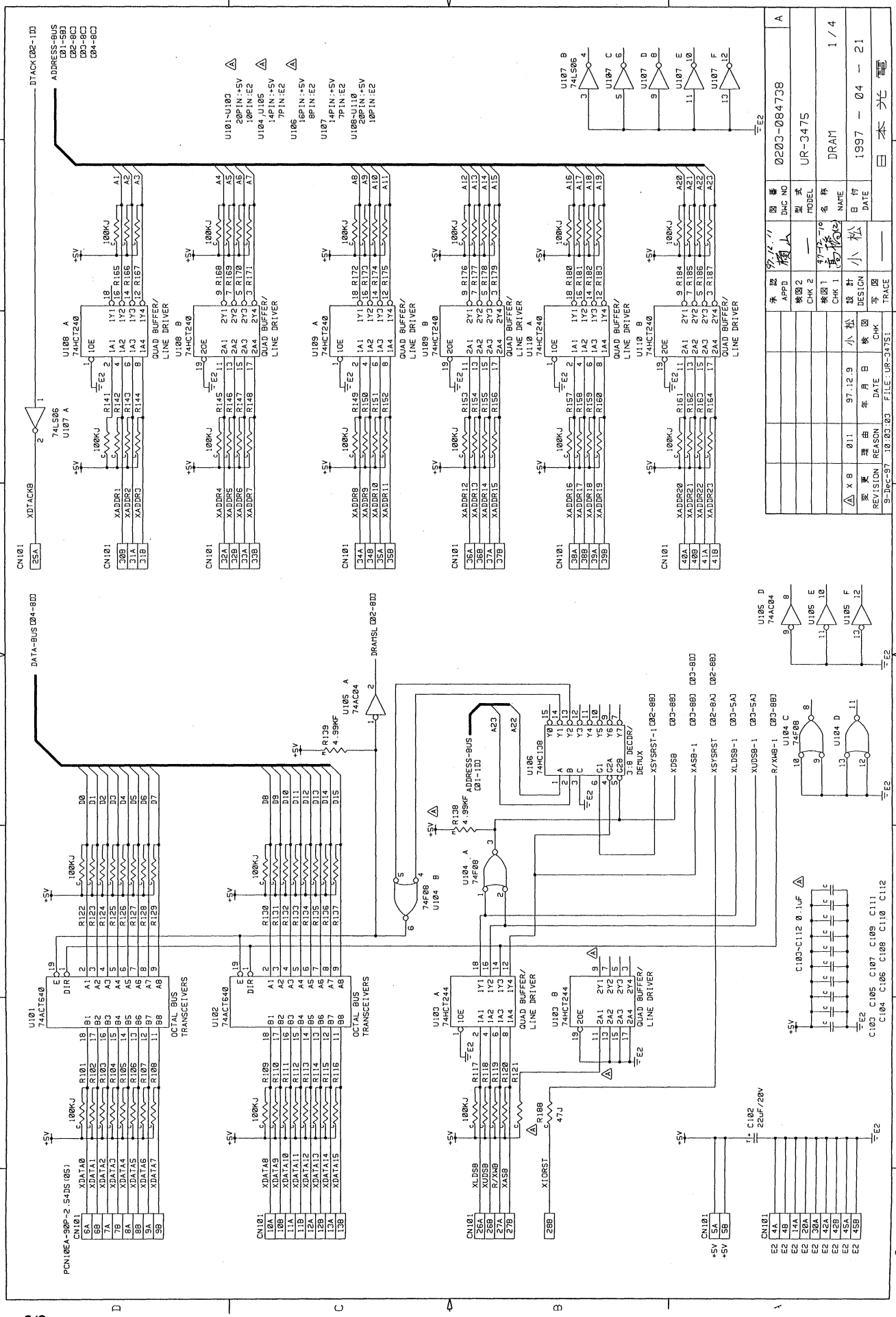
4) DRAM
   The DRAM block consists of four 16 Mbit DRAMs; the total memory capacity is 8 MB. Refer to the UR-3475 DRAM board circuit diagram (4/4) in Section 11.

Electrical Parts List

UR-3475 DRAM Board

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UR-3475	CN101	089957	1	PCN	PCN10EA-90P-2.54DS (05)
UR-3475	C102	159641	1	TAC	267M2002 226MR533 22MF20V
UR-3475	C103-C112	368905	10	CEC	ECU V1H 104ZFX
UR-3475	C201-C202	363411	2	CEC	GRM39SL 101J50PT 50V 100PF
UR-3475	C203	159721A	1	CEC	GRM39SL 220J50PT 22PF 5V
UR-3475	C204	159748A	1	CEC	GRM39SL 470J50PT 47PF 50V
UR-3475	C205-C206	070148	2	EC	ECEA1CU101B 16V 100UF
UR-3475	C207	159641	1	TAC	267M2002 226MR533 22MF20V
UR-3475	C208-C223	368905	16	CEC	ECU V1H 104ZFX
UR-3475	C224-C227	046861	4	C	EECF5R5U105 1F/5.5V
UR-3475	C301-C308	368905	8	CEC	ECU V1H 104ZFX
UR-3475	C309	159721A	1	CEC	GRM39SL 220J50PT 22PF 50V
UR-3475	C401-C415	368905	15	CEC	ECU V1H 104ZFX
UR-3475	D201-D202	160087	2	D	1SS307 TE85R
UR-3475	D203	160096	1	D	1SS294 TE85R
UR-3475	L201	037113	1	COIL	ELE-Y221KA 220μH
UR-3475	Q201	160122	1	TR	2SA1122 CORD TR
UR-3475	Q202	373347	1	FET	2SJ182S-TR
UR-3475	Q203-Q205	160149	3	TR	2SC2618 D TR
UR-3475	Q206	334443	1	TR	2SA1213-Y TE12R
UR-3475	Q207-Q208	160149	3	TR	2SC2618 D TR
UR-3475	R101-R137	159579A	37	MR	RK73K1JTD 100kΩJ 1-16W
UR-3475	R138-R139	158963	2	MR	RN41C2DT3 4.99kΩF 1/5W
UR-3475	R141-R187	159579A	47	MR	RK73K1JTD 100kΩJ 1/16W
UR-3475	R188	161478A	1	MR	RK73K1JTD 47ΩJ 1/16W
UR-3475	R205	159588A	1	MR	RK73K1JTD 1.0MΩJ 1/16W
UR-3475	R206	158963	1	MR	RN41C2DT3 4.99kΩF 1/5W
UR-3475	R207-R212	159579A	6	MR	RK73K1JTD 100kΩJ 1/16W
UR-3475	R213-R214	159561A	2	MR	RK73K1JTD 47kΩJ 1/16W
UR-3475	R215-R216	159552A	2	MR	RK73K1JTD 10kΩJ 1/16W
UR-3475	R217	159534A	1	MR	RK73K1JTD 1.0kΩJ 1/16W
UR-3475	R218	159579A	1	MR	RK73K1JTD 100kΩJ 1/16W
UR-3475	R219	159561A	1	MR	RK73K1JTD 47kΩJ 1/16W
UR-3475	R220	159552A	1	MR	RK73k1JTD 10kΩJ 1/16W
UR-3475	R221	159534A	1	MR	RK73K1JTD 1.0kΩJ 1/16W
UR-3475	R222	159579A	1	MR	RK73K1JTD 100kΩJ 1/16W
UR-3475	R223	159552A	1	MR	RK73K1JTD 10kΩJ 1/16W
UR-3475	R224	159151	1	MR	RN41C2DT3 33.2kΩF 1/5W
UR-3475	R225	159213	1	MR	RN41C2DT3 49.9kΩF 1/5W
UR-3475	R226-R227	159552A	2	MR	RK73K1JTD 10kΩJ 1/16W
UR-3475	R228	159285	1	MR	RN41C2DT3 100kΩF 1/5W
UR-3475	R229	159151	1	MR	RN41C2DT3 33.2kΩF 1/5W
UR-3475	R230	158963	1	MR	RN41C2DT3 4.99kΩF 1/5W
UR-3475	R231	158874	1	MR	RN41C2DT3 2.00kΩF 1/5W
UR-3475	R232	159552A	2	MR	RK73K1JTD 10kΩJ 1/16W
UR-3475	R233	158963	1	MR	RN41C2DT3 4.99kΩF 1/5W
UR-3475	R234	159507	1	MR	RN41C2DT3 499ΩF 1/5W
UR-3475	R235-R236	161478A	2	MR	RK73K1JTD 47ΩJ 1/16W
UR-3475	R237-R240	158776	4	MR	RN41C2DT3 200ΩF 1/5W

UR-3475	R301	158963	1	MR	RN41C2DT3 4.99kΩF 1/5W
UR-3475	R302-R304	161478A	3	MR	RK73K1JTD 47ΩJ 1/16W
UR-3475	R401-R424	161478A	24	MR	RK73K1JTD 47ΩJ 1/16W
UR-3475	R425-R436	159579A	12	MR	RK73K1JTD 100kΩJ 1/16W
UR-3475	U101-U102	520091	2	CMOS	TC74ACT640F 1668
UR-3475	U103	161647	1	CMOS	HD74HCT244FP
UR-3475	U104	161406	1	TTL	74F08SJ
UR-3475	U105	333836	1	CMOS	74AC04SJ NS
UR-3475	U106	161023	1	CMOS	HD74HC138FP
UR-3475	U107	161469	1	TTL	SN74LS06 NS
UR-3475	U108-U110	161415	3	CMOS	HD74HCT240FP
UR-3475	U201	160612	1	CMOS	MC14069UBF
UR-3475	U202-U203	160978	2	CMOS	HD74HC74FP
UR-3475	U204	160889	1	CMOS	HD74HCO8FP
UR-3475	U205	400844	1	CPU	M51945BL
UR-3475	U206	323027	1	CMOS	HD74HC123AFP
UR-3475	U207	400817	1	REG	MAX631ACPA
UR-3475	U208	160898	1	CMOS	HD74HC10FP
UR-3475	U209	365204	1	CMOS	74AC00SJ
UR-3475	U210	333863	1	CMOS	74AC08SJ NS
UR-3475	U211	400835	1	CPU	M51943BL
UR-3475	U212-U214	149901A	2	CMOS	74AC74SJ (CD74AC74M) (SOP)
UR-3475	U215	160898	1	CMOS	HD74HC10FP
UR-3475	U216	333863	1	CMOS	74AC08SJ NS
UR-3475	U301	161398	1	TTL	74F74SJ
UR-3475	U302	161095	1	CMOS	HD74HC164FP
UR-3475	U303	161023	1	CMOS	HD74HC138FP
UR-3475	U304-U305	160951	1	CMOS	HD74HC32FP
UR-3475	U306	333827	1	CMOS	74AC32SJ NS
UR-3475	U307	333863	1	CMOS	74AC08SJ NS
UR-3475	U401-U403	161068	3	CMOS	HD74HC157FP
UR-3475	U404-U408	536653	4	RAM	HM5116160J-7 2073
UR-3475	X201	400826	1	XTAL	CSB455J
UR-3475	X301	500941	1	XTAL	HAT8700A 32MHz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ADDRESS-BUS (D1-5D) (D2-8C) (D3-8C) (D4-8C)
DATA-BUS D4-8D
DRAMSL D2-8D
U101 74ACT640 OCTAL BUS TRANSCEIVERS
U102 74ACT640 OCTAL BUS TRANSCEIVERS
U103 A 74HCT244 QUAD BUFFER/ LINE DRIVER
U103 B 74HCT244 QUAD BUFFER/ LINE DRIVER
U104 A 74F08
U104 B 74F08
U104 C 74F08
U104 D 74F08
U105 A 74AC04
U105 D 74AC04
U106 74HC138 3:8 DECDR/ DEMUX
U107 A 74LS06
U107 B 74LS06
U108 A 74HCT240 QUAD BUFFER/ LINE DRIVER
U108 B 74HCT240 QUAD BUFFER/ LINE DRIVER
U109 A 74HCT240 QUAD BUFFER/ LINE DRIVER
U109 B 74HCT240 QUAD BUFFER/ LINE DRIVER
U110 A 74HCT240 QUAD BUFFER/ LINE DRIVER
U110 B 74HCT240 QUAD BUFFER/ LINE DRIVER
U101~U103 20PIN:+5V 10PIN:E2
U104,U105 14PIN:+5V 7PIN:E2
U106 16PIN:+5V 8PIN:E2
U107 14PIN:+5V 7PIN:E2
U108~U110 20PIN:+5V 10PIN:E2
PCN10EA-90P-2.54DS(05)
C102 22uF/20V
C103~C112 0.1uF
R139 4.99KF
R138 4.99KF
R188 47J
XDSB
XASB-1
XSYSRST
XLDSB-1
XUDSB-1
R/XWB-1
XSYSRST-1
XIORST
XDTACKB
XDATA0 XDATA1 XDATA2 XDATA3 XDATA4 XDATA5 XDATA6 XDATA7
XDATA8 XDATA9 XDATA10 XDATA11 XDATA12 XDATA13 XDATA14 XDATA15
XADDR1 XADDR2 XADDR3 XADDR4 XADDR5 XADDR6 XADDR7
XADDR8 XADDR9 XADDR10 XADDR11 XADDR12 XADDR13 XADDR14 XADDR15
XADDR16 XADDR17 XADDR18 XADDR19 XADDR20 XADDR21 XADDR22 XADDR23
承認 APPD 97.12.11 欄山
検図2 CHK 2
検図1 CHK 1 97.12.10 小松
設計 DESIGN 小松
検図 CHK
写図 TRACE
図番 DWG NO 0203-084738
型式 MODEL UR-3475
名称 NAME DRAM 1/4
日付 DATE 1997 - 04 - 21
日本光電
REVISION X 8 011 97.12.9 変更理由 REASON DATE
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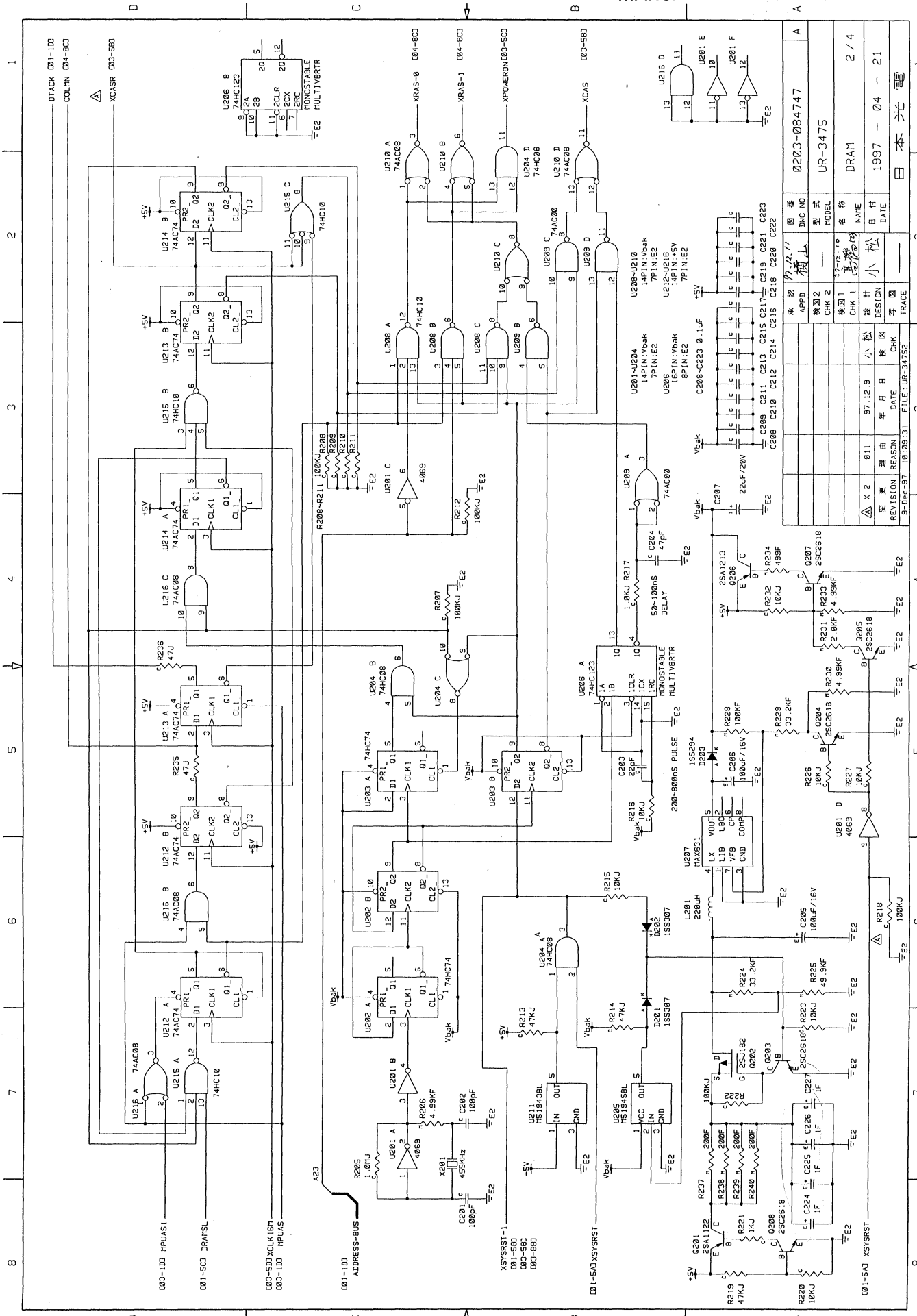

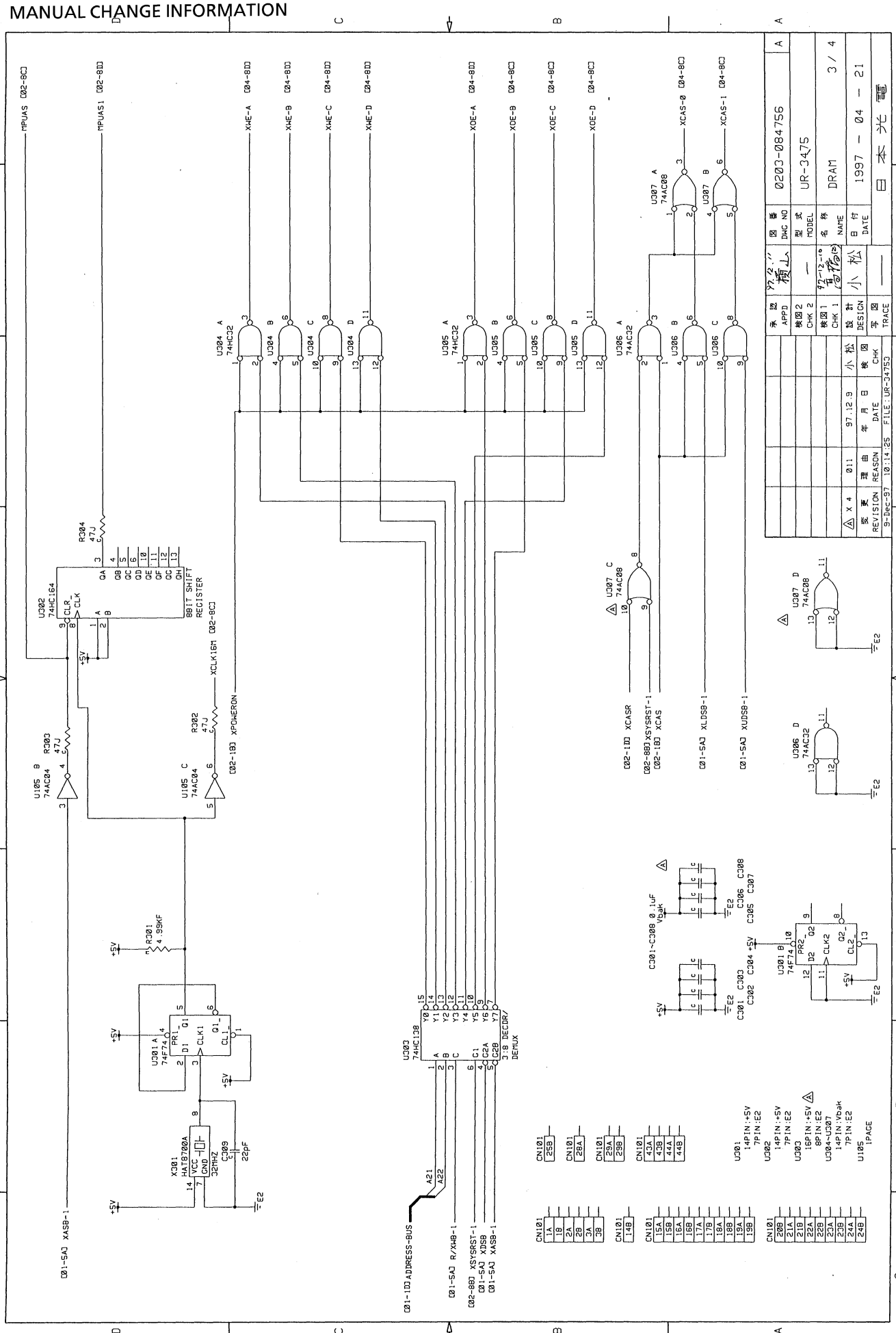
MPUAS [02-8C]
MPUAS1 [02-8D]
XHE-A [04-8D]
XHE-B [04-8D]
XHE-C [04-8D]
XHE-D [04-8D]
XOE-A [04-8D]
XOE-B [04-8C]
XOE-C [04-8C]
XOE-D [04-8C]
XCAS-0 [04-8C]
XCAS-1 [04-8C]
U304 74HC32
U305 74HC32
U306 74AC32
U307 74AC08
U302 74HC164
8BIT SHIFT REGISTER
R304 47J
R303 47J
R302 47J
R301 4.99KF
U105 74AC04
XCLK16M [02-8C]
[02-10] XPOWERON
U301 74F74
X301 HAT8700A 32MHZ
C309 22pF
U303 74HC138
3-8 DECDR/ DEMUX
[01-1D] ADDRESS-BUS
[01-5A] XASB-1
[01-5A] R/XWB-1
[02-8D] XSYSRST-1
[01-5A] XDSB
[02-1D] XCASR
[02-8B] XSYSRST-1
[02-1B] XCAS
[01-5A] XLDSB-1
[01-5A] XUDSB-1
C301~C308 0.1uF
C301 C302 C303 C304 C305 C306 C307 C308
U301 74F74
CN101
U301 14PIN +5V 7PIN E2
U302 14PIN +5V 7PIN E2
U303 16PIN +5V 8PIN E2
U304~U307 14PIN Vbak 7PIN E2
U105 1PAGE
承認 APP'D
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
小松
97.12.9
図番 DWG NO
0203-084756
型式 MODEL
UR-3475
名称 NAME
DRAM
3 / 4
日付 DATE
1997 - 04 - 21
REVISION
変更 理由 REASON
年月日 DATE
検図 CHK
X 4
011
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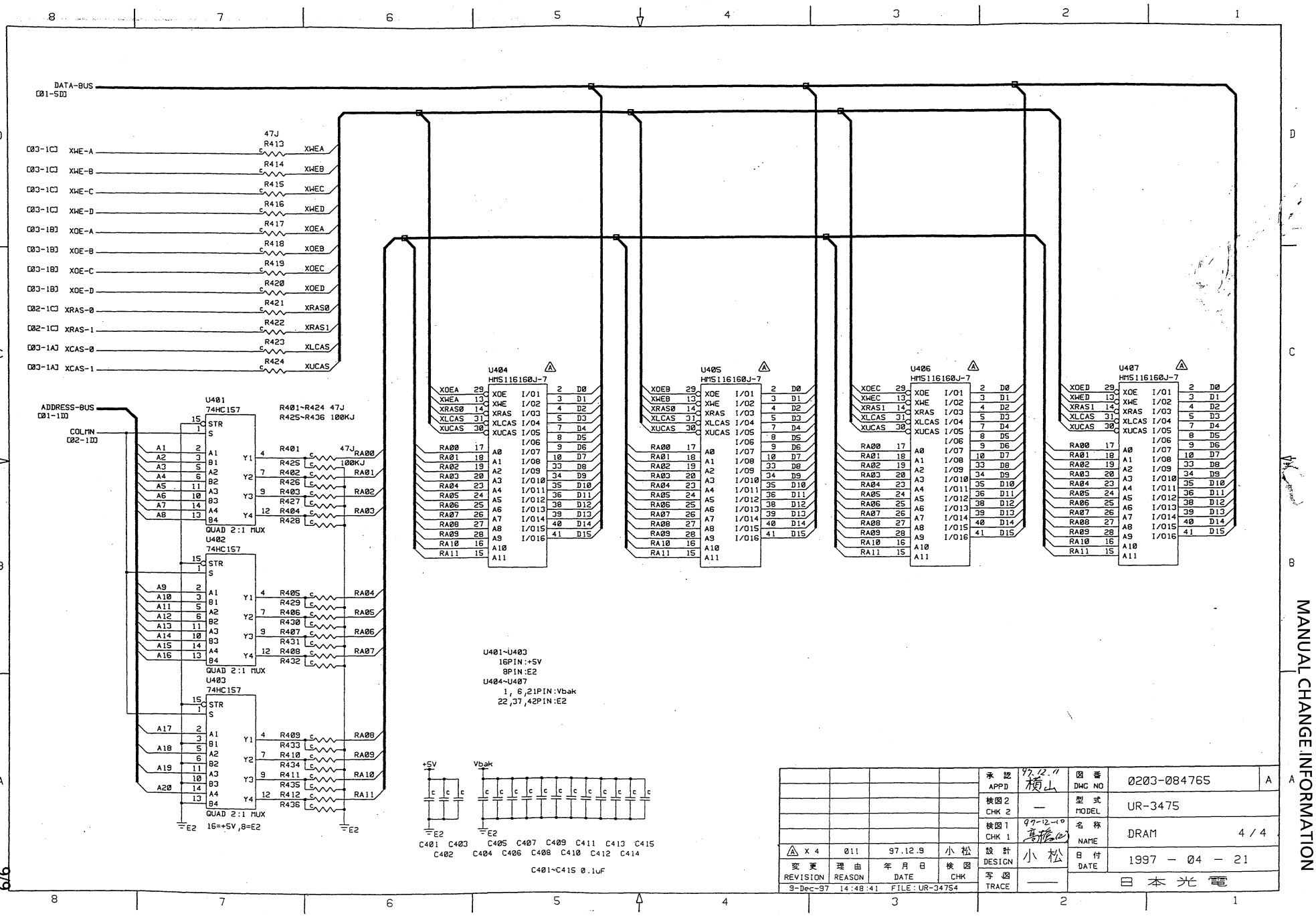
FILE: UR-3475J
日本光電



A X 4	011	97.12.9	小松	
変更 REVISION	理由 REASON	年月日 DATE	検図 CHK	
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承認 APPD	97.12.11 横山	図番 DWG NO	0203-084765 A
検図2 CHK 2	—	型式 MODEL	UR-3475
検図1 CHK 1	97-12-10 高橋(仁)	名称 NAME	DRAM 4/4
設計 DESIGN	小松	日付 DATE	1997 − 04 − 21
写図 TRACE	——	日本光電	

MANUAL CHANGE INFORMATION

0634-000103E

MANUAL CHANGE INFORMATION

Unit	Main unit
CRT Unit VM-003P Main board UP-03731 CRT board UP-0372	MU-820RA
	MU-820RJ
	MU-820RK

CRT Unit: Video controller is changed.

Section 3 Circuit Descriptions

Page	From	To
3-25	(Replace the whole page.)	Page 2/4
3-26	(Replace the whole page.)	Page 3/4

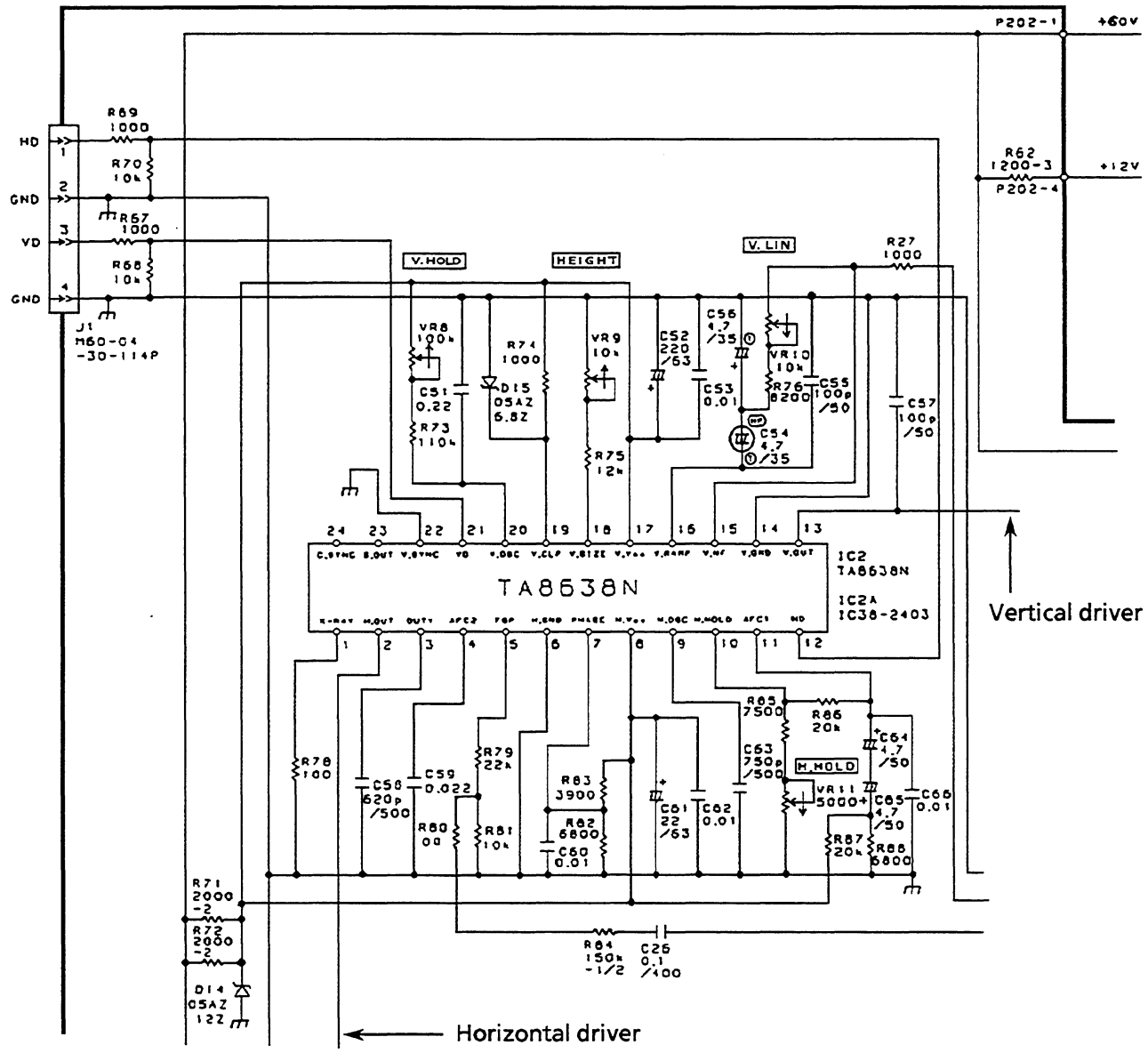
Section 11 Electrical Parts List

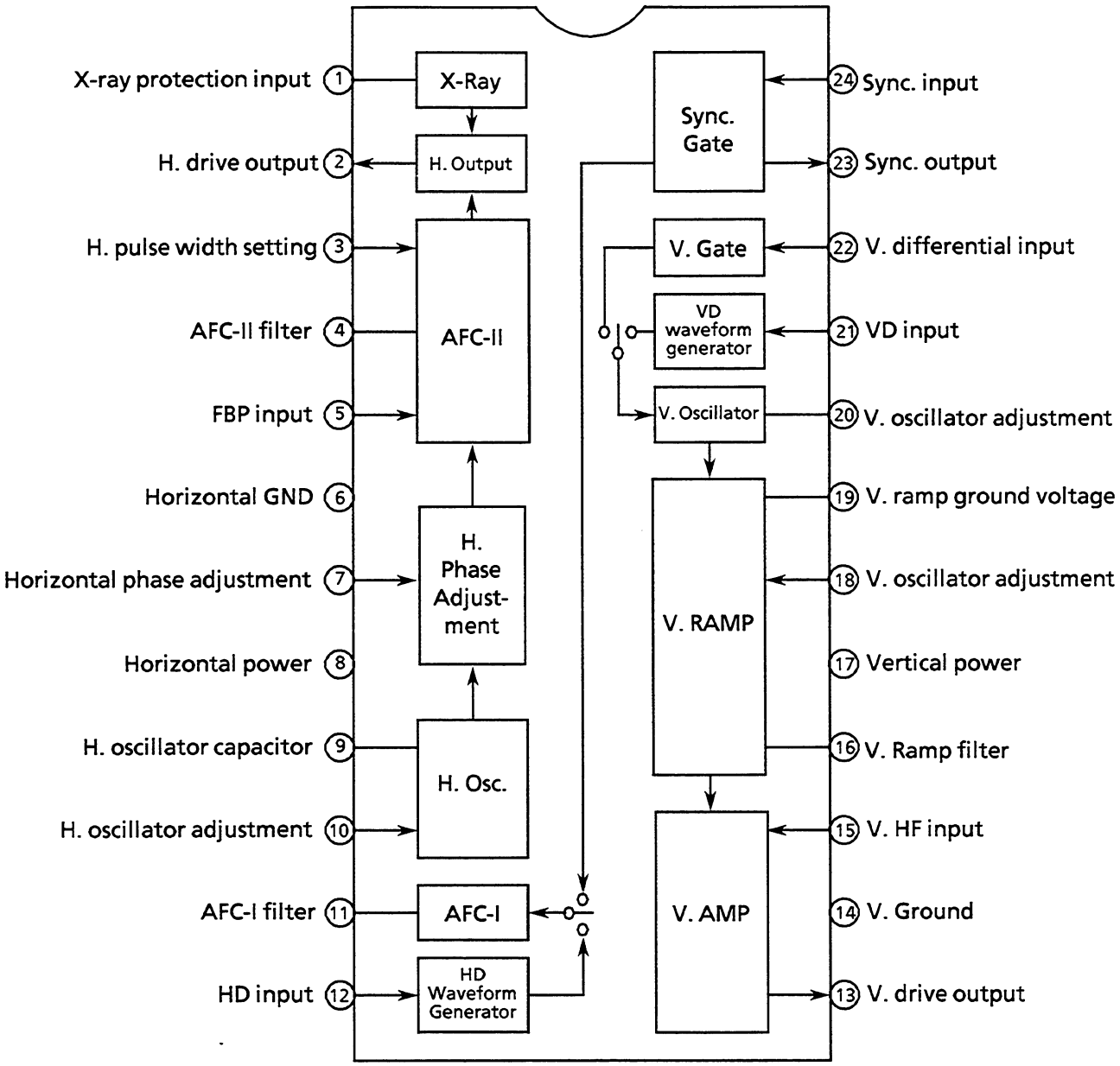
Page	From	To
11-22 to 11-24	(CRT MAIN PWB board UP-0372 and UP-03731)	(Deleted)

Section 13 Circuit Diagram

Page	From	To
13-35	(Replace the whole page.)	Page 4/4

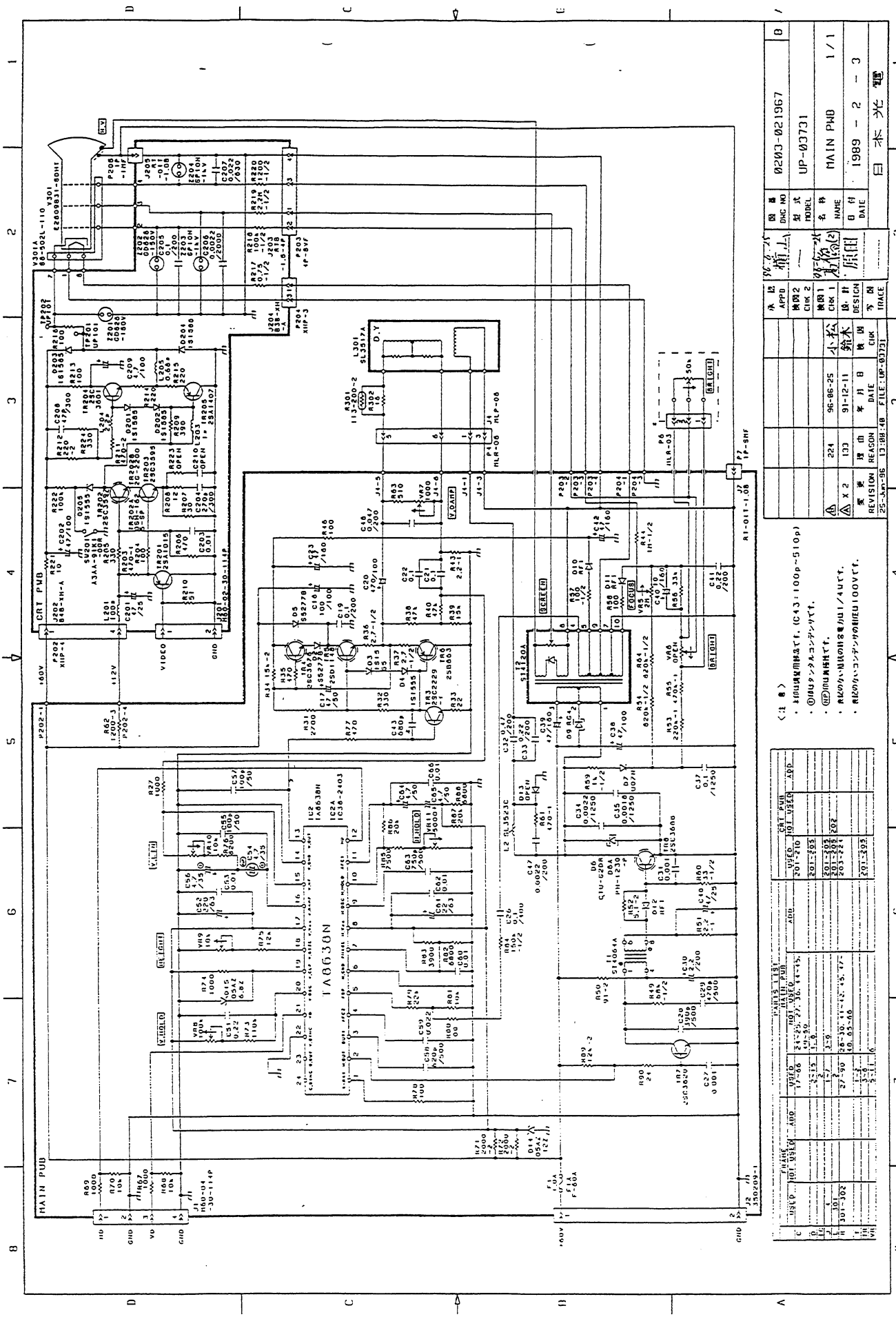
3.3.3 CRT Signal Processing Circuit





1. Vertical Oscillating Circuit
   This circuit is controlled by IC2. Adjust VR8 (V. HOLD) if the screen continuously scrolls along the X-axis. Adjust VR9 (HEIGHT) if the screen size along the X-axis is not correct. Adjust VR10 (V. LIN) to compensate the linearity along the vertical axis.

2. Horizontal Oscillating Circuit
   This circuit is also controlled by IC2 through its AFC port. Adjust VR11 (H. HOLD) if the screen continuously scrolls along the Y-axis.


MAIN PWB
CRT PWB
IA86308
0203-021967
UP-03731
MAIN PWB
1 / 1
1989 - 2 - 3
日本光電

0634-000103C

MANUAL CHANGE INFORMATION

Unit	Main unit	Starting serial No.	Revision (software)	Revision (Hardware)
CRT Unit VM-003P Main board UP-03731 CRT board UP-0372	MU-820RA	00384	B1-02	E2
	MU-820RJ	00045	B1-02	C1
	MU-820RK	00126	B1-02	D2

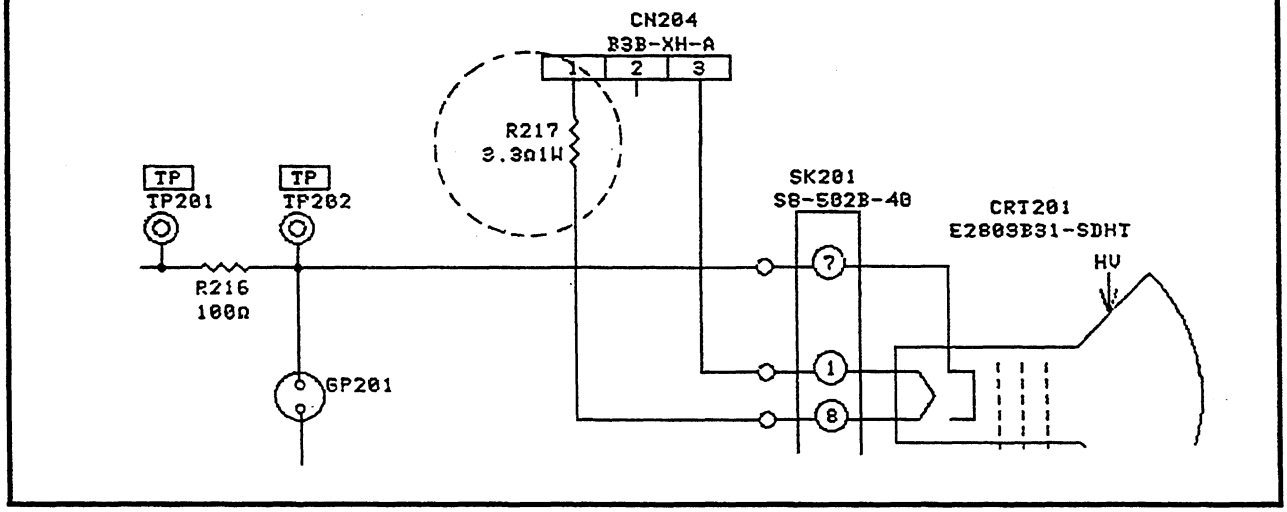
CRT unit: The CRT unit's HSYNC frequency is changed from 64kHz to 62.5kHz.

Section 11 Electrical parts list (Page 11-23)

Unit	Changes	Ckt. No.	Part No.	Description
Main PWB UP-03731	From	C021	7401152	AWS-100V-683J
	To	C021	144657	AWS-100V-104J
	From	C035	7401972	DTB152K1250V
	To	C035	359194	DTB182K1250V

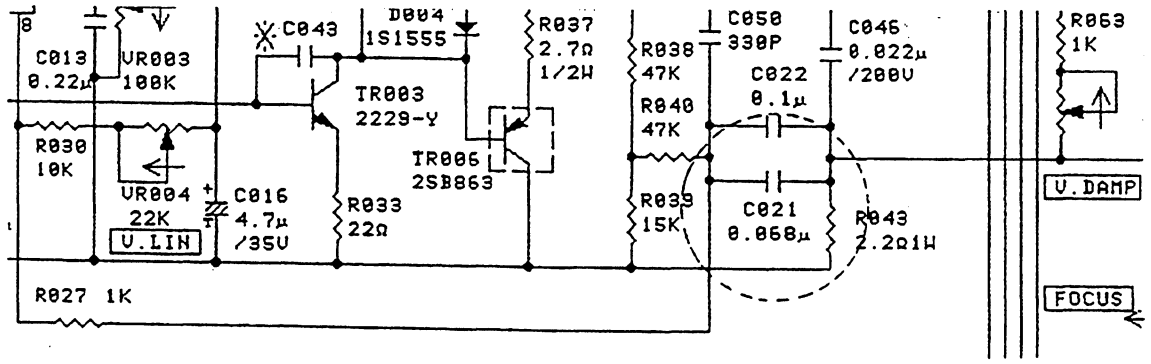
Section 13 Circuit diagram (Page 13-36)

From	To
DWG No.105600C	DWG No. 0203-018926A
3.3Ω1W	0.75Ω1/2W

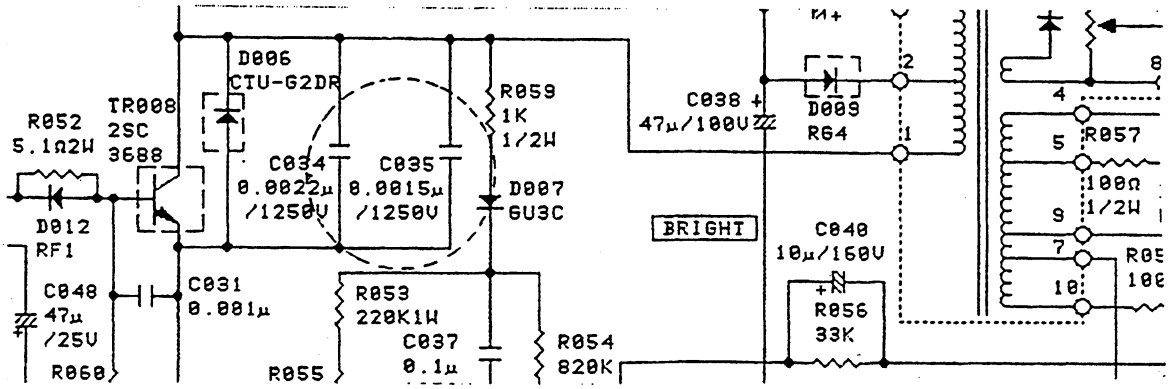


(Page 13-35)

From	To
DWG No.106259	DWG No. 0203-021967A
0.068μF	0.1μF



0.0015μF	0.0018μF



COMPATIBILITY

The software for CRT unit is upgraded to accomodate the changes in the hardware.

CRT unit VM-003P Serial No.	Software revision	
	Previous	B1-02*1, A5-04*2 or later
Previous	Yes	Yes
5793 or later	No*3	Yes

*1: B1-02 is used for CPU board UP-0668(16MHz system clock.)

*2: A5-04 is used for CPU board UP-02602(8MHz system clock.)

*3: Whole screen cannot be displayed.

0634-000103B

MANUAL CHANGE INFORMATION

Unit	Main unit	Starting Serial No.	Revision (Hardware)
Transformer unit SC-017RA Regulator UP-06541	MU-820RA	00379	
Transformer unit SC-017RJ Regulator UP-06541	MU-820RJ	00045	
Transformer unit SC-017RK Regulator UP-06542	MU-820RK		

Content (Page C-2, C-5)
Section 1 Introduction (Page 1-11, 1-12, 1-13, 1-19, 1-20)
Section 3 Circuit Description (page 3-79)
Section 10 Mechanical part list (10-3)
Section 13 Circuit diagram (page 13-3, 13-4)

From	To
SC-001RA/RJ/RK	SC-017RA/RJ/RK
UP-0315	UP-06541 (SC-017RA/RJ) UP-06542 (SC-017RK)

Section 11 Electrical parts list

From	To
Page 11-7, 11-8, 11-20, 11-21	Page 3/12 to 7/12

Section 12 Part location guide

From	To
Page 12-12	Page 8/12

Section 13 Circuit Diagrams

From page	To page
13-84	9/12
13-85	10/12
13-86	11/12
13-87	12/12

COMPATIBILITY

The same unit is also used in the other instruments. Compatibility between the power supply blocks and main instruments is shown below.

	UP-0315 (C117: 2200μF) SC-001RA/RJ/RK	UP-0315 (C117: 4700μF) SC-001RA/RJ/RK	UP-0654 SC-013RA/RJ/RK	UP-06541/06542 SC-017RA/RJ/RK
MU-820RA/RJ/RK	No	Yes	Yes	Yes
JJ-810/820RA/RJ/RK	No	Yes	Yes	Yes
MU-800RA/RJ/RK	Yes	Yes	Yes	Yes
MU-802RA/RJ/RK	No	No	Yes	Yes
MU-841RA MU-843RA/RJ/RK	No	No	Yes	Yes

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
SC-017RA TRANSFORMER UNIT				
SC-017RA	CN001	5415337	8	NCN Receptacle 170458-1
SC-017RA	CN001	5415373	1	NCN Housing 172024-1
SC-017RA	F001	5620062	1	FUSE SAU-4A
SC-017RA	F001	5625396	1	FH FEU 031.1681 Body
SC-017RA	F001	5625404	1	FH FEK 031.1661 Cap
SC-017RA	F002	5620062	1	FUSE SAU-4A
SC-017RA	F002	5625396	1	FH FEU 031.1681 Body
SC-017RA	F002	5625404	1	FH FEK 031.1661 Cap
SC-017RA	LF001	1706022	1	TH SUP-E3G-E-2 Line filter
SC-017RA	SW001	3250367	1	SW JPZ2120-0101
SC-017RA	T001	317462	1	PT T-3715409 117V MU-820RA
SC-017RJ TRANSFORMER UNIT				
SC-017RJ	CN001	5415337	8	NCN Receptacle 170458-1
SC-017RJ	CN001	5415373	1	NCN Housing 172024-1
SC-017RJ	F001	5620062	1	FUSE SAU-4A
SC-017RJ	F001	5625396	1	FH FEU 031.1681 Body
SC-017RJ	F001	5625404	1	FH FEK 031.1661 Cap
SC-017RJ	F002	5620062	1	FUSE SAU-4A
SC-017RJ	F002	5625396	1	FH FEU 031.1681 Body
SC-017RJ	F002	5625404	1	FH FEK 031.1661 Cap
SC-017RJ	LF001	1706022	1	TH SUP-E3G-E-2 Line filter
SC-017RJ	SW001	3250367	1	SW JPZ2120-0101
SC-017RJ	TB001	5611972	1	TERM ULC-505-3P-C
SC-017RJ	T001	342737	1	PT T-3715436 100V MU-820RJ
SC-017RK TRANSFORMER UNIT				
SC-017RK	CN001	5415337	8	NCN Receptacle 170458-1
SC-017RK	CN001	5415373	1	NCN Housing 172024-1
SC-017RK	F001	5621079	1	FUSE 179 120-2A
SC-017RK	F001	5625396	1	FH FEU 031.1681 Body
SC-017RK	F001	5625413	1	FH FEK 031.1663 Cap
SC-017RK	F002	5621079	1	FUSE 179 120-2A
SC-017RK	F002	5625396	1	FH FEU 031.1681 Body
SC-017RK	F002	5625413	1	FH FEK 031.1663 Cap
SC-017RK	LF001	1706022	1	TH SUP-E3G-E-2 Line filter
SC-017RK	SW001	3250367	1	SW JPZ2120-0101
SC-017RK	TB001	5611972	1	TERM ULC-505-3P-C
SC-017RK	T001	342728	1	PT T-3715427 200V MU-820RK

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-06541 REGULATOR UNIT					
UP-06541	CNJ001	5413981	1	NCN	172038-1 11P
UP-06541	CNJ002	5415239	1	NCN	171363-1 17pin MALE
UP-06541	CNJ003	5428225	1	PCN	M60-02-30-114P
UP-06541	CNJ004	5424755	1	PCN	HNC2-2.5P-2DS 2P
UP-06541	CNP004	5424621	1	NCN	Contact HNC-2.5S-D-A
UP-06541	CNP004	5424657	1	PCN	Housing HNC2-2.5S-2 2P
UP-06541	C001	7415244	1		ECOS2CA821BA
UP-06541	C002	7415271	1		ECEA1HGE010
UP-06541	C003	3839757	1	FLC1	ECQ-V1H104JZ 0.1uF
UP-06541	C004	3839525	1	FLC1	ECQ-B1H102JZ 0.001uF
UP-06541	C005	7415262	1		ECEA2AGE220
UP-06541	C006	7415378	1		ECOS1VA822BA
UP-06541	C007	7415271	1		ECEA1HGE010
UP-06541	C008	3839525	1	FLC1	ECQ-B1H102JZ 0.001uF
UP-06541	C009	7415298	1		ECEA1EGE332
UP-06541	C010	7415315	1		ECEA1EGE102
UP-06541	C011-C012	7415289	2		ECEA1VGE330
UP-06541	C013	7415378	1		ECOS1VA822BA
UP-06541	C014	7415306	1		ECEA1VGE102
UP-06541	C015	7415369	1		ECOS1EA822BA
UP-06541	C016	7415289	1		ECEA1VGE330
UP-06541	C017	7415369	1		ECOS1EA822BA
UP-06541	C018	7415289	1		ECEA1VGE330
UP-06541	C019	3820795	1	FLC1	ECQ-B1H 103JZ 0.01uF
UP-06541	D001	7415476	1		D3SB40
UP-06541	D002	1090089	1	ZD3	HZ12LA2 Orange
UP-06541	D003-D004	7400198	2		V06E
UP-06541	D005	7415467	1		D5SB20
UP-06541	D006	7400126	1		HZ6LB2
UP-06541	D007	0910561	1	DP	S10SC4M 10A40V
UP-06541	D008-D009	7415467	2	D	D5SB20
UP-06541	D010-D011	003649	2	D	1SS81
UP-06541	D012	7400135	1	D	HZ6LA2
UP-06541	F001-F006	273838	6	FUSE	HOLDER FP213
UP-06541	F001	341216	1	FUSE	239002
UP-06541	F002	346199	1	FUSE	23901.6
UP-06541	F003-F007	346207	5	FUSE	23902.5

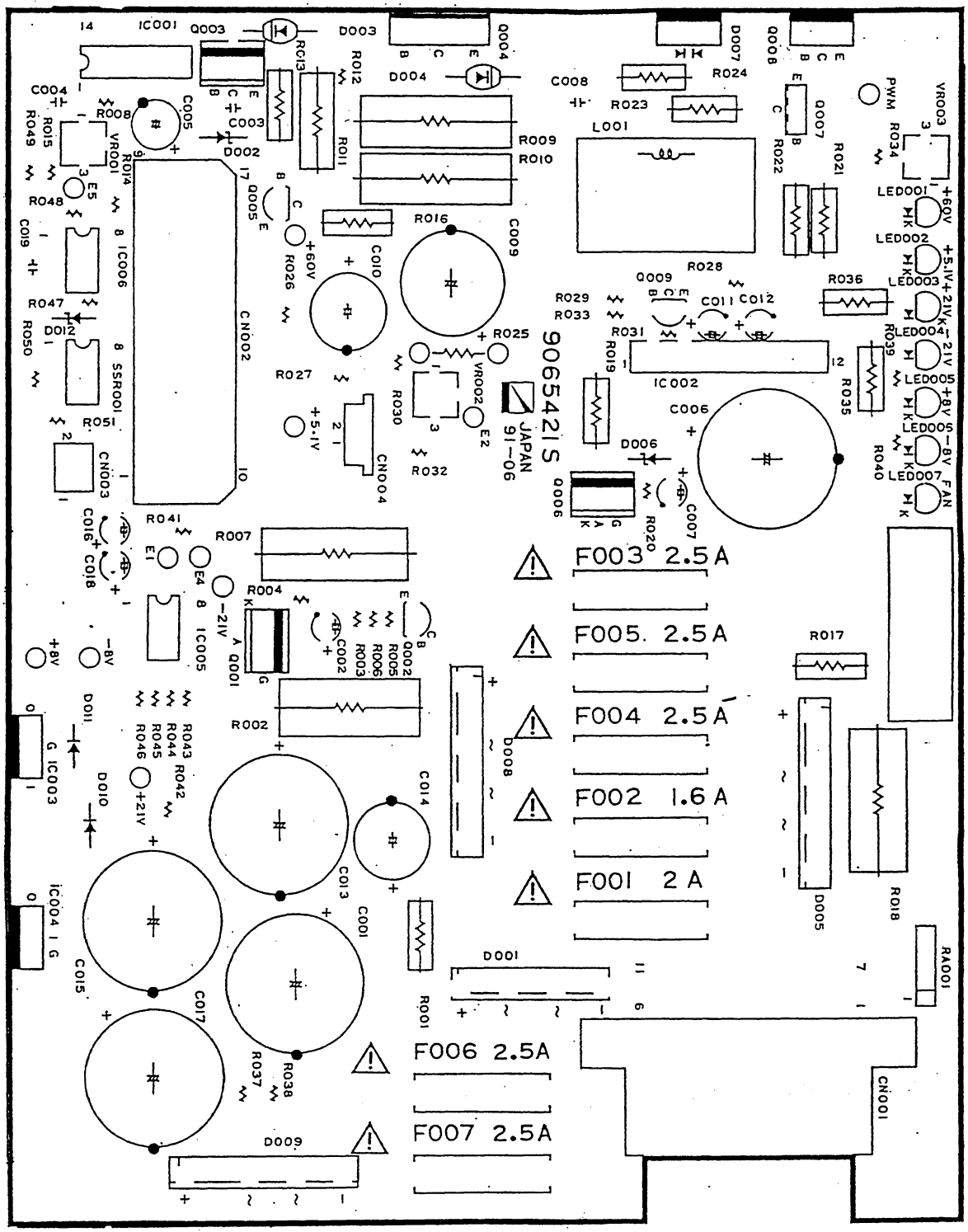
ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-06541	IC001	1250219	1	REG HA17723 (723CJ.G)
UP-06541	IC002	1601893	1	MD SWC-01
UP-06541	IC003	1253305	1	REG uPC7808H Regulator
UP-06541	IC004	1253288	1	REG uPC7908H Regulator
UP-06541	IC005-IC006	1204867	2	AIC HA17903PS Comparator
UP-06541	LED001-LED007	1102246	7	LED GL-3AR2 Red
UP-06541	L001	7415431	1	EN4-120-0090
UP-06541	Q001	5601323	1	SOCKET RT807
UP-06541	Q001	7415387	1	3P4MH
UP-06541	Q003	5601323	1	SOCKET RT807
UP-06541	Q003	7400162	1	2SD1135(C)
UP-06541	Q004	7400153	1	2SD1090
UP-06541	Q006	0950615	1	SCR 5P4M (5A400V)
UP-06541	Q006	5601323	1	SOCKET RT807
UP-06541	Q007	7415449	1	2SA1244
UP-06541	Q008	7415396	1	2SC3693
UP-06541	RA001	4090582	1	RM EXB-P84-103J
UP-06541	SSR001	7415458	1	PTR S12MD22
UP-06541	TSW001	7415422	1	COIL OHD3-90MU
UP-06541	VR001	4160809	1	TPOT GF06P 2KOHM
UP-06541	VR002	4160613	1	TPOT GF06P 10KOHM
UP-06541	VR003	4160907	1	TPOT GF-06S(ET-6S) 1KOHM

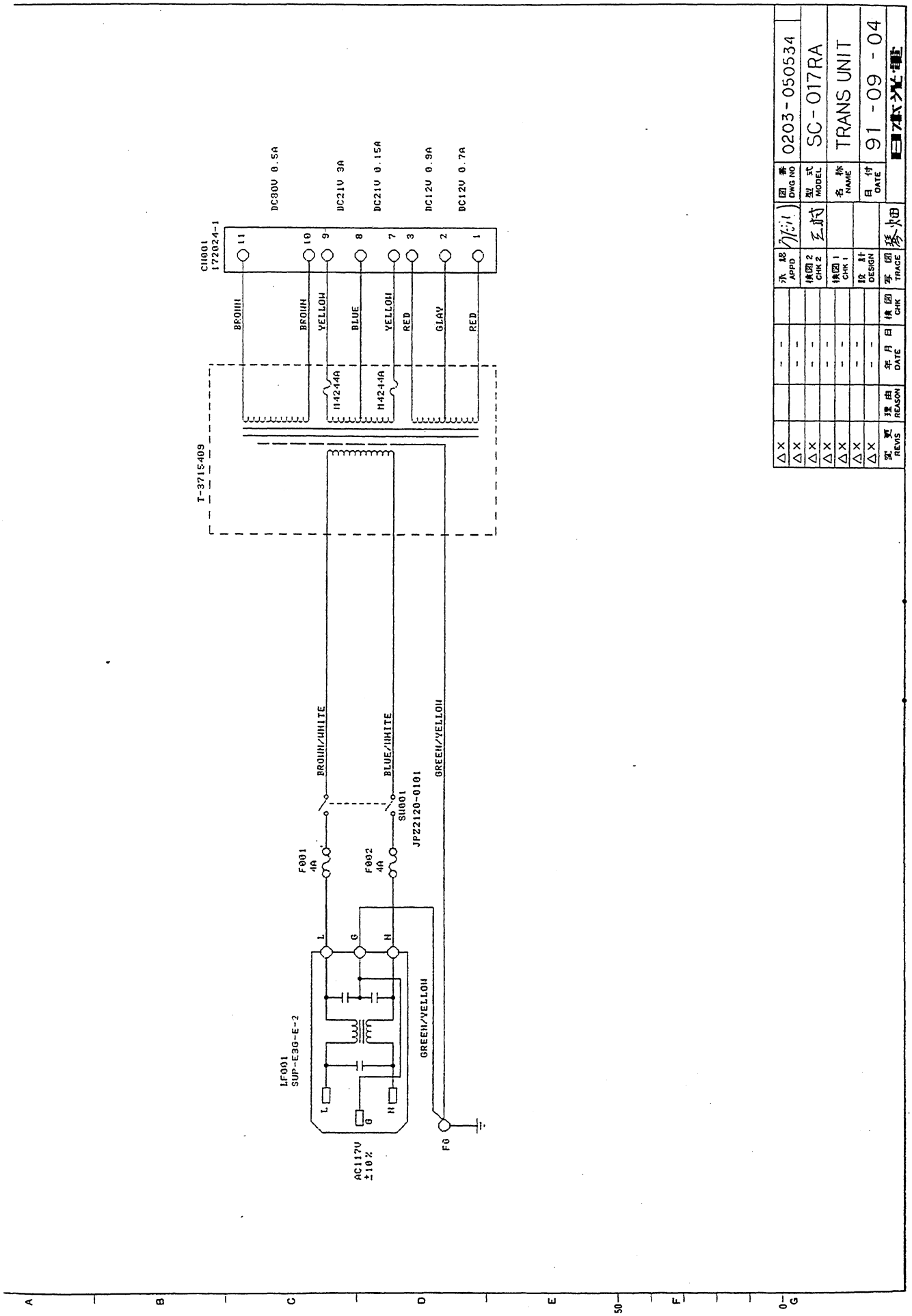
ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-06542 REGULATOR UNIT					
UP-06542	CNJ001	5413981	1	NCN	172038-1 11P
UP-06542	CNJ002	5415239	1	NCN	171363-1 17pin MALE
UP-06542	CNJ003	5428225	1	PCN	M60-02-30-114P
UP-06542	CNJ004	5424755	1	PCN	HNC2-2.5P-2DS 2P
UP-06542	CNP004	5424621	1	NCN	Contact HNC-2.5S-D-A
UP-06542	CNP004	5424657	1	PCN	Housing HNC2-2.5S-2 2P
UP-06542	C001	7415244	1		ECOS2CA821BA
UP-06542	C002	7415271	1		ECEA1HGE010
UP-06542	C003	3839757	1	FLC1	ECQ-V1H104JZ 0.1uF
UP-06542	C004	3839525	1	FLC1	ECQ-B1H102JZ 0.001uF
UP-06542	C005	7415262	1		ECEA2AGE220
UP-06542	C006	7415378	1		ECOS1VA822BA
UP-06542	C007	7415271	1		ECEA1HGE010
UP-06542	C008	3839525	1	FLC1	ECQ-B1H102JZ 0.001uF
UP-06542	C009	7415298	1		ECEA1EGE332
UP-06542	C010	7415315	1		ECEA1EGE102
UP-06542	C011-C012	7415289	2		ECEA1VGE330
UP-06542	C013	7415378	1		ECOS1VA822BA
UP-06542	C014	7415306	1		ECEA1VGE102
UP-06542	C015	7415369	1		ECOS1EA822BA
UP-06542	C016	7415289	1		ECEA1VGE330
UP-06542	C017	7415369	1		ECOS1EA822BA
UP-06542	C018	7415289	1		ECEA1VGE330
UP-06542	C019	3820795	1	FLC1	ECQ-B1H 103JZ 0.01uF
UP-06542	D001	7415476	1		D3SB40
UP-06542	D002	1090089	1	ZD3	HZ12LA2 Orange
UP-06542	D003-D004	7400198	2		V06E
UP-06542	D005	7415467	1		D5SB20
UP-06542	D006	7400126	1		HZ6LB2
UP-06542	D007	0910561	1	DP	S10SC4M 10A40V
UP-06542	D008-D009	7415467	2	D	D5SB20
UP-06542	D010-D011	003649	2	D	1SS81
UP-06542	D012	7400135	1	D	HZ6LA2
UP-06542	F001-F006	325854	6	FUSE	HOLDER F4034P
UP-06542	F001	104576	1	FUSE	179 120-2A
UP-06542	F002	342773	1	FUSE	179 120-1.6A
UP-06542	F003-F007	346181	5	FUSE	179 120-2.5A

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-06542	IC001	1250219	1	REG HA17723 (723CJ.G)
UP-06542	IC002	1601893	1	MD SWC-01
UP-06542	IC003	1253305	1	REG uPC7808H Regulator
UP-06542	IC004	1253288	1	REG uPC7908H Regulator
UP-06542	IC005-IC006	1204867	2	AIC HA17903PS Comparator
UP-06542	LED001-LED007	1102246	7	LED GL-3AR2 Red
UP-06542	L001	7415431	1	EN4-120-0090
UP-06542	Q001	5601323	1	SOCKET RT807
UP-06542	Q001	7415387	1	3P4MH
UP-06542	Q003	5601323	1	SOCKET RT807
UP-06542	Q003	7400162	1	2SD1135(C)
UP-06542	Q004	7400153	1	2SD1090
UP-06542	Q006	0950615	1	SCR 5P4M (5A400V)
UP-06542	Q006	5601323	1	SOCKET RT807
UP-06542	Q007	7415449	1	2SA1244
UP-06542	Q008	7415396	1	2SC3693
UP-06542	RA001	4090582	1	RM EXB-P84-103J
UP-06542	SSR001	7415458	1	PTR S12MD22
UP-06542	TSW001	7415422	1	COIL OHD3-90MU
UP-06542	VR001	4160809	1	TPOT GF06P 2KOHM
UP-06542	VR002	4160613	1	TPOT GF06P 10KOHM
UP-06542	VR003	4160907	1	TPOT GF-06S(ET-6S) 1KOHM

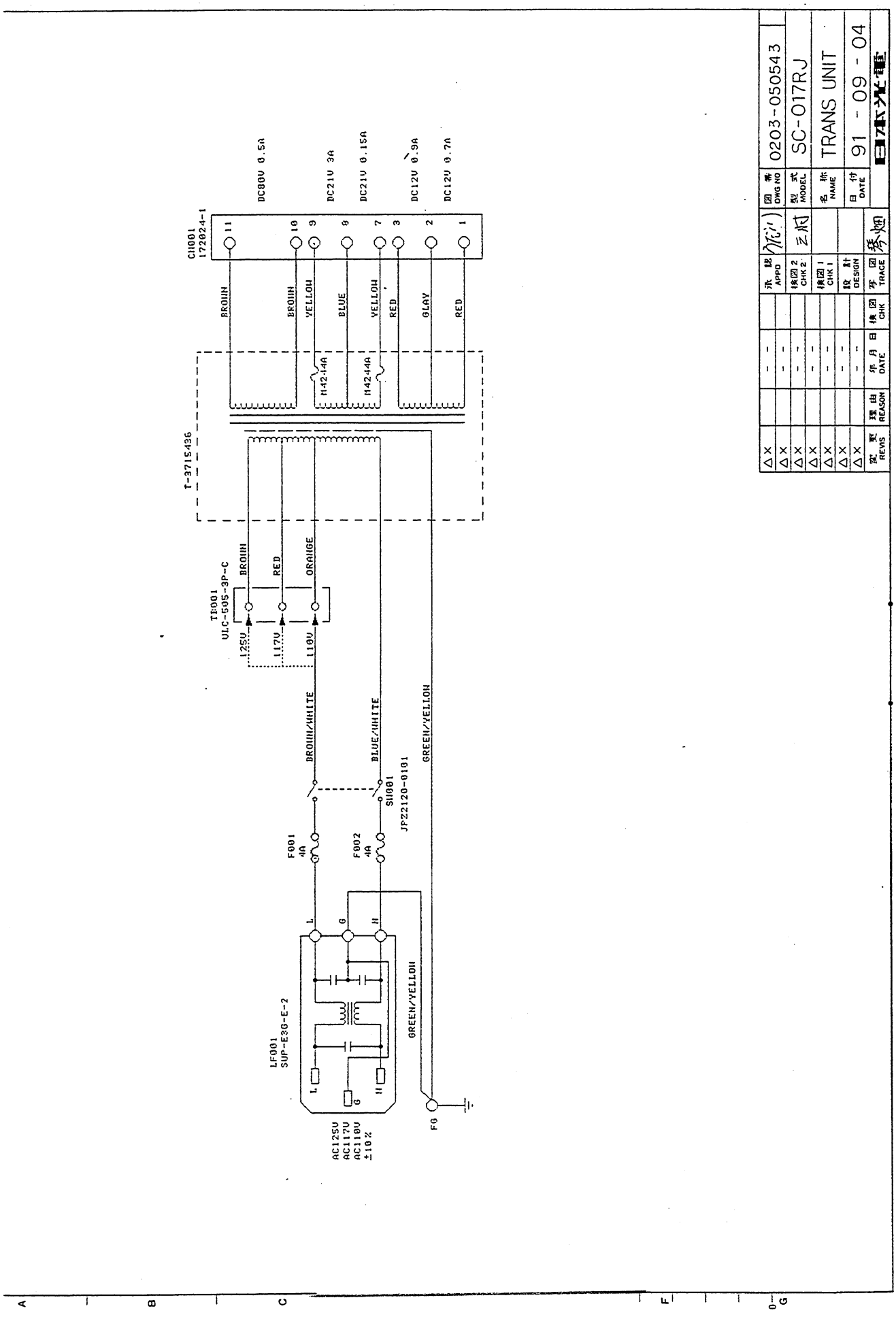
UP-06541 / 06542 Regulator Board

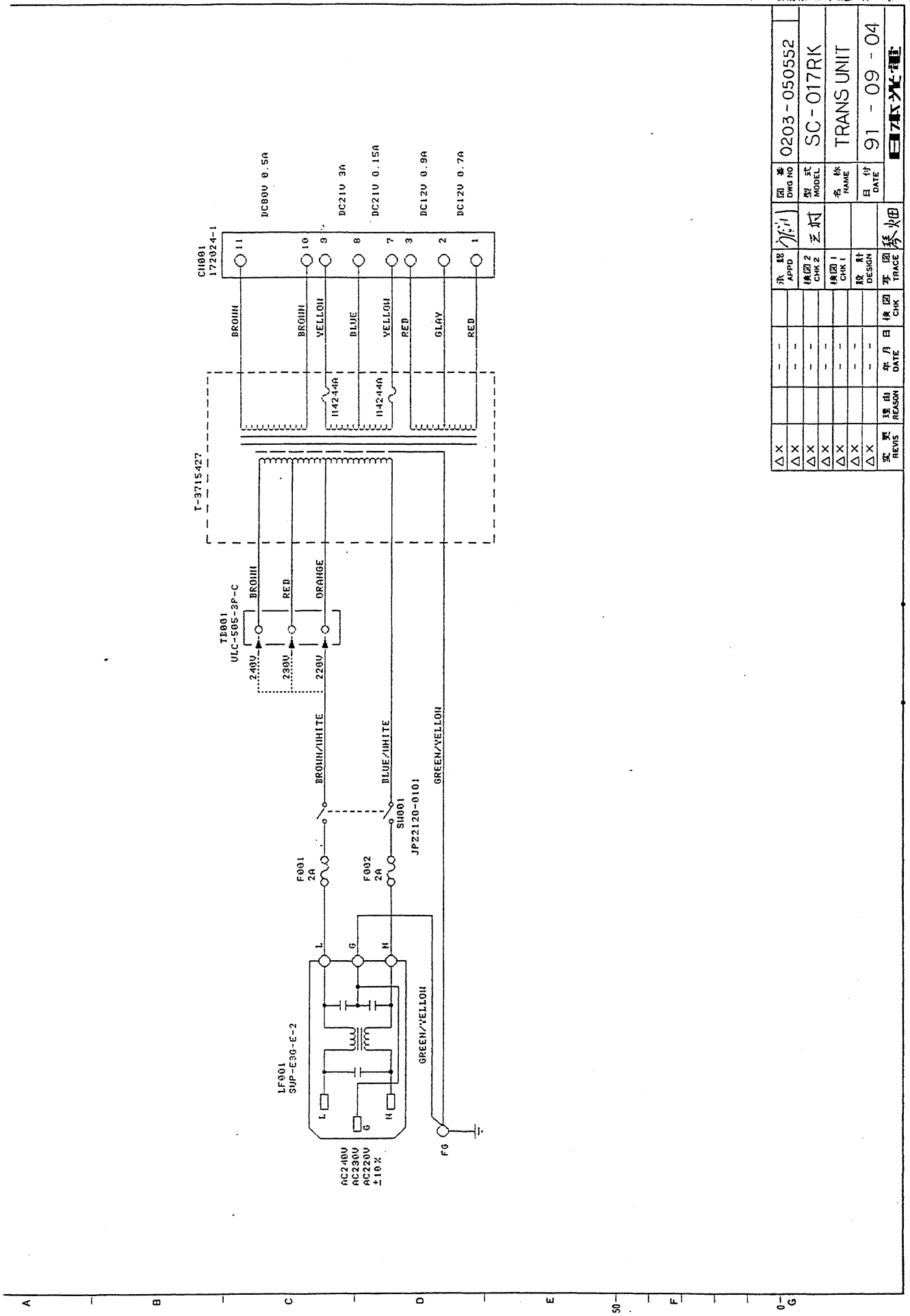
(Drawing shows UP-06541 and UP-06542 are the same except the fuses.)



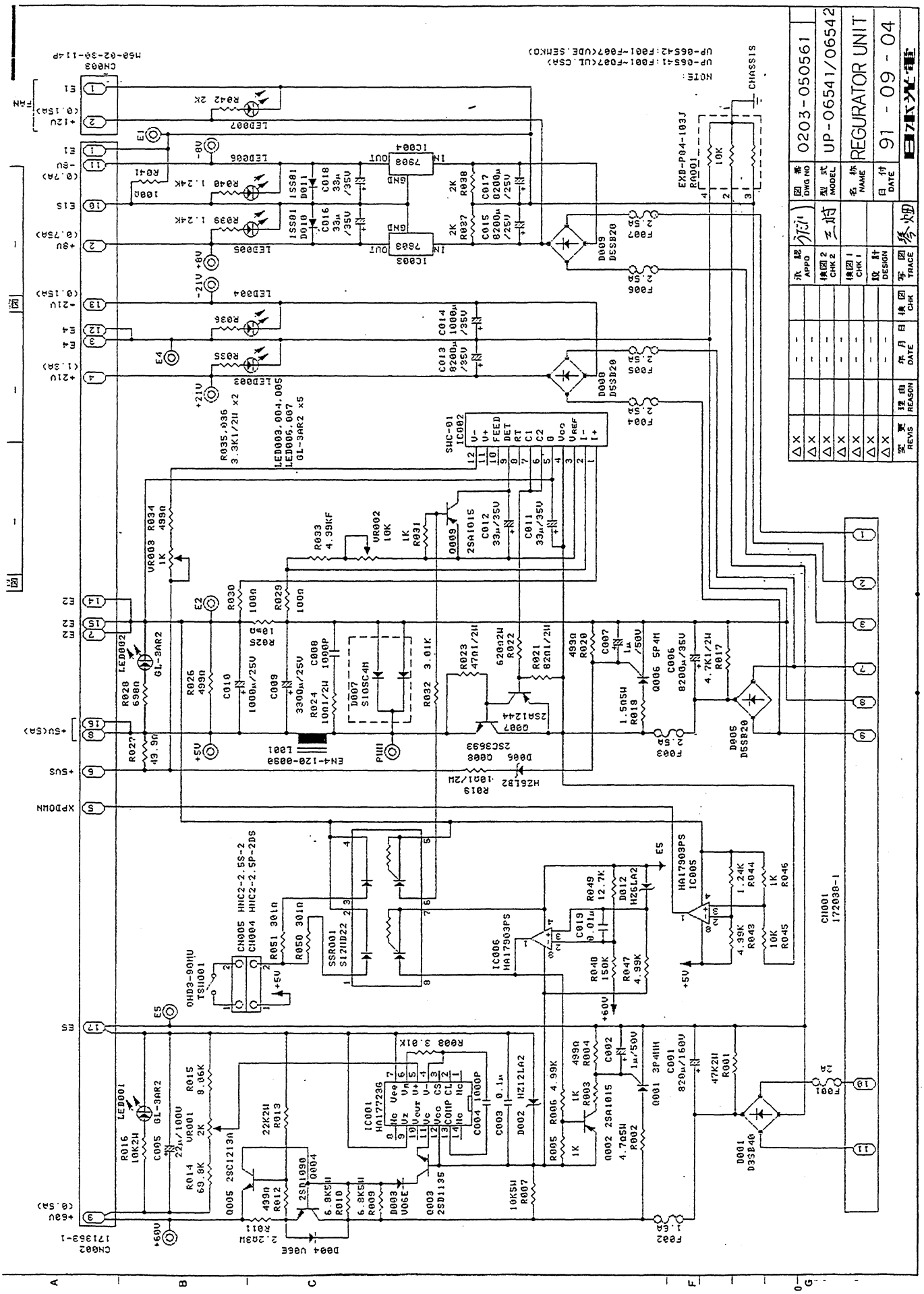


△X			- -			承認 APPD		図番 DWG NO	0203-050534				
△X			- -			検図2 CHK 2	名村	型式 MODEL	SC-017RA				
△X			- -			検図1 CHK 1		名称 NAME	TRANS UNIT				
△X			- -			設計 DESIGN		日付 DATE	91-09-04				
△X			- -			写図 TRACE	多畑	日本光電					
変更 REVIS		理由 REASON	年月日 DATE		検図 CHK								


CN001
172024-1
DC80V 0.5A
DC21V 3A
DC21V 0.15A
DC12V 0.9A
DC12V 0.7A
BROWN
BROWN
YELLOW
BLUE
YELLOW
RED
GRAY
RED
H42-14A
H42-14A
T-3715436
TB001
VLC-595-3P-C
BROWN
RED
ORANGE
125V
117V
110V
BROWN/WHITE
BLUE/WHITE
GREEN/YELLOW
F001
4A
F002
4A
SW001
JPZ2120-0101
LF001
SUP-E30-E-2
GREEN/YELLOW
FG
AC125V
AC117V
AC110V
±10%
△X
△X
△X
△X
△X
△X
改訂 REVIS
理由 REASON
作月日 DATE
作図 CHK
承認 APPD
作図 TRACE
図番 DWG NO
0203-050543
型式 MODEL
SC-017RJ
名称 NAME
TRANS UNIT
日付 DATE
91 - 09 - 04
日本光電


CN001
172024-1
DC30V 0.5A
DC21V 3A
DC21V 0.15A
DC12V 0.9A
DC12V 0.7A
BROWN
YELLOW
BLUE
RED
GRAY
T-3715427
TB001
ULC-505-3P-C
240V
230V
220V
ORANGE
BROWN/WHITE
BLUE/WHITE
GREEN/YELLOW
SW001
JP22120-0101
F001
2A
F002
2A
LF001
SUP-E30-E-2
AC240V
AC230V
AC220V
±10%
FG
0203-050552
SC-017RK
TRANS UNIT
91 - 09 - 04

· MANUAL CHANGE INFORMATION



0634-000103A

MANUAL CHANGE INFORMATION

Unit		Model	Serial No.	Revision
CPU board	UP-0668 (US-0668F)	MU-820RA	From 00379	E0
		MU-820RJ	From 00040	C0
DRAM board	QM-800P	MU-820RK	From 00116	

CPU board: To use optional DRAM board or 32-bed system, system clock is changed from 8 MHz to 16 MHz and ROM capacity is changed from 512 kbit to 1 Mbit.

DRAM board: Optional board to display disclosure ECG can be used from this revision.

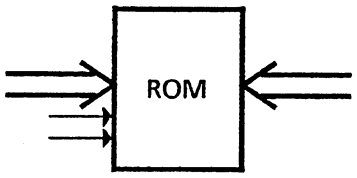
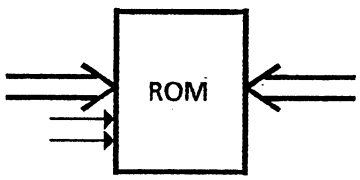
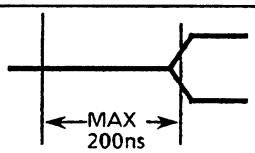
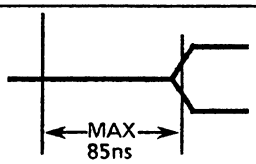
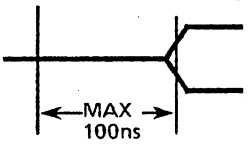
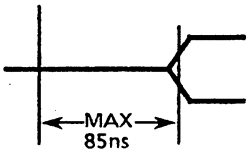
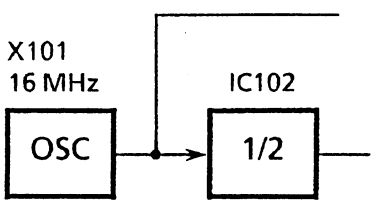
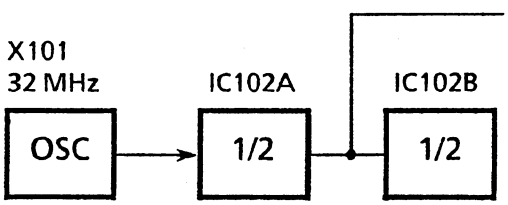
Pages 1-11, 1-13, 1-19, 1-20, 2-3, 3-1, 5-1, 5-3, 6-1, 6-2, 7-1, 8-1, 8-2, 10-3, 11-1, 12-1, 12-3, 13-C01

From	To
US-0260B	US-0668F
UP-02602	UP-0668

Section 1 Introduction

Page	From	To
1-12	(Replace the whole page.)	Page 6/44

Section 3 Circuit descriptions

Page	From	To
3-2	IC144-IC151 	IC144, 146, 148, 150 
	The Micro Processor ... ROMs (IC144-151).	The Micro Processor ... ROMs (IC144-150).
	CLK8M	CLK16M
		
	The ROM provides 512 kbyte memory and 200 ns access time. The total ... (IC144-151) is 256 kwords.	The ROM provides 1 Mbit memory and 85 ns access time. The total ... (IC144, 146, 148, 150) is 512 kwords.
3-3	CLK8M	CLK16M
		
	The RAM provides ... and 100 ns access time.	The RAM provides ... and 85 ns access time.
3-4		
Addition	(Add next to the last page.)	Page 7/44 to 13/44

Section 4 Selfcheck program

<table>
<tr><th>Page</th><th>From</th><th>To</th></tr>
<tr><td>4-2</td><td>Addition</td><td>
<table>
<tr><th>PCB</th><th>Initial self check</th><th>Manual self check</th></tr>
<tr><td>DRAM board
(option)</td><td>DRAM</td><td>DRAM
Backup battery</td></tr>
</table>
</td></tr>
<tr><td>4-6</td><td>Addition</td><td>4.2.5 DRAM board (option)
1) DRAM check
Queing construction check</td></tr>
</table>

<table>
<tr><th>Page</th><th>From</th><th>To</th></tr>
<tr><td>4-7</td><td>CPU-CHECK MENU
ROM
RAM
KEY
SOUND
RS232C</td><td>CPU-CHECK MENU
ROM
RAM
DRAM
KEY
SOUND
RS232C</td></tr>
<tr><td rowspan="2">4-8</td><td>—— POWER ON CHECK RESULT ——
CPU ------- OK
AD -------- OK
REC CNTL -- OK
WS/IO ------ OK</td><td>—— POWER ON CHECK RESULT ——
CPU ------- OK
AD -------- OK
REC CNTL -- OK
WS/IO ------ OK
DRAM ----- OK</td></tr>
<tr><td>—— SOFTWARE REVISION ——
CPU ----- Rev. X0-10
IC144, 145 Rev X0-10
IC146, 147 Rev X0-10

REC CNTL - Rev X0-05</td><td>—— SOFTWARE REVISION ——
CPU ----- Rev. **-**
IC144, 145 Rev **-**
IC146, 147 Rev **-**
IC148, 149 Rev **-**
IC150, 151 Rev **-**
REC CNTL - Rev **-**
WS/IO ---- Rev **-**</td></tr>
</table>

Page	From	To
4-9	17. BEAT SOUND - - - - - - - - LOW/HIGH 18. QRS SOUND - - - - ENABLE/DISABLE 19. 20. 21. 22. 23. 24. 25. 26.	17. BEAT SOUND - - - - - - - - LOW/HIGH 18. QRS SOUND - - - - - - ENABLE/DISABLE 19. WS841 COPY SIZE - - - - - - - NORMAL 20. ALARM ON/OFF - - - ENABLE/DISABLE 21. KEYBOARD TYPE - - - - - NEC/IBM AT 22. VITAL ALARM OFF MARK - - - ON/OFF 23. BAUD RATE (CNS-JJ) - - - 19200bps 24. FULL DISCLOSURE - - - - 10/60hours 25. ORG-8200 SUSPEND TIME - - - - 3min 26. ORG-8200 NOISE - - - - - - ON/OFF
4-12	※ROM CHECK · RAM CHECK · KEY CHECK ⋮	※ROM CHECK · RAM CHECK · DRAM CHECK · KEY CHECK
Between 4-14 and 4-15	(Add next to 4.3.4.1.2.)	Pages 14/44 to 17/44

Section 11 Electrical parts list

Page	From	To
Addition	(Add next to the last page.)	Pages 18/44 to 21/44

Section 12 Part location guide

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12-3	(Replace the whole page.)	Page 22/44
Addition	(Add next to the last page.)	Page 23/44

Section 13 Circuit diagram

Page	From	To
13-7 to 13-22	(Replace the whole pages.)	Pages 24/44 to 39/44
Addition	(Add next to the last page.)	Page 40/44 to 43/44

COMPATIBILITY

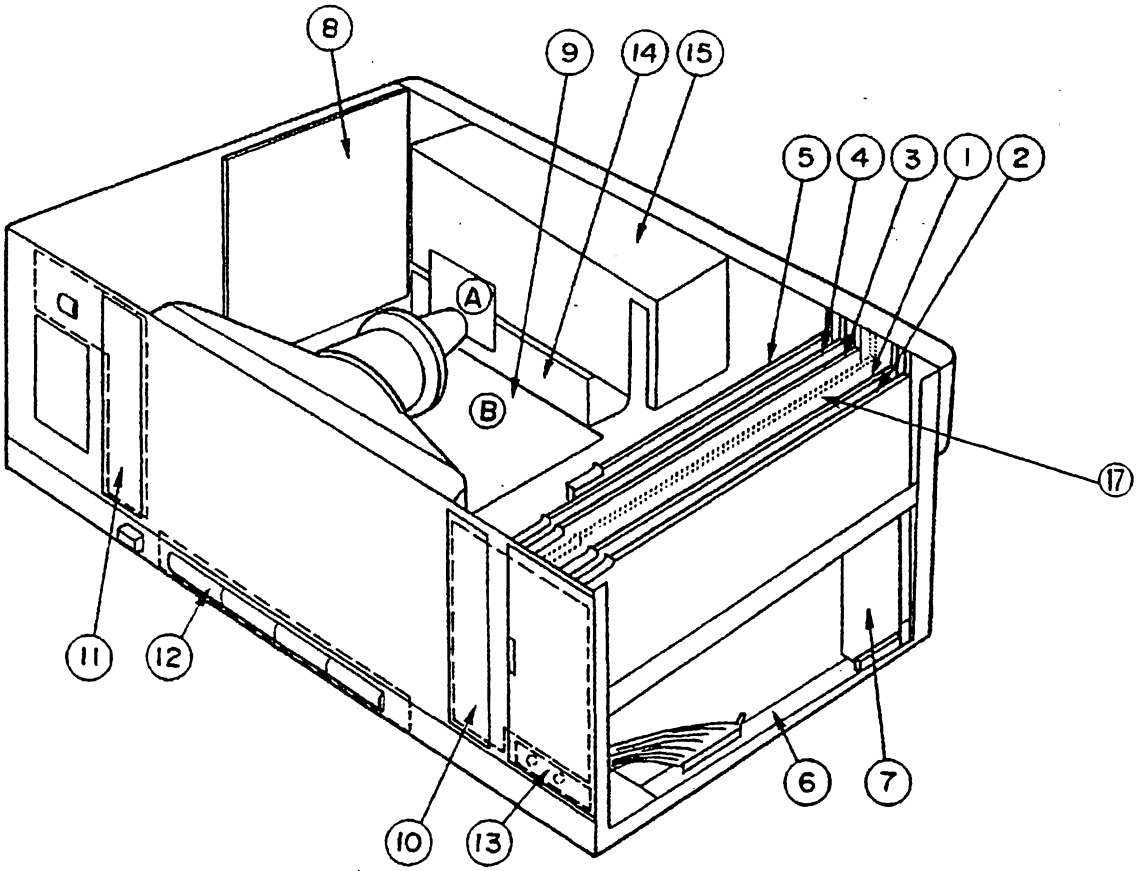
US-0260B = UP-02602 + ROM (A5-03 or previous)
US-0668F = UP-0668 + ROM (B1-01)

	~ A5-03	B1-01 ~
UP-02602	Yes	No
UP-0668	No	Yes

	QM-800P	32-bed system	Other functions
US-0260B	No	No	Yes
US-0668F	Yes	Yes *	Yes

*: Signal exchanger JJ-820RA/J/K (software revision B1-01) and and interface QI-808P are required.

1.5 Component location



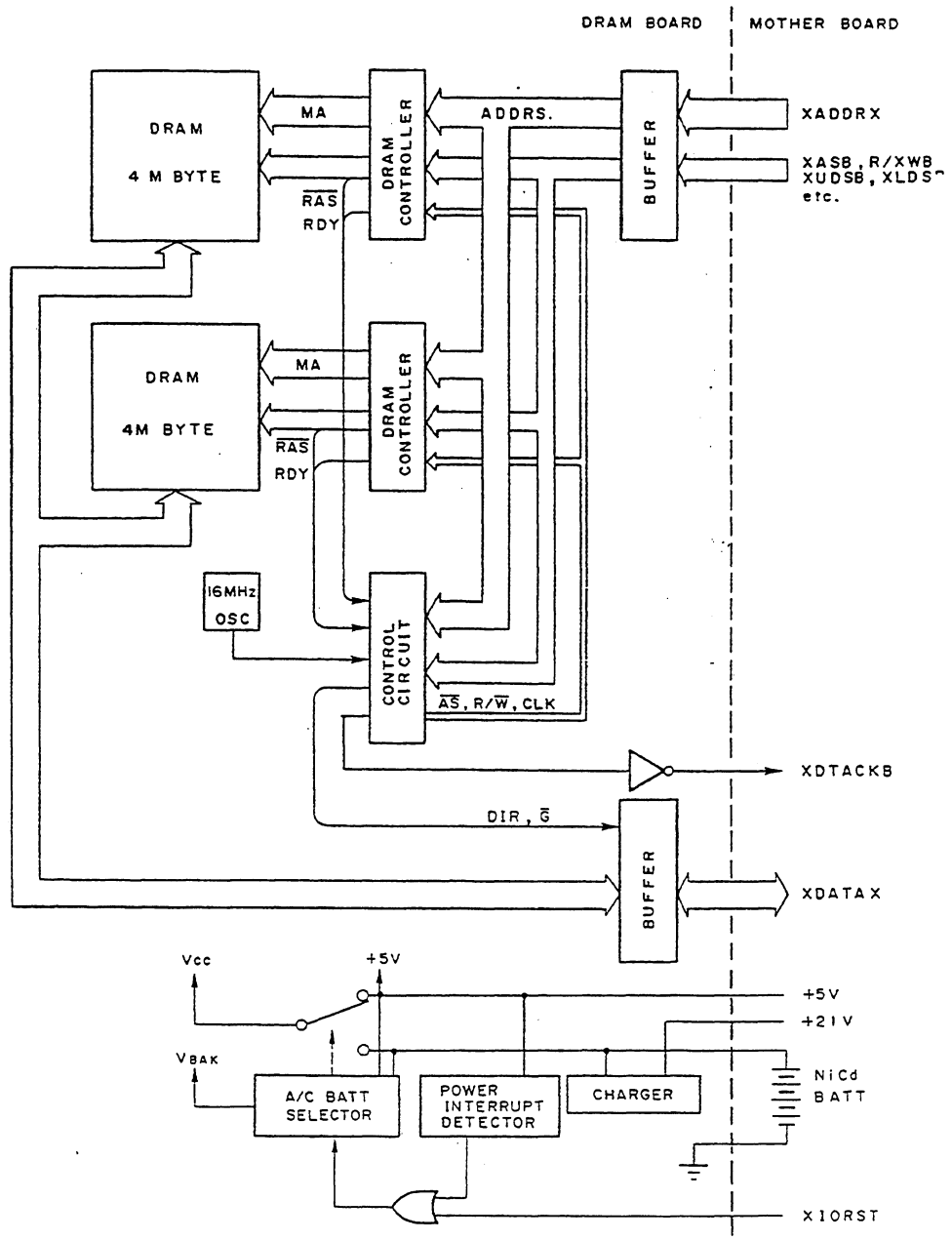
Index No.	Model	Description
①	UP-0668	CPU board
②	UP-0262	CRTC board
③	UP-0464	AD board
④	UP-0511	REC CNTL board
⑤	UP-0507	WS/IO board
⑥	UP-0539	Mother board
⑦	UP-0265	Sound control board
⑧	UP-0512	REC DRV board
⑨	VM-003P	CRT unit
⑩	UP-0481	Operation board, main
⑪	UP-0483	Operation board, left
⑫	UP-0564	Operation board, bottom
⑬	UP-0482	Operation board, VR
⑭	SC-013RA/J/K	Transformer unit
⑮	UP-0654	Regulator unit
⑯	RG712P	Recorder unit
⑰	QM-800P	DRAM board (Option)

3.11 DRAM Board (QM-800P)

3.11.1 General

Main Function

1) Stores disclosure waveform of 4 Mbyte and recall waveform of 992 episodes.
2) Memory backup for 10 min against power failure.



DRAM Block diagram

3.11.2 Block Diagram Explanation

1) DRAM/DRAM control
   DRAM controller ICs control DRAM IC of 64 pieces.

2) DTACK generator
   DTACK is sent to the CPU board only when the CPU accesses to DRAM.

3) Decoder
   Decoder is the selector for access to DRAM board from bus.

4) AC power failure detection circuit, AC / battery selector
   AC power failure is detected when XIORST signal is received from CPU board or +5V line of DRAM board decreased to less than 4.6V. When detected, +5V line for memory back-up etc. is switched to external battery .

5) Discharge stop timer
   Discharge stop timer stops the power supply from external battery after approx. 10min. of AC power failure detection in order to protect the battery from over-discharge.

6) Charger
   When the voltage of +5V line in DRAM board is more than 4.6V, +21V line charges the external battery in trickle mode.

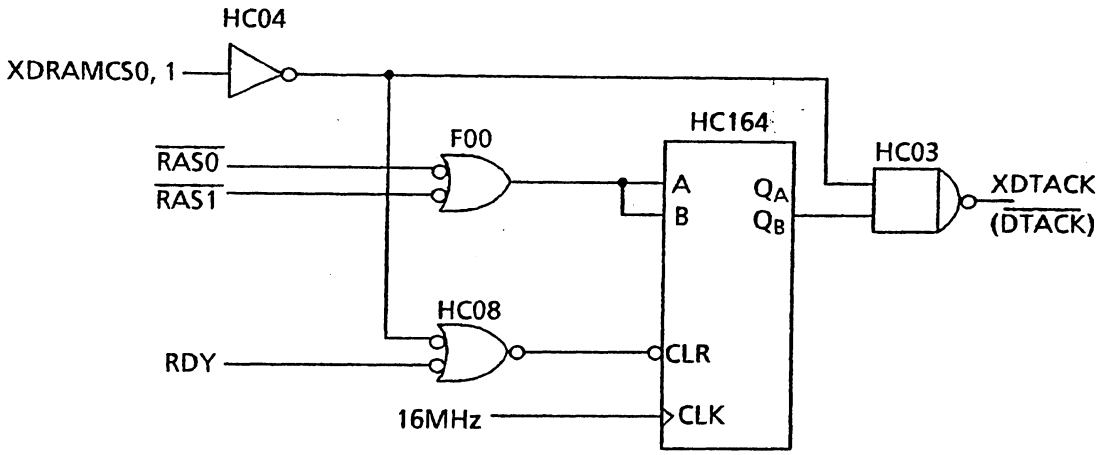
3.11.3 DRAM, DRAM control

DRAM board uses 1M bit DRAMs. One DRAM controller controls one block memory of 4Mbyte consisting 32pcs. of DRAM. Two blocks (8Mbyte) are mounted.

DRAM controller refreshes DRAMs at the interval of approx. 7.4 msec controlled by 15 MHz clock in internal refresh mode. During refreshing, RDY signal is set to low to suspend sending DTACK. Normal read cycle and early write cycle are employed.

3.11.4 DTACK generator

DTACK is sent to CPU board only when CPU accessees to DRAM. Timing of shift register is controlled by the internal generator clock.

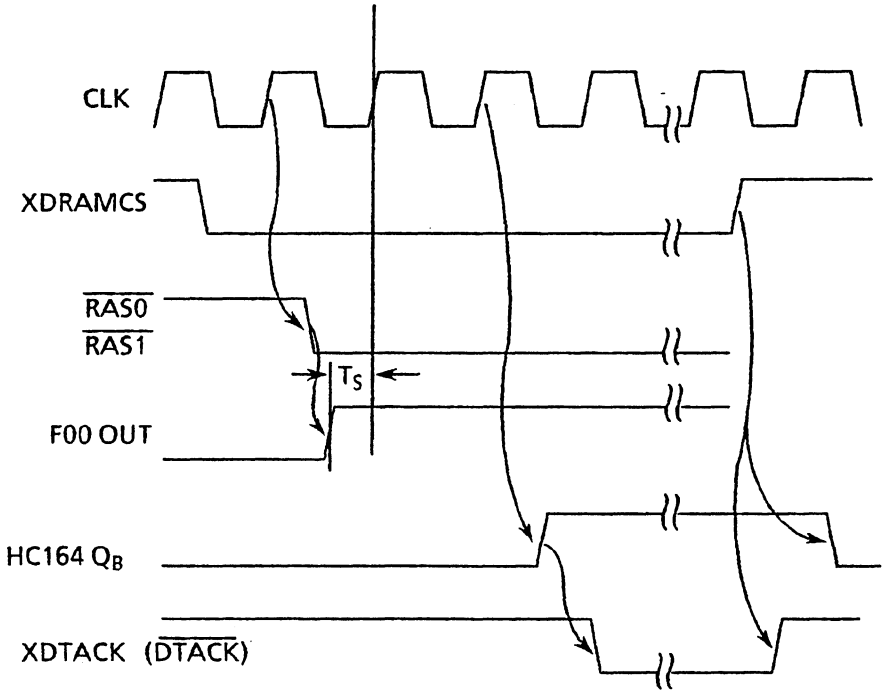


DTACK generator circuit

XDRAMCS0,1 : DRAM controller selection signal

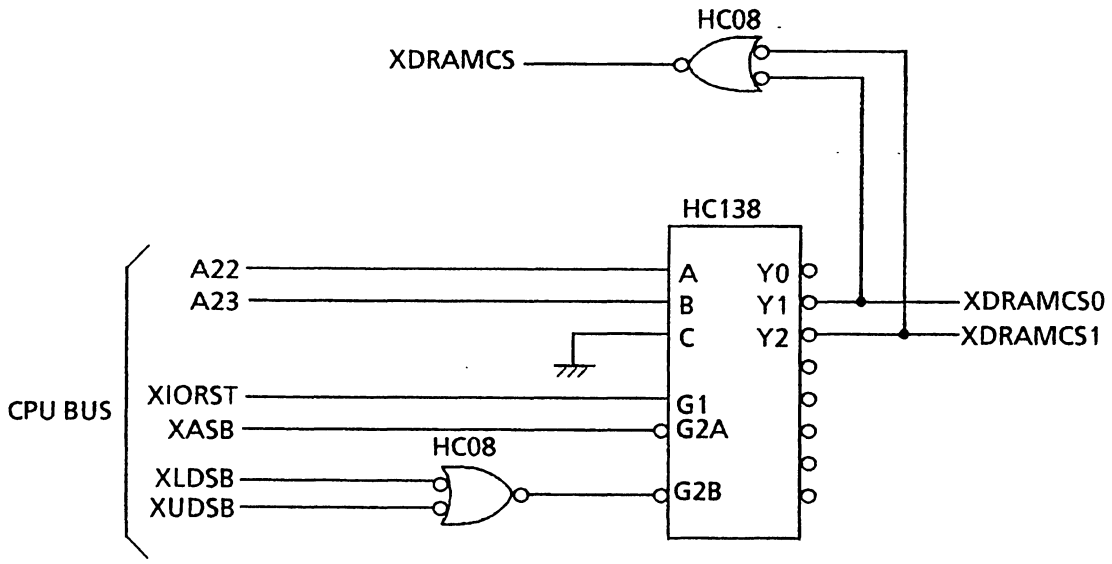
RAS0, RAS 1: RAS0, RAS1 output of DRAM controller

RDY: RDY output of DRAM controller. During refreshing DRAM, RDY output is set to low to clear shift register HC164 and stop DTACK generation.



DTACK generator timing chart

3.11.5 Decoder



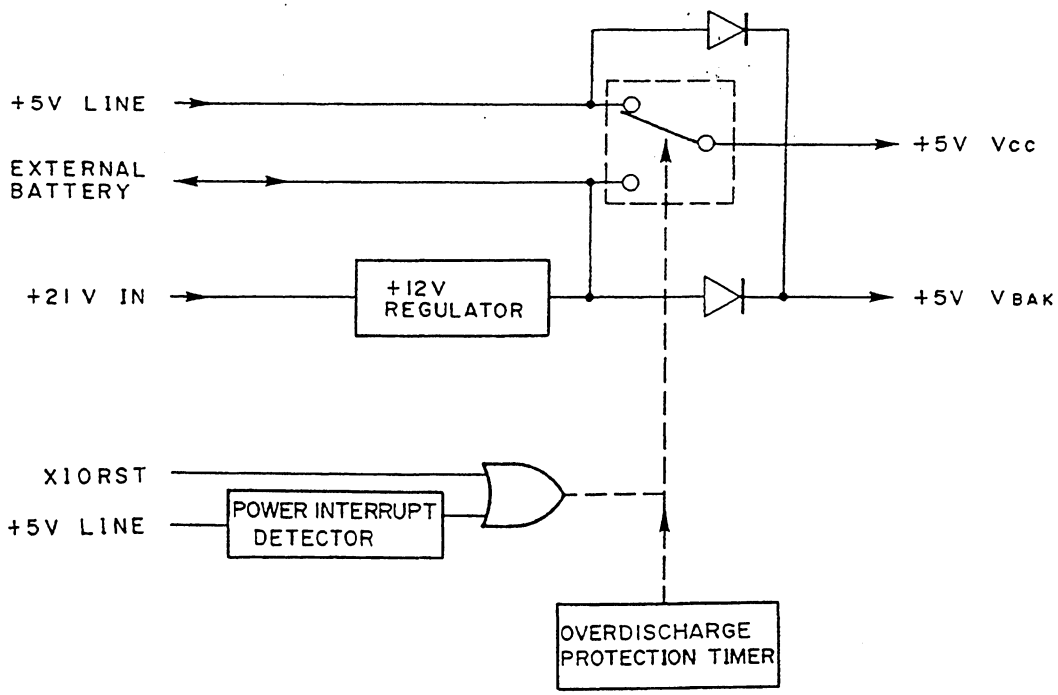
Decoder circuit

XDRAMCS: Also used for gate signal for bus buffer HCT640.

XIORST signal connected to G1 of HC138 blocks DRAM selection signal XDRAMCS0, 1 when the power of the CPU fails.
Normally the power of the DRAM board is supplied by +5V line. When power fails, this status is detected by the detector in the CPU board, XIORST is set low (XIORST is also set low when the CPU is reset by software or hardware), and the AC / battery selector selects battery to backup the memory. However, the detector functions securely only when the power fails quickly. If the power line voltage gradually drops, the detector may not function. Besides, XIORST chatters when it changes from high to low. To enhance detection reliability, another voltage detector is mounted and the detector out and XIORST are connected to OR gate. If the DRAM board switches to backup status earlier than the CPU board, a bus error occurs. Therefore, detection threshold level of the detector in the CPU board is approx. 4.8V and that in the DRAM board is approx. 4.6V. Additional transistors improve detection range as the detector TL7705 may not function under the power supply of 3.5V or less.

3.11.6 Power Failure Detector, AC / Battery Selector

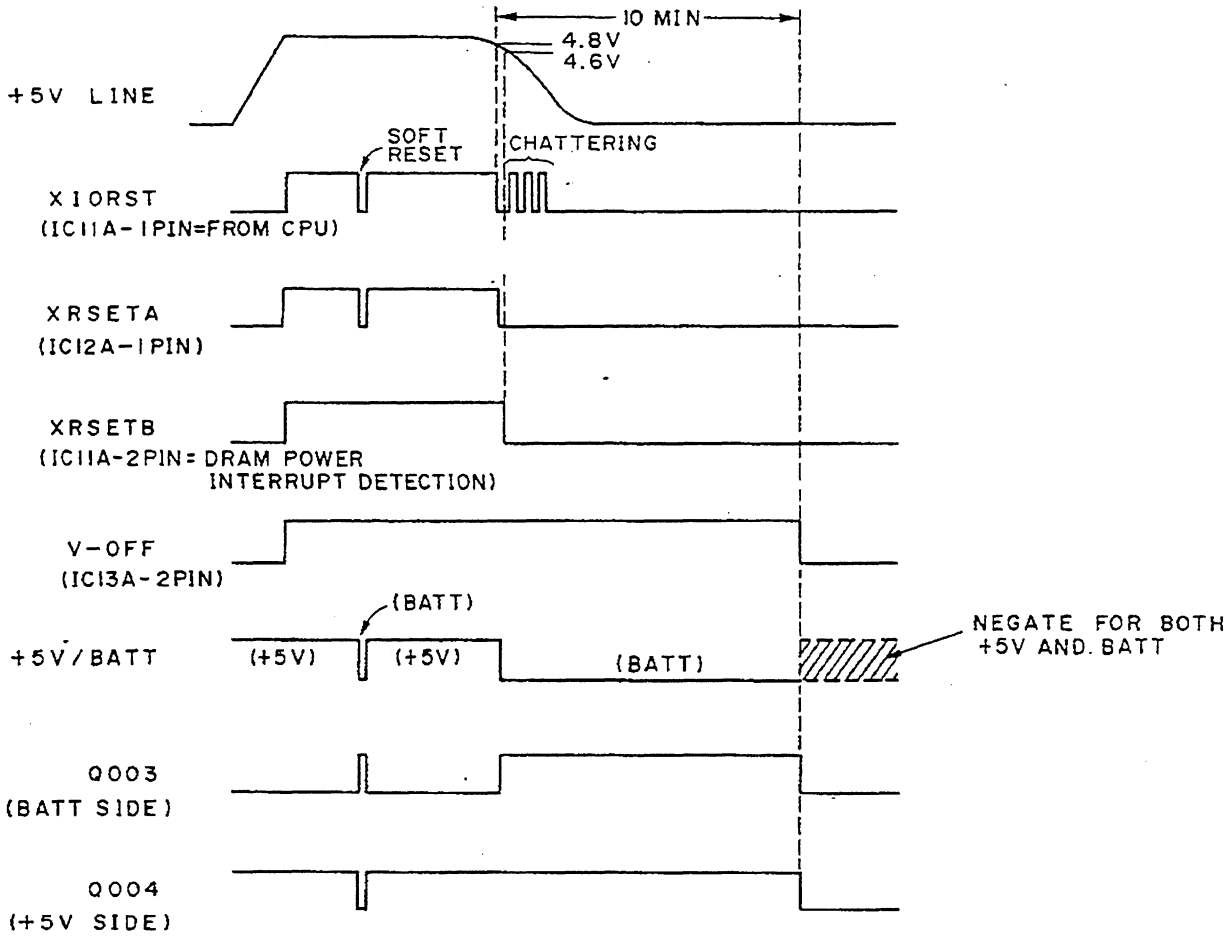
When XIORST is applied from the CPU board or the detector in the DRAM board detects the failure status, backup is maintained for 10 min. max.



Power failure detector and overdischarge protection timer block

3.11.7 Overdischarge Protection Timer

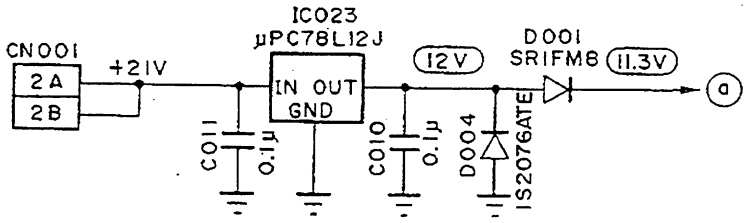
To protect the backup battery from being damaged due to overdischarge, backup is maintained for 10 min. controlled by the timer MC14521.



Power failure detection and protection timer timing

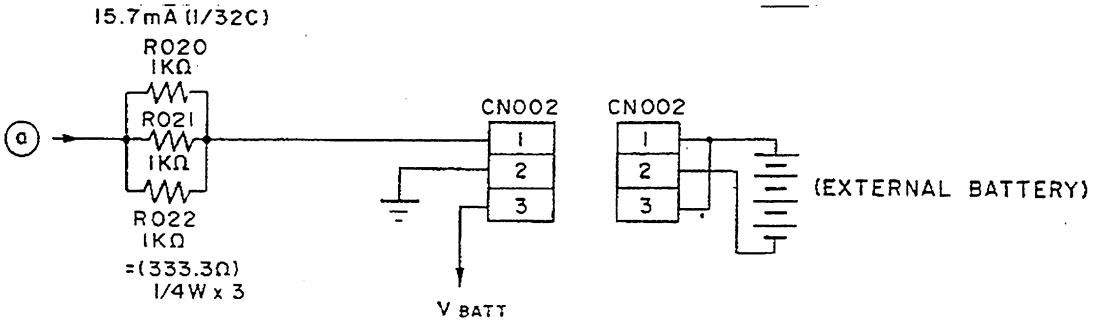
3.11.8 Charger

The external battery is charged by a +12V regulator from unregulated +21V. D101 protects the regulator from damage due to back current during power-off so that actual voltage applied to the battery is 11.3V.



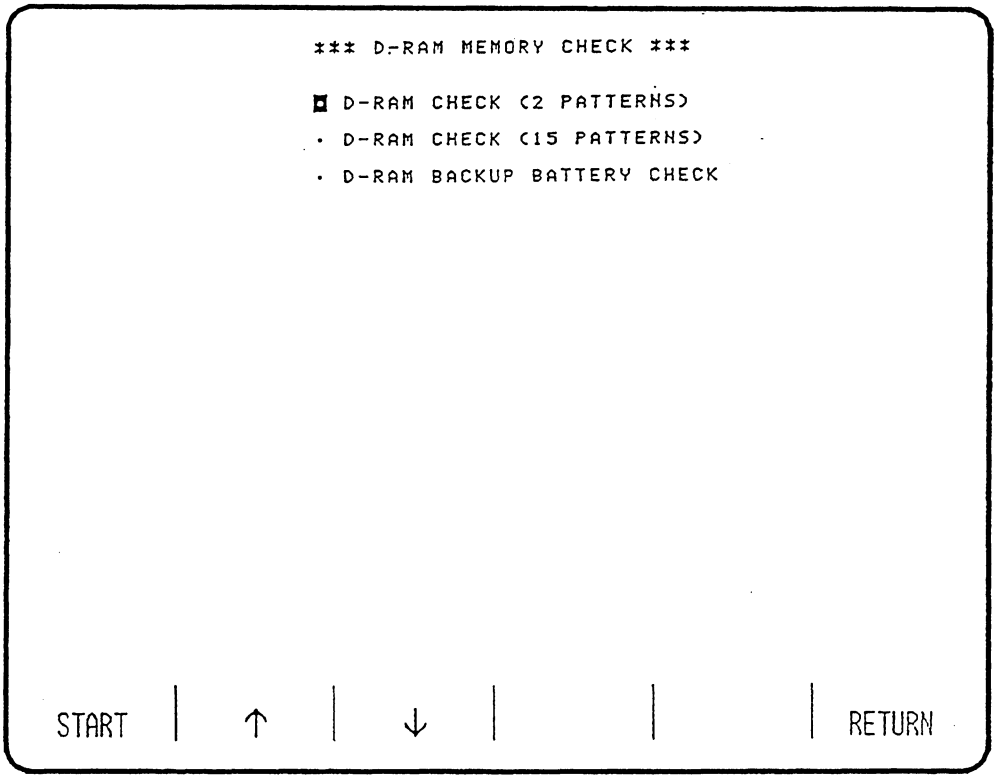
Regulator circuit

11.3 V is applied to the battery through R020 to R022. When the battery is fully charged (6.08V), charging current is 15.7 mA (1 / 32C). When the battery voltage decreases, the current increases (eg. current of 1 / 25C at voltage of 4.5V). When the battery connector is disconnected, charging current is turned off.



VBAK is power supply for the power failure detector and the overdischarge protection timer. VBAK is constantly supplied by either +5V line or external battery regardless of power on or off. While the power is turned off, 120μA is consumed. With this power consumption, the external battery of 500 mAH lasts for 5.8 months.

4.3.4.1.3 DRAM Memory Check

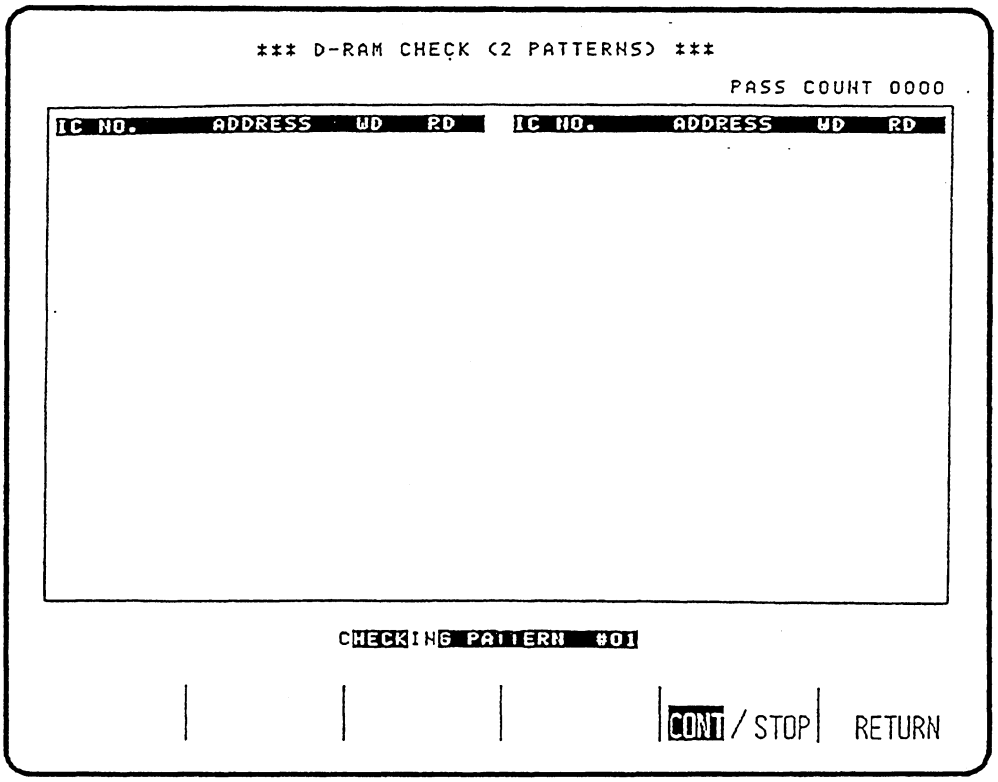


↑ ↓: Selects a check item from the check items on the CRT

START: Executes the program for selected check item while changing to the display for the check item

RETURN: Returns to the CHECK MENU display

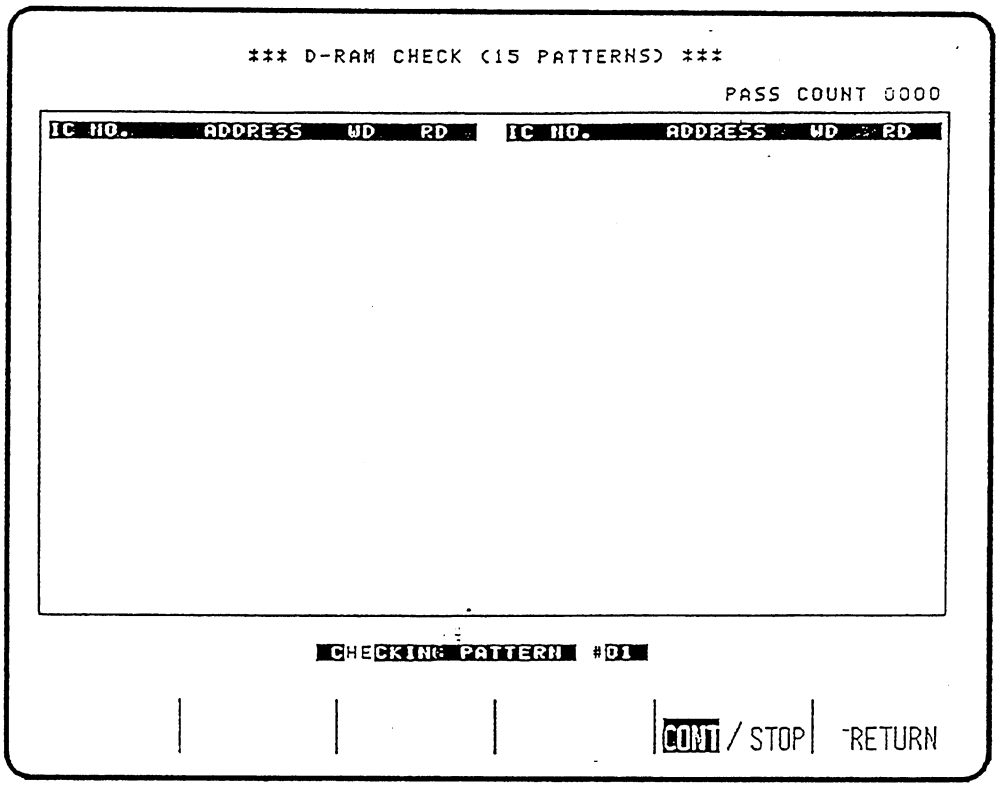
◆ **DRAM Check (2 patterns)**



The check is executed by comparing each data after writing one of the following check patterns No. 1 and 2. This check is repeated until the STOP key pressed.

No.	Pattern
1	55555555H
2	AAAAAAAAH

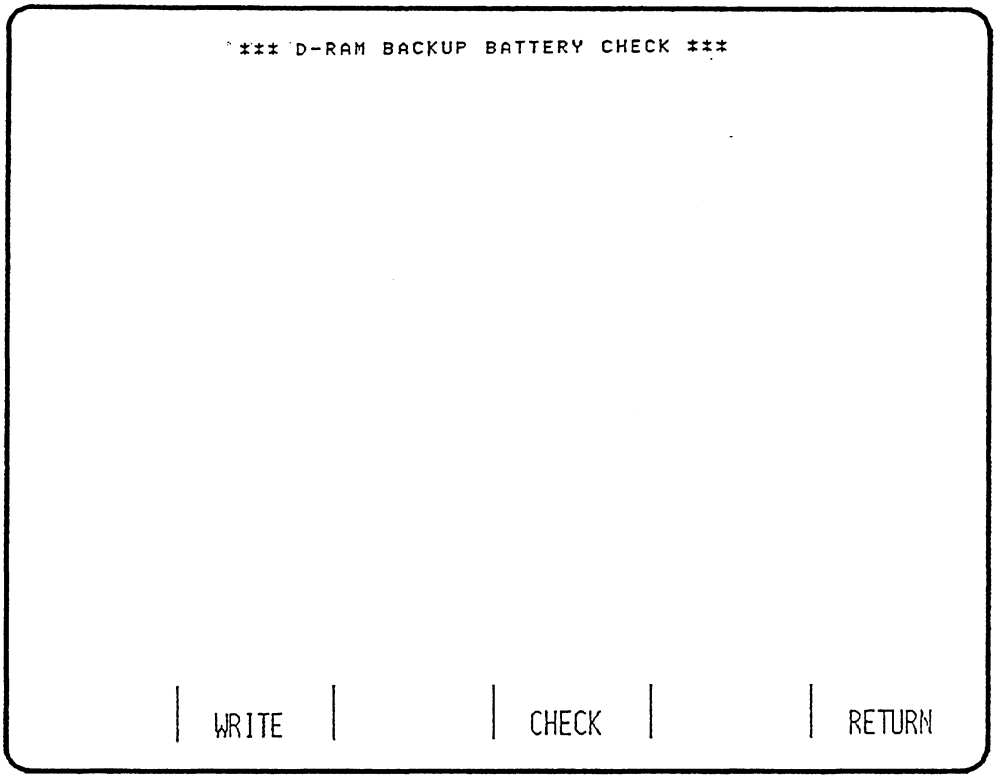
◆ **DRAM Check (15 patterns)**



The check is executed by comparing each data after writing one of the following check patterns No. 1 to No. 15. This check is repeated until the STOP key pressed.

No.	Pattern	No.	Pattern
1	Decrement (byte)	9	Upper byte: FFH, lower byte: 00H
2	55H (byte)	10	00H (byte)
3	OFH (byte)	11	Bit shift (word)
4	Alternating 00H and FFH	12	5555H (word)
5	Upper byte: 00H, lower byte: FFH	13	AAAAH (word)
6	AAH (byte)	14	FFFFH (word)
7	FOH (byte)	15	0000H (word)
8	Alternating FFH and 00H		

◆ **DRAM Backup Battery Check**



Checks if the backup battery is fully charged.

(1) Press the WRITE key.
(2) Turn off the power.
(3) Wait for 9 minutes (less than 10 minutes).
(4) Keep pressing the SELFCHECK key and turn on the power.
(5) Call up this screen again and press the CHECK key.

If it is normal, ERROR is not displayed. If not, ERROR is displayed.

Electrical Parts list

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-0668 CPU BD (without ROM)				
UP-0668	BAT101	5650546	1	CR17335SE-T-C7
UP-0668	CN101	5427939	1	PCN PCN10EA-90P-2.54DS(05)
UP-0668	CN102	5427895	1	PCN PCN10EA-32P-2.54DS(05)
UP-0668	CN103	5408033	1	ACN2 RDBD-25SE-LNA FEMALE
UP-0668	CN104	5445474	1	PCN IL-2P-S3FP2-1
UP-0668	C101	4312575	1	TC04 204M2002 226MB(22uF/20V)
UP-0668	C102	4317525	1	CEC1 TP D55Y5V1H 104Z 5-W
UP-0668	C103	4312557	1	TC04 204M2002 106MB(10uF/20V)
UP-0668	C104	4315304	1	FLC1 ECQ-V 1H 104JZ3 (0.1uF)
UP-0668	C105	4315162	1	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0668	C106	4312503	1	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0668	C107	4317552	1	CEC2 DD05-989SL 220K500 (22pF)
UP-0668	C109	4312503	1	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0668	C110-C117	4317525	8	CEC1 TP D55Y5V1H 104Z 5-W
UP-0668	C118-C124	4312503	7	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0668	C125-C141	4317525	17	CEC1 TP D55Y5V1H 104Z 5-W
UP-0668	D101	4320013	1	D 1SS104,TP3
UP-0668	D102	4320022	1	D 1SS106TE
UP-0668	D103	4325071	1	ZD1 HZ3C3TE (3.3-3.5V)
UP-0668	D105-D106	4320031	2	D 1S2076ATE
UP-0668	D107-D108	4320013	2	D 1SS104,TP3
UP-0668	IC101	1208533	1	CPU TMP68HC000N-16
UP-0668	IC102	1205135	1	TIC 74F74PC
UP-0668	IC104	1203271	1	TIC SN74LS164
UP-0668	IC105	1203895	1	TIC SN74LS393
UP-0668	IC106	1205518	1	TIC 74F00PC
UP-0668	IC107-IC108	1205126	2	TIC 74F32PC
UP-0668	IC109	1202664	1	TIC SN74LS09
UP-0668	IC111-IC112	1206544	2	TIC 74F138PC(N74F138N)
UP-0668	IC113	1304465	1	TIC 74ACT138PC
UP-0668	IC114	1206544	1	TIC 74F138PC(N74F138N)
UP-0668	IC115	1202503	1	TIC SN74LS27N
UP-0668	IC116	1253207	1	AIC TL7705CP Voltage Detector
UP-0668	IC117	1303528	1	MIC uPD74HC123C(HD74HC123P)
UP-0668	IC118	1303092	1	MIC HD74HC74P(uPD74HC74C)
UP-0668	IC119	1302948	1	MIC uPD74HC08C(HD74HC08P)
UP-0668	IC120	1206598	1	TIC 74F14PC(N74F14N)
UP-0668	IC121	1303706	1	MIC HD74HC01P
UP-0668	IC122	1202726	1	TIC SN74LS21
UP-0668	IC123	1303742	1	MIC HD74HCT138P
UP-0668	IC124	1302948	1	MIC uPD74HC08C(HD74HC08P)

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-0668	IC125-IC126	1303092	2	MIC	HD74HC74P(uPD74HC74C)
UP-0668	IC127	1303715	1	MIC	uPD74HC148C
UP-0668	IC128	1302948	1	MIC	uPD74HC08C(HD74HC08P)
UP-0668	IC129	1303092	1	MIC	HD74HC74P(uPD74HC74C)
UP-0668	IC130	1303813	1	MIC	HD74HCT534P
UP-0668	IC131	1303715	1	MIC	uPD74HC148C
UP-0668	IC132	1303769	1	MIC	uPD74HCT240C
UP-0668	IC133	1303742	1	MIC	HD74HCT138P
UP-0668	IC134-IC135	1302948	2	MIC	uPD74HC08C(HD74HC08P)
UP-0668	IC136-IC139	1303092	4	MIC	HD74HC74P(uPD74HC74C)
UP-0668	IC140	1303804	1	MIC	uPD74HCT374C
UP-0668	IC141	1303715	1	MIC	uPD74HC148C
UP-0668	IC142	1303769	1	MIC	uPD74HCT240C
UP-0668	IC143	1303742	1	MIC	HD74HCT138P
UP-0668	IC152-IC167	1208604	16	CPU	HM62256LP-8 /85
UP-0668	IC168	1303234	1	MIC	uPD74HC132C(HD74HC132P)
UP-0668	IC169	1303662	1	CPU	MSM6242 RS
UP-0668	IC172	1206446	1	CPU	uPD71051C
UP-0668	IC173	1206455	1	CPU	uPD71054C
UP-0668	IC174	1205206	1	TIC	SN75188N
UP-0668	IC175	1205198	1	TIC	SN75189AN
UP-0668	IC176	1302859	1	CPU	uPD8279C-2
UP-0668	IC177	1202762	1	TIC	SN74LS32
UP-0668	IC178	1204867	1	AIC	HA17903PS Comparator
UP-0668	IC179-IC180	1303769	2	MIC	uPD74HCT240C
UP-0668	IC181	1303813	1	MIC	HD74HCT534P
UP-0668	IC182-IC184	1206589	3	TIC	74F533PC(N74F533N)
UP-0668	IC185-IC186	1204983	2	TIC	SN74LS640
UP-0668	IC187-IC188	1303769	2	MIC	uPD74HCT240C
UP-0668	IC189	4346529	1	REG	uPC78L12J-T
UP-0668	IC190	4346538	1	REG	uPC79L12J-T
UP-0668	IC191	1205108	1	TIC	74F04PC
UP-0668	IC192-IC193	1205135	2	TIC	74F74PC
UP-0668	IC196-IC198	1205153	3	TIC	74F164PC
UP-0668	IC199	1206268	1	TIC	74F158
UP-0668	IC200	1206214	1	TIC	SN74LS06
UP-0668	IC201	1205117	1	TIC	74F08PC
UP-0668	IC202	1205135	1	TIC	74F74PC
UP-0668	IC203	1302957	1	MIC	HD74HC14P(uPD74HC14C)
UP-0668	IC204	1205572	1	TIC	74F244PC 8BUFF
UP-0668	LED101-LED110	1102246	10	LED	GL-3AR2 Red
UP-0668	Q101	4335069	1	TRC	2SC1213AKDTZ
UP-0668	RA101-RA106	4342783	6	RM	EXB-F9 E 104JYV
UP-0668	RA107	4342765	1	RM	EXB-F9 E 472JYV

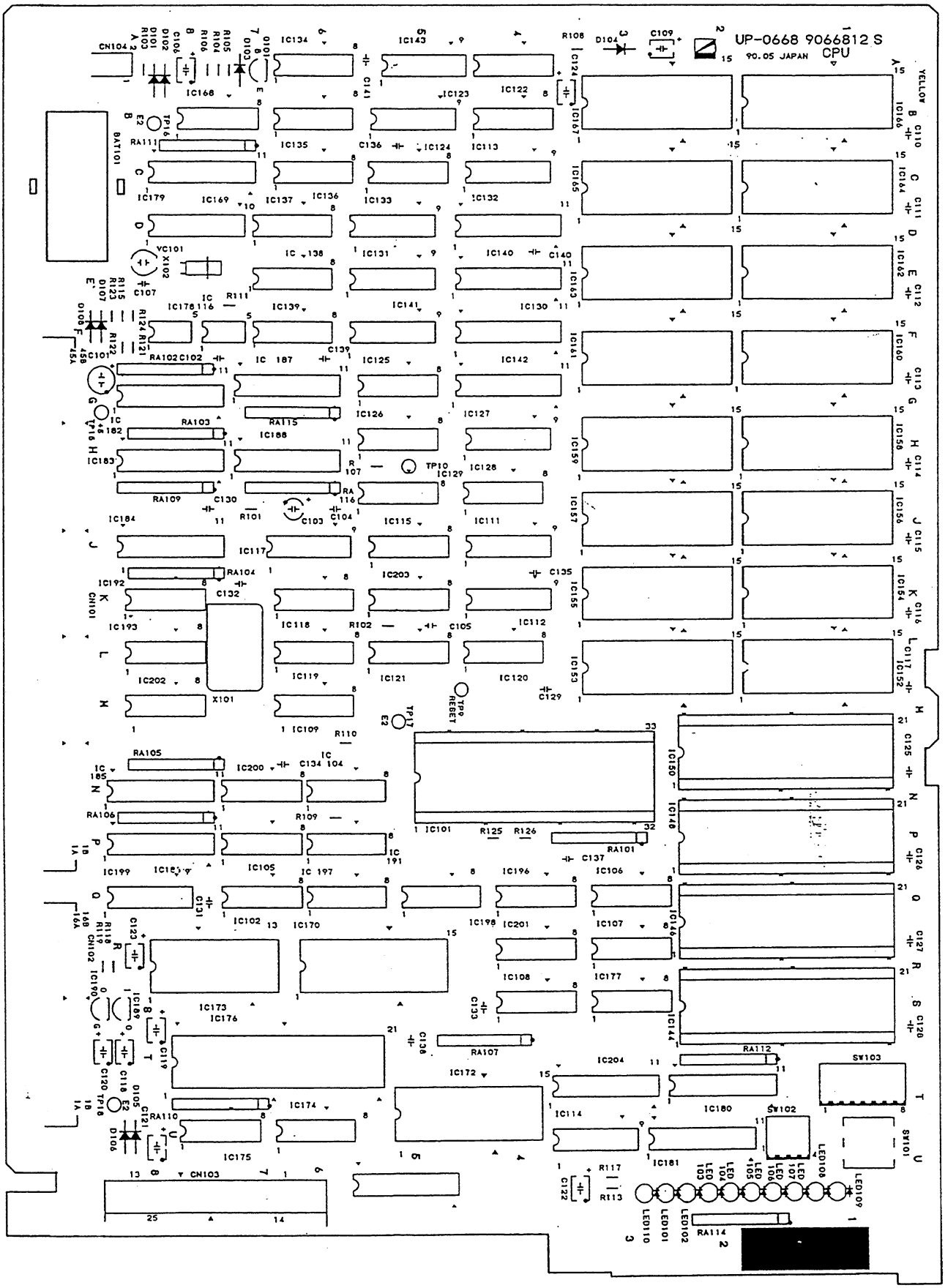
ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-0668	RA109-RA112	4342765	4	RM	EXB-F9 E 472JYV
UP-0668	RA114	4342729	1	RM	EXB-F9 E 102JYV
UP-0668	RA115-RA116	4342765	2	RM	EXB-F9 E 472JYV
UP-0668	SKT101	5601582	1	SOKT	IC SOCKET XR3G-6401
UP-0668	SKT144	5422605	1	SOKT	IC SOCKET DL-2-40A (01)
UP-0668	SKT146	5422605	1	SOKT	IC SOCKET DL-2-40A (01)
UP-0668	SKT148	5422605	1	SOKT	IC SOCKET DL-2-40A (01)
UP-0668	SKT150	5422605	1	SOKT	IC SOCKET DL-2-40A (01)
UP-0668	SW101	3352088	1	SW	SKHCAD (KHC10904)
UP-0668	SW102	3280325	1	SW	B-4A-T
UP-0668	SW103	3352435	1	SW	D1P SW B-8A
UP-0668	VC101	3890469	1	VC	TZ03R 300ER 5.2-30pF
UP-0668	X101	1706076	1	XTAL	TD308C 32MHz
UP-0668	X102	1702597	1	XTAL	KF38G 32.768KHz

UP-0485 DRAM BD

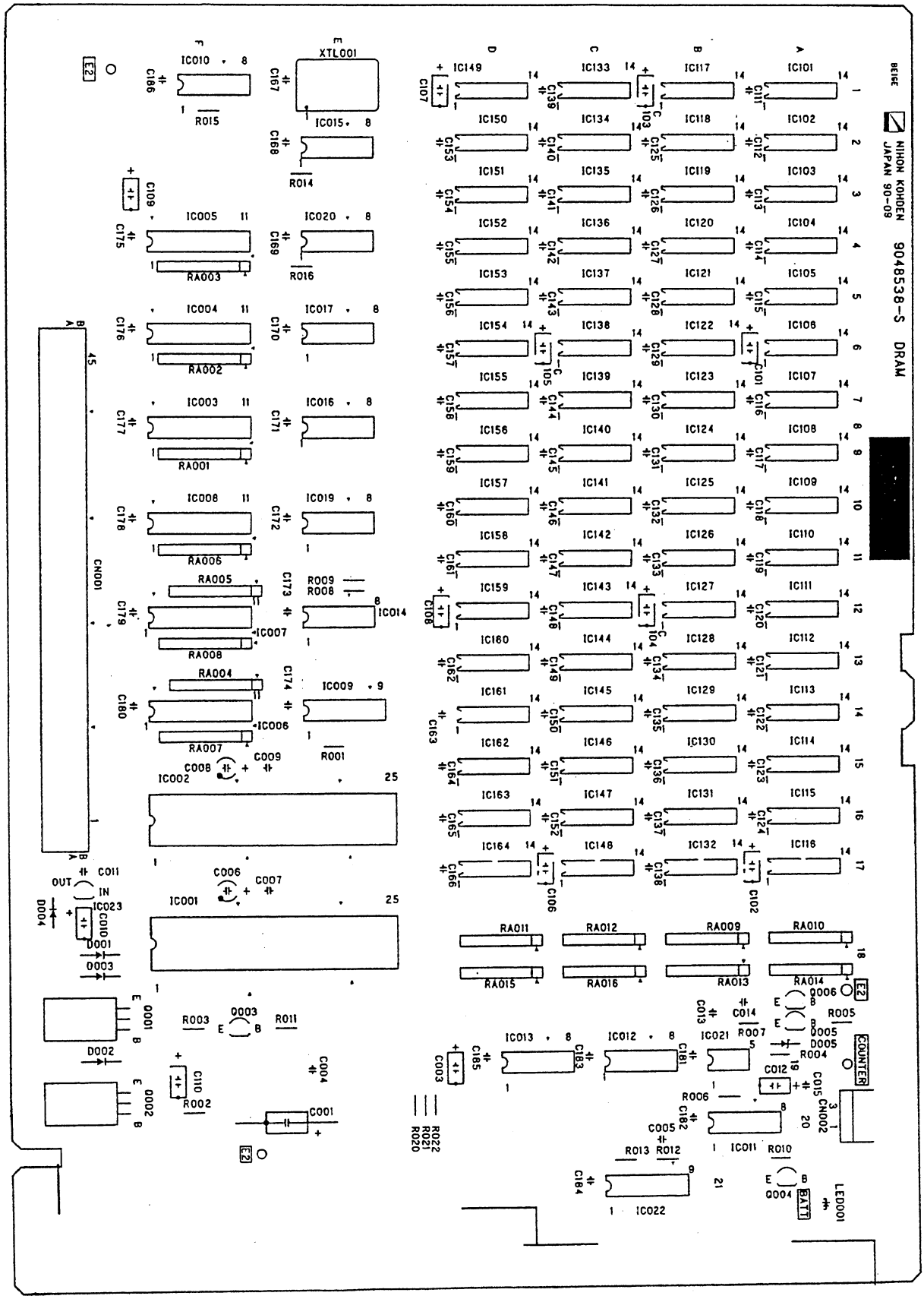
UP-0485	CN001	5427939	1	PCN	PCN10EA-90P-2.54DS(05)
UP-0485	CN002	5431061	1	PCN	IL-3P-S3FP2-1
UP-0485	C001	3801717	1	ECO2	ECEB1CG101S 100uF/16V
UP-0485	C003	4312503	1	TC04	ECSZ35HS6R8B 6.8uF/35V
UP-0485	C004	4317525	1	CEC1	TP D55Y5V1H 104Z 5-W
UP-0485	C005	4315144	1	FLC1	ECQ-B 1H 682JZ3 0.0068uF
UP-0485	C006	4312557	1	TC04	204M2002 106MB(10uF/20V)
UP-0485	C007	4317525	1	CEC1	TP D55Y5V1H 104Z 5-W
UP-0485	C008	4312557	1	TC04	204M2002 106MB(10uF/20V)
UP-0485	C009	4317525	1	CEC1	TP D55Y5V1H 104Z 5-W
UP-0485	C010	4312503	1	TC04	ECSZ35HS6R8B 6.8uF/35V
UP-0485	C011	4317525	1	CEC1	TP D55Y5V1H 104Z 5-W
UP-0485	C012	4312503	1	TC04	ECSZ35HS6R8B 6.8uF/35V
UP-0485	C013-C014	4317525	2	CEC1	TP D55Y5V1H 104Z 5-W
UP-0485	C015	4317597	1	CEC2	DD05-989B 101K500 (100pF)
UP-0485	C101-C110	4312503	10	TC04	ECSZ35HS6R8B 6.8uF/35V
UP-0485	C111-C186	4317525	76	CEC1	TP D55Y5V1H 104Z 5-W
UP-0485	D001-D003	0910008	3	DP	SR1FM8 800mA 400V
UP-0485	D004	4320031	1	D	1S2076ATE
UP-0485	D005	4325071	1	ZD1	HZ3C3TE (3.3-3.5V)
UP-0485	IC001-IC002	1208613	2	CPU	MB1431AP
UP-0485	IC003-IC005	1303769	3	MIC	uPD74HCT240C
UP-0485	IC006-IC007	1303822	2	MIC	uPD74HCT640C
UP-0485	IC008	1303778	1	MIC	uPD74HCT244C
UP-0485	IC009	1302984	1	MIC	uPD74HC138C(HD74HC138P)

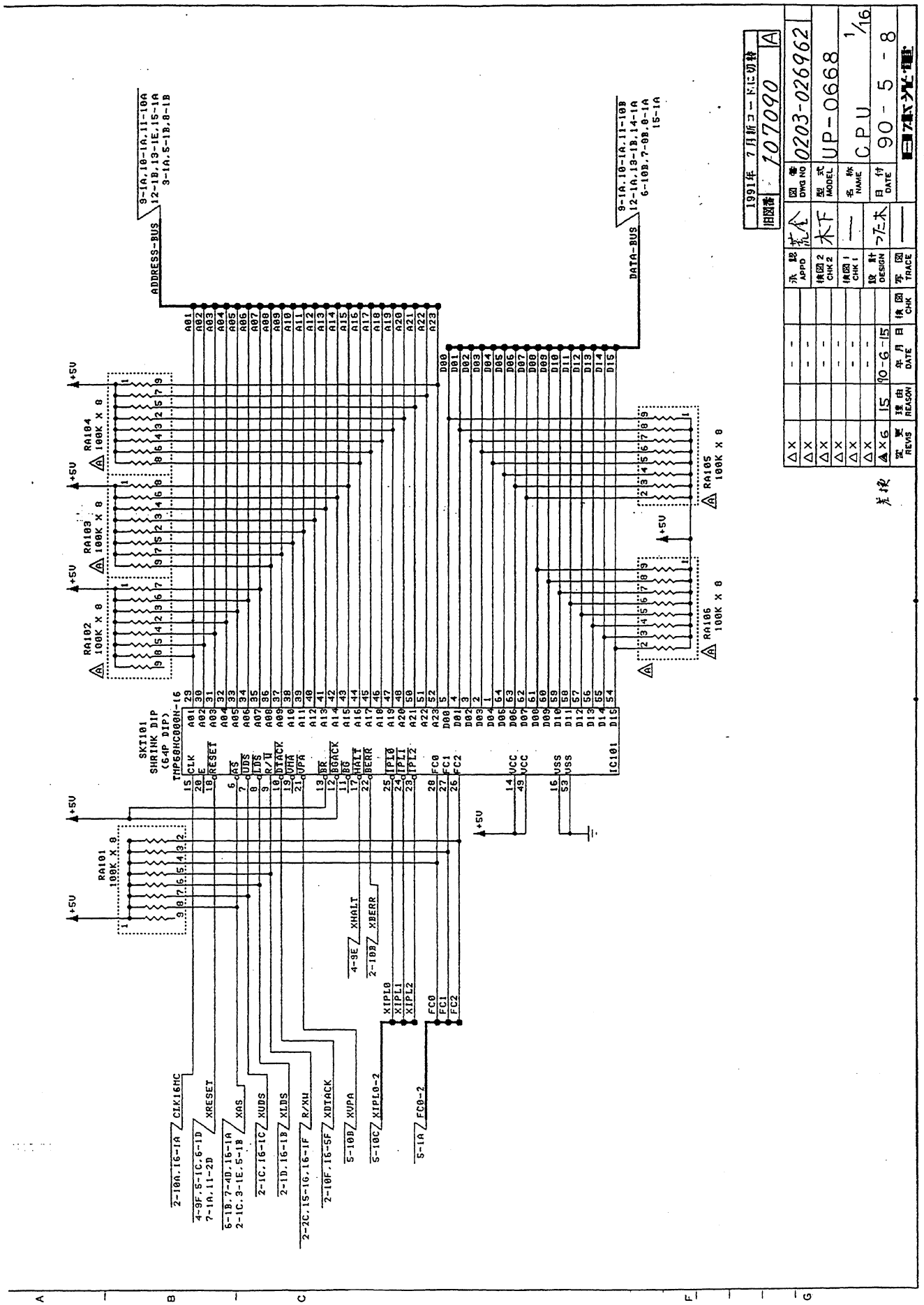
ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-0485	IC010	1205135	1	TIC	74F74PC
UP-0485	IC011	1302948	1	MIC	uPD74HC08C(HD74HC08P)
UP-0485	IC012	1302921	1	MIC	uPD74HC02C(HD74HC02P)
UP-0485	IC013	1300237	1	MIC	MC14013BCP (CD4013BE)
UP-0485	IC014	1205117	1	TIC	74F08PC
UP-0485	IC015	1303564	1	MIC	HD74HC164P(uPD74HC164C)
UP-0485	IC016	1205518	1	TIC	74F00PC
UP-0485	IC017	1202628	1	TIC	SN74LS01
UP-0485	IC019	1302975	1	MIC	HD74HC32P(uPD74HC32C)
UP-0485	IC020	1303564	1	MIC	HD74HC164P(uPD74HC164C)
UP-0485	IC021	1253207	1	AIC	TL7705CP Voltage Detector
UP-0485	IC022	1301432	1	MIC	MC14521BCP
UP-0485	IC023	4346529	1	REG	uPC78L12J-T
UP-0485	LED001	1102246	1	LED	GL-3AR2 Red
UP-0485	Q003-Q006	4335051	4	TRC	2SC1345KDTZ
UP-0485	RA001-RA008	4342783	8	RM	EXB-F9 E 104JYV
UP-0485	RA009-RA016	4343559	8	RM	EXB-F8 V 470JYV
UP-0485	XTL001	1706076	1	XTAL	TD308C 32MHz

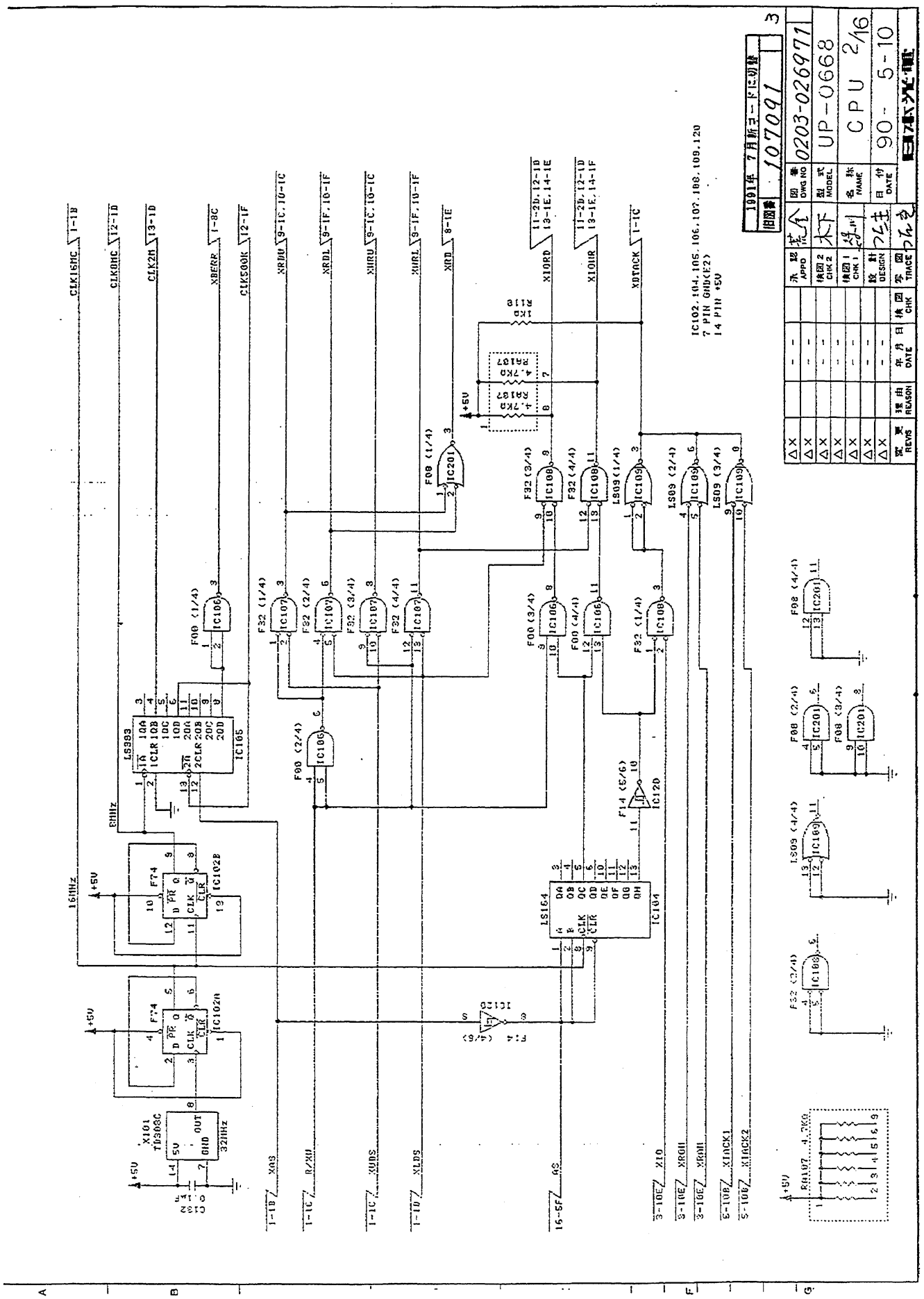
UP-0668 CPU board

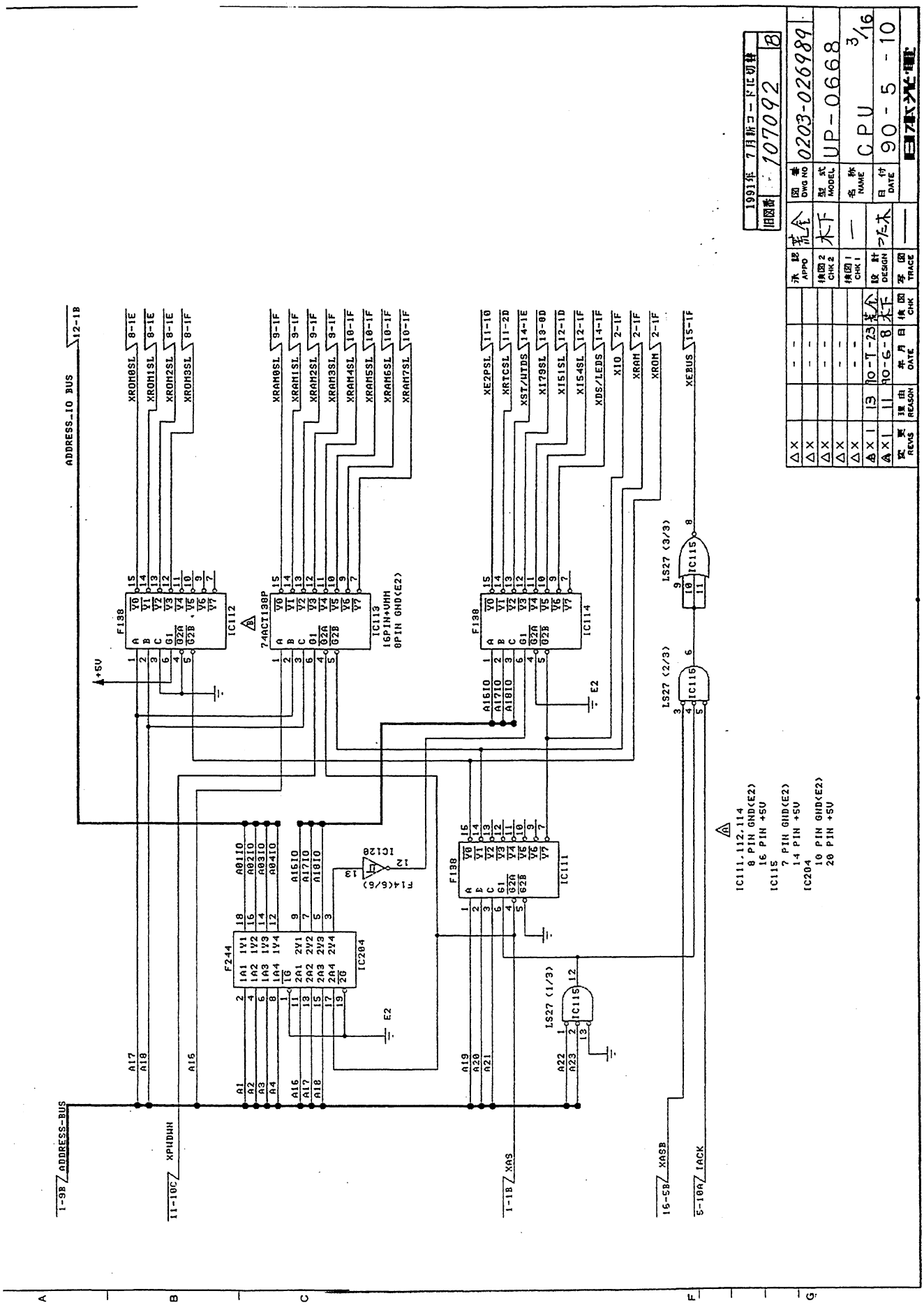


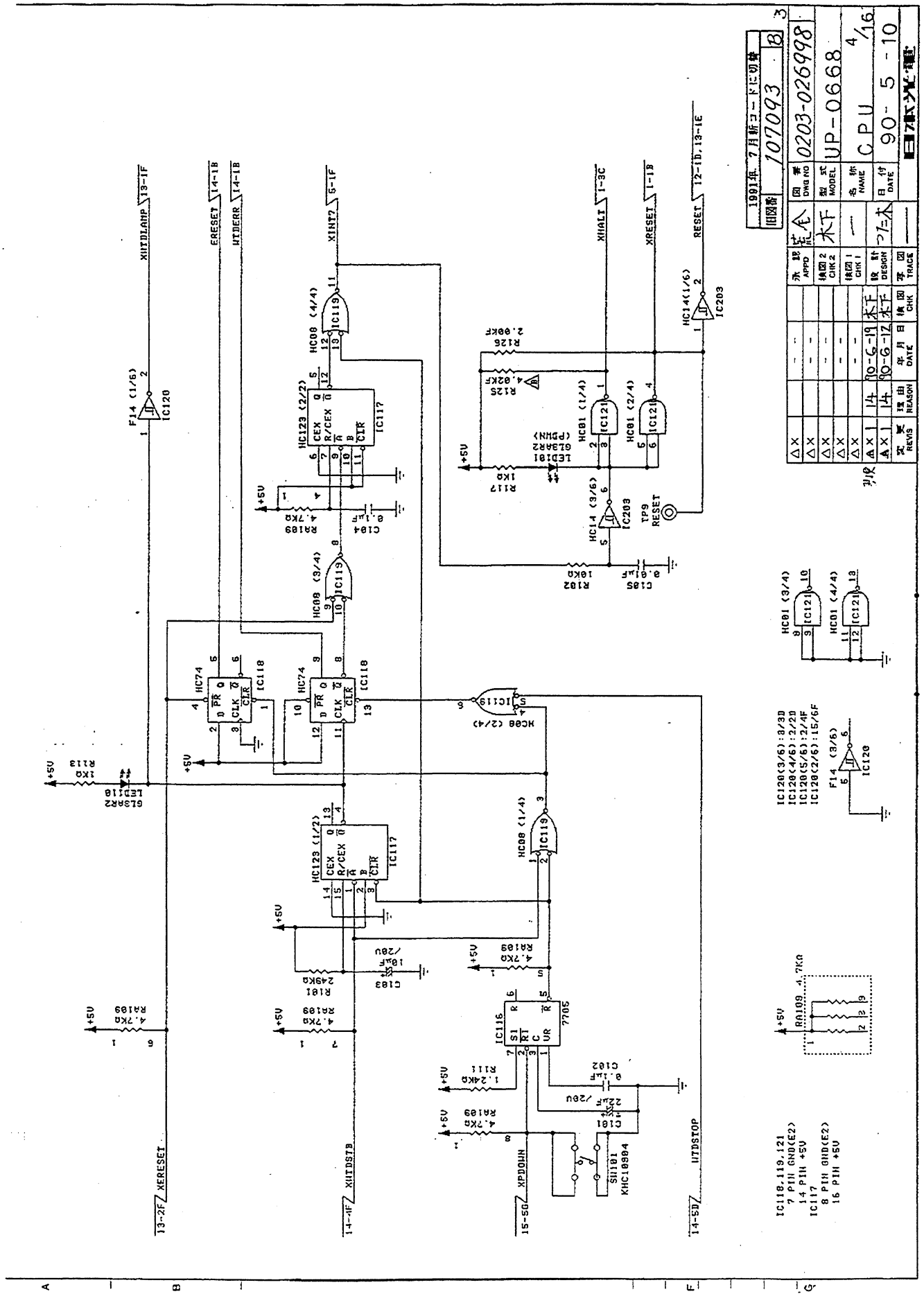
UP-0485 DRAM board

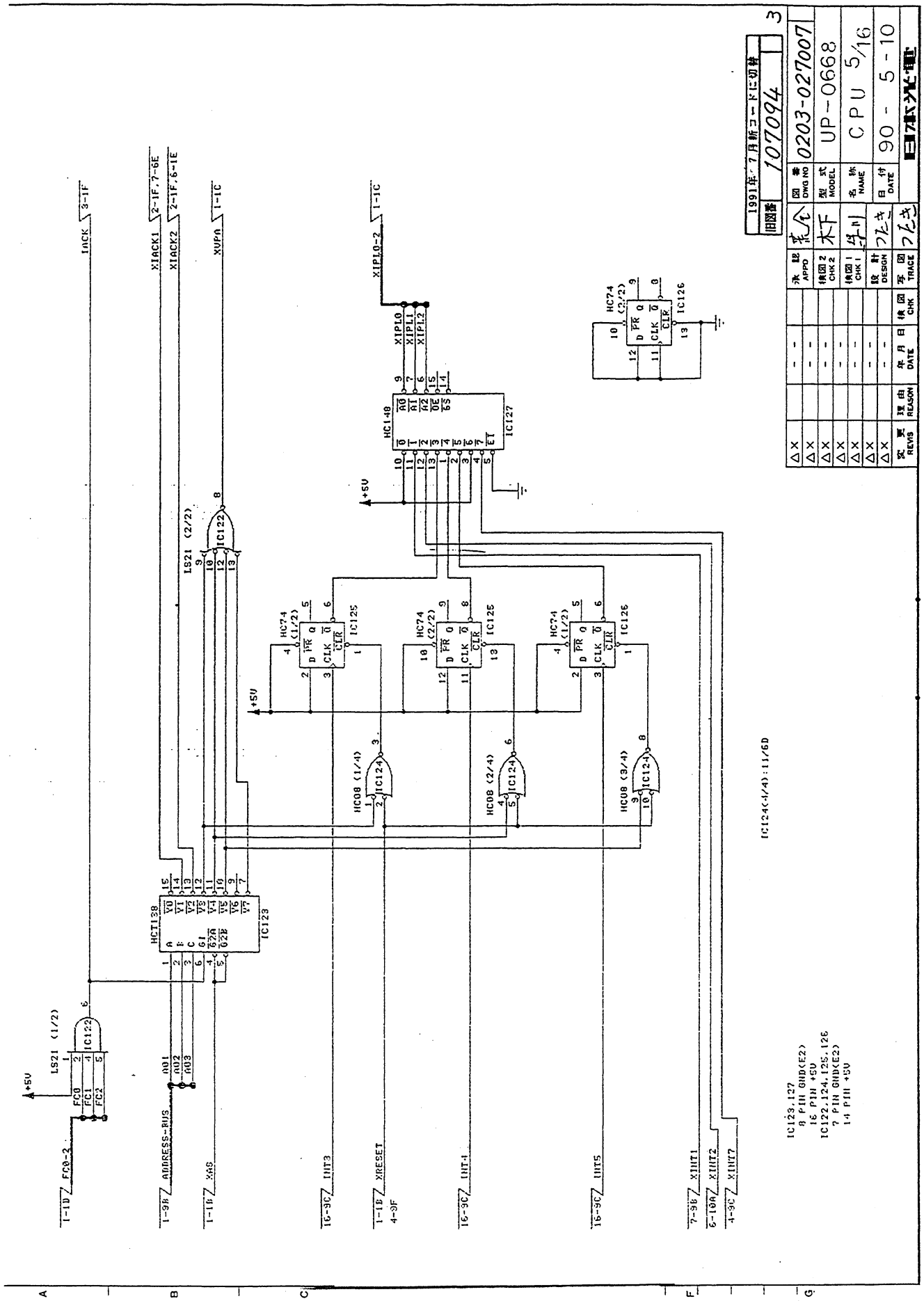


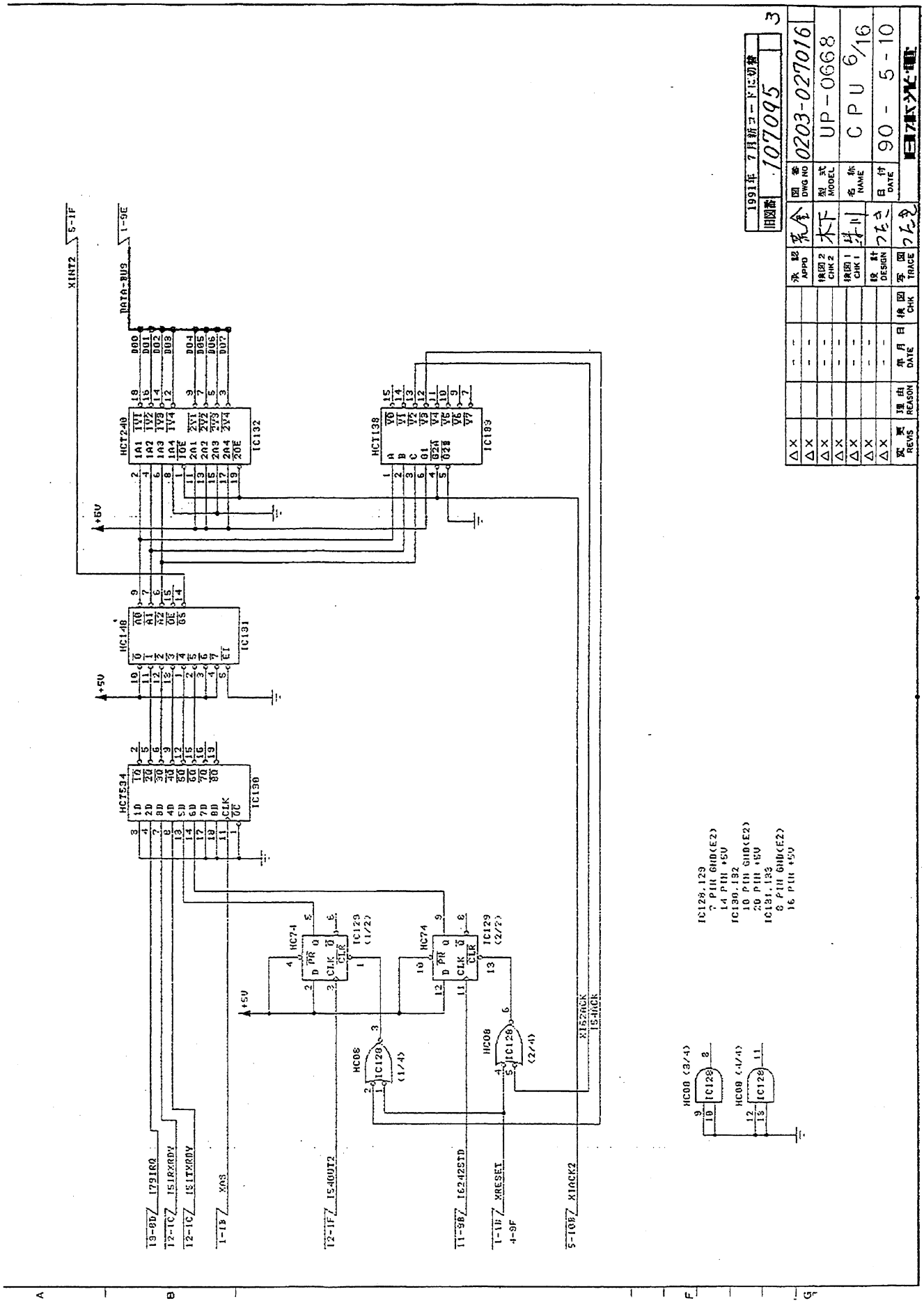

SK101
SHRINK DIP
(64P DIP)
TMP68HC000N-16
RA101 100K X 9
RA102 100K X 8
RA103 100K X 8
RA104 100K X 8
RA105 100K X 8
RA106 100K X 8
IC101
+5V
ADDRESS-BUS
DATA-BUS
A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23
D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15
CLK
E
RESET
AS
UDS
LDS
R/W
DTACK
VMA
VPA
BR
BGACK
BG
HALT
BERR
IPL0
IPL1
IPL2
FC0
FC1
FC2
VCC
VSS
XRESET
XAS
XUDS
XLDS
R/XW
XDTACK
XVPA
XHALT
XBERR
XIPL0-2
FC0-2
CLK16MC
1991年 7月新コードに切替
旧図番 107090 A
0203-026962
UP-0668
CPU
90-5-8
1/16

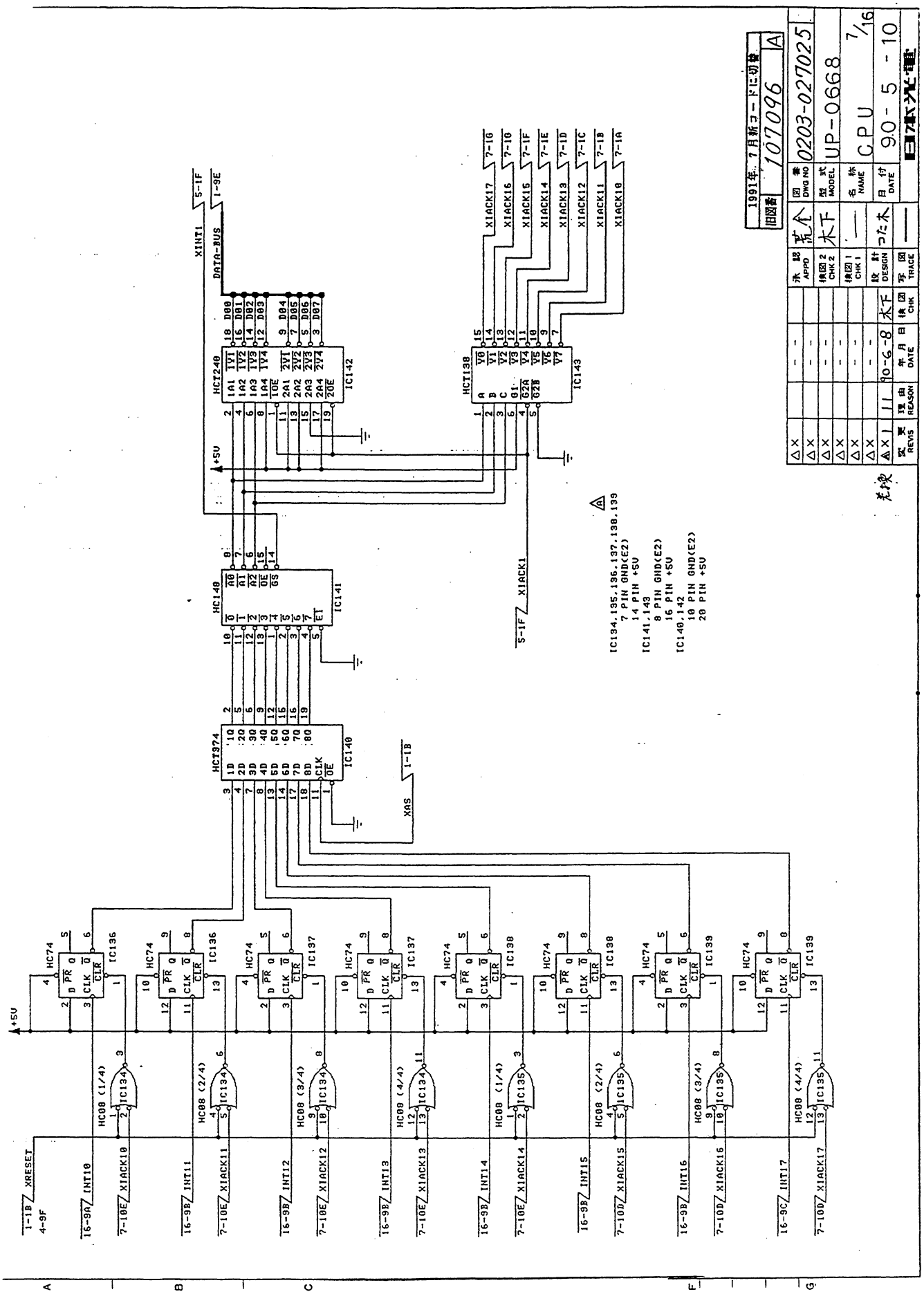

CPU 2/16
UP-0668
0203-026971
90-5-10
107091
IC102.104.105.106.107.108.109.120
7 PIN GND(E2)
14 PIN +5V
X101 TD308C 32MHz
16MHz
8MHz
4MHz
CLK16MC
CLK8MC
CLK2M
CLK500K
XBERR
XRMW
XRDL
XRDU
XUDL
XRD
X10RD
X10WR
X10ACK
XDS
R/XW
XUDS
XLDS
AS
X10
XRQII
XRQUI
XIACK1
XIACK2
IC165
IC164
IC120
IC102A
IC102B
IC102C
IC106
IC107
IC108
IC109
IC201
R4107 4.7KΩ
R4108 2KΩ
+5V

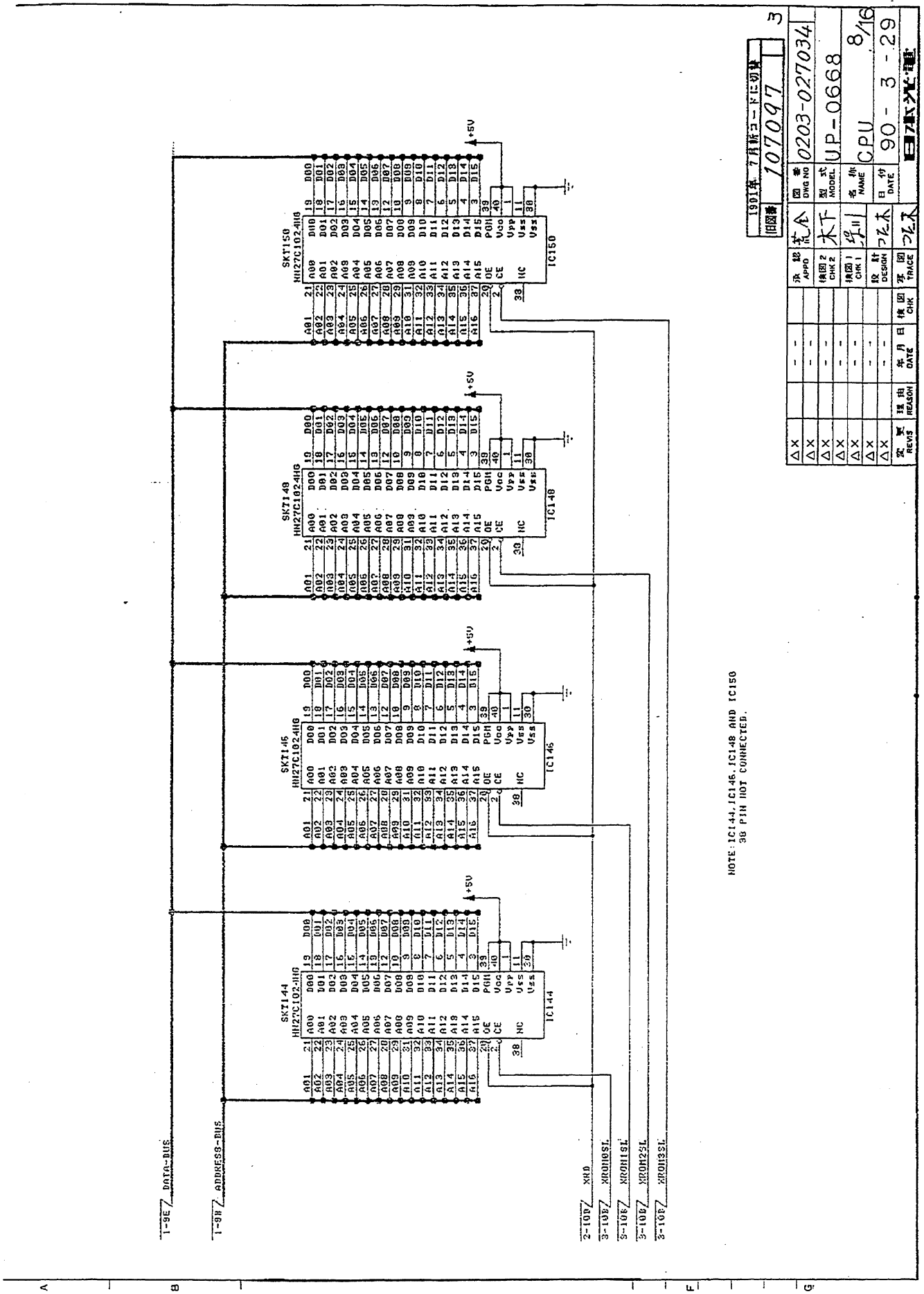

ADDRESS_IO BUS
F138
74ACT138P
F244
F14(6/6)
IS27 (1/3)
IS27 (2/3)
IS27 (3/3)
IC111,112,114
8 PIN GND(E2)
16 PIN +5V
IC115
7 PIN GND(E2)
14 PIN +5V
IC204
10 PIN GND(E2)
20 PIN +5V
XPUDWN
XAS
XASB
IACK
XEBUS
XROH
XIO
XRAH
XDS/LEDS
XI54SL
XI51SL
XI79SL
XST/UTDS
XRTCSL
XE2PSL
XRAM7SL
XRAM6SL
XRAM5SL
XRAM4SL
XRAM3SL
XRAM2SL
XRAM1SL
XRAM0SL
XROM3SL
XROM2SL
XROM1SL
XROM0SL
+5V
E2
1991年 7月新コード化切替
旧図番 107092 B
0203-026989
UP-0668
CPU
3/16
90-5-10
日本光電

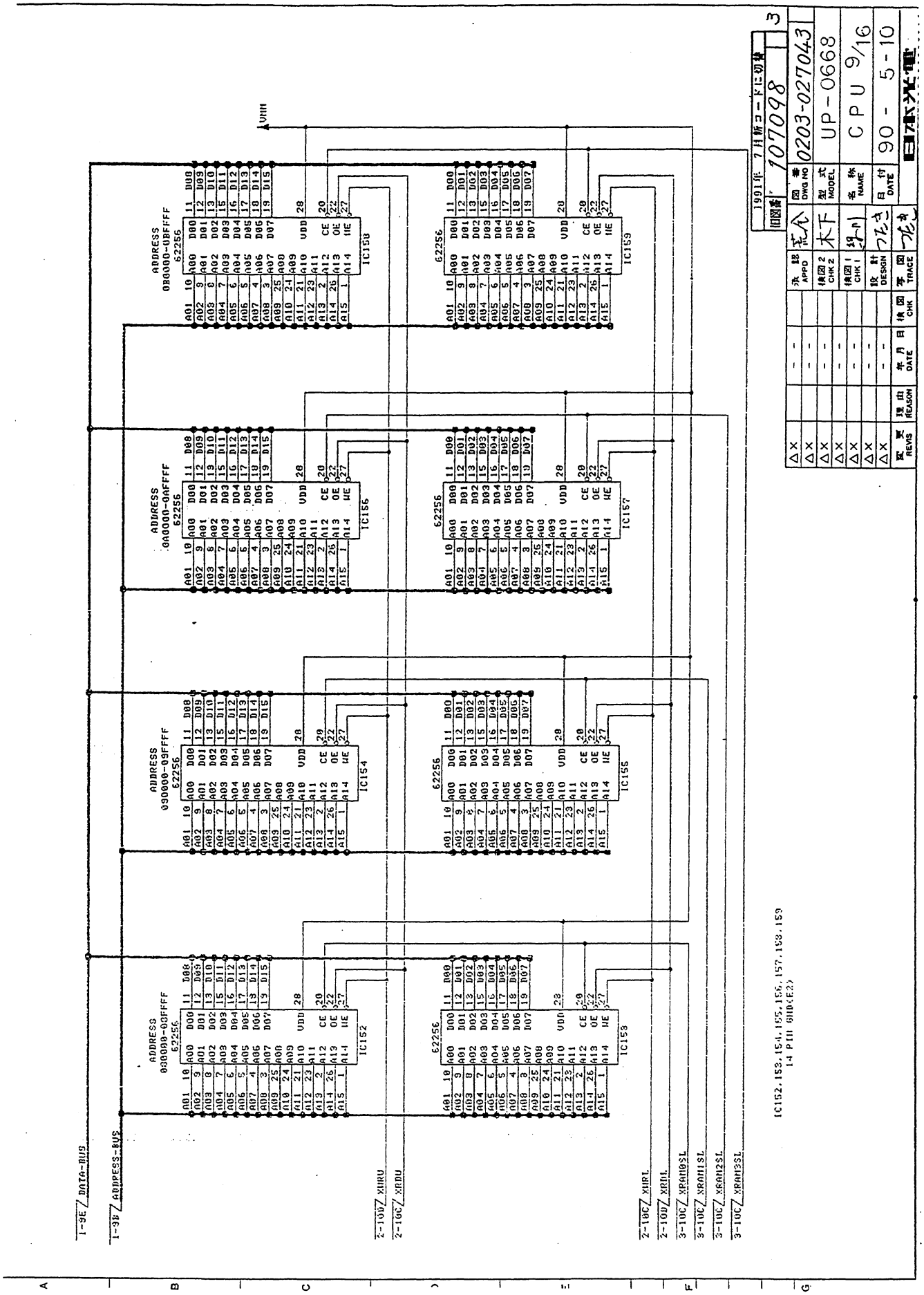

CPU
UP-0668
0203-026998
90-5-10
4/16
XHITDLAMP
ERESET
HTDERR
XINT2
XHALT
XRESET
RESET
XERESET
XHITDSTB
XPDOWN
HTDSTOP
+5V
IC118,119,121
7 PIN GND(E2)
14 PIN +5V
IC117
8 PIN GND(E2)
16 PIN +5V

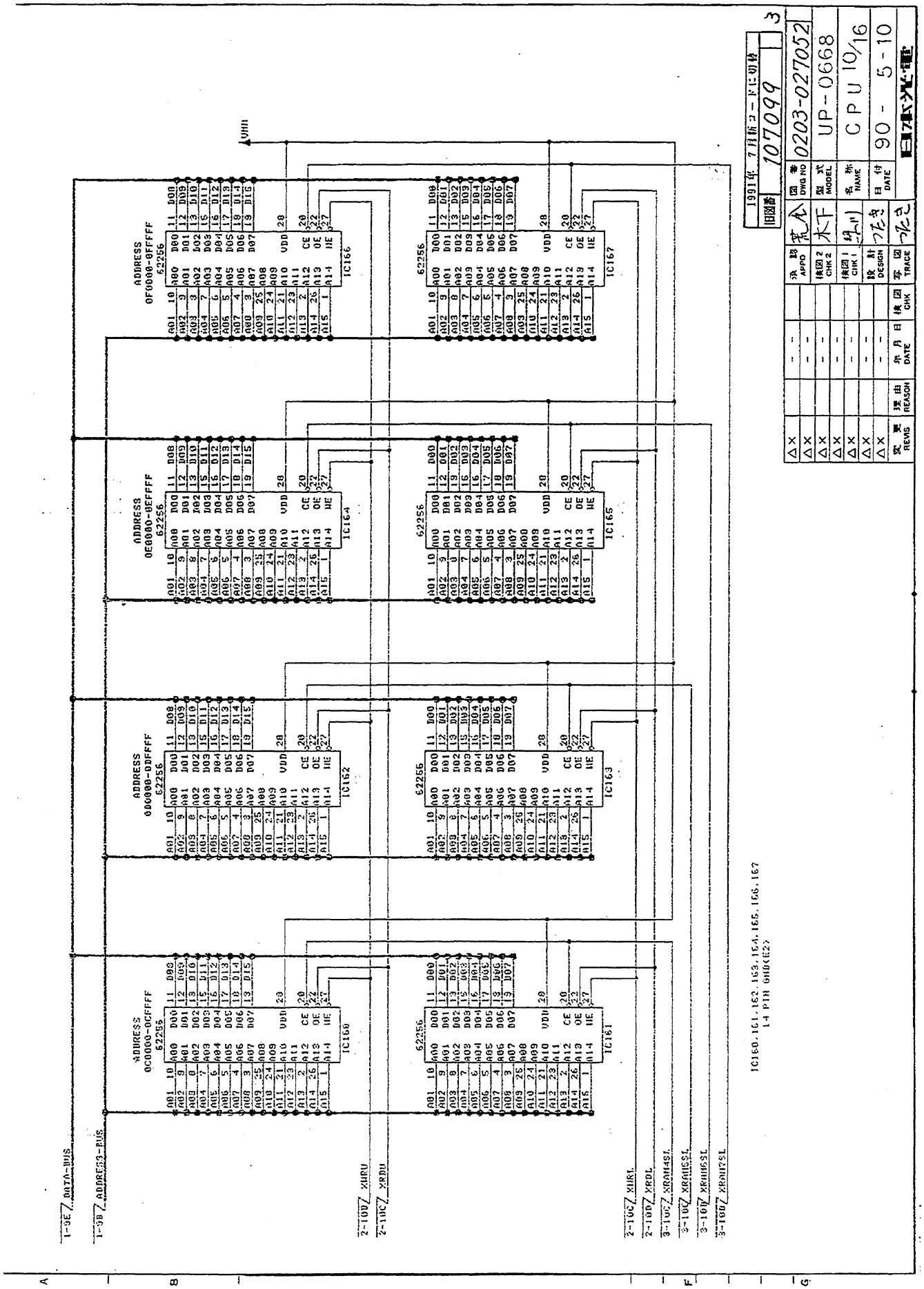

IACK
XIACK1
XIACK2
XVPA
XIPL0-2
XIPL0
XIPL1
XIPL2
LS21 (2/2)
LS21 (1/2)
IC122
IC123
IC124
IC125
IC126
IC127
HCT138
HC148
HC74
HC08 (1/4)
HC08 (2/4)
HC08 (3/4)
+5V
FC0-2
FC0
FC1
FC2
A01
A02
A03
ADDRESS-BUS
XAS
XRESET
IHT3
IHT4
IHT5
XIHT1
XIHT2
XIHT7
IC123,127
8 PIN GND(E2)
16 PIN +5V
IC122,124,125,126
7 PIN GND(E2)
14 PIN +5V
IC124(1/4):11/6D
1991年7月新コード已切替
旧図番
1070947
3
0203-027007
UP-0668
CPU 5/16
90 - 5 - 10
日本光電

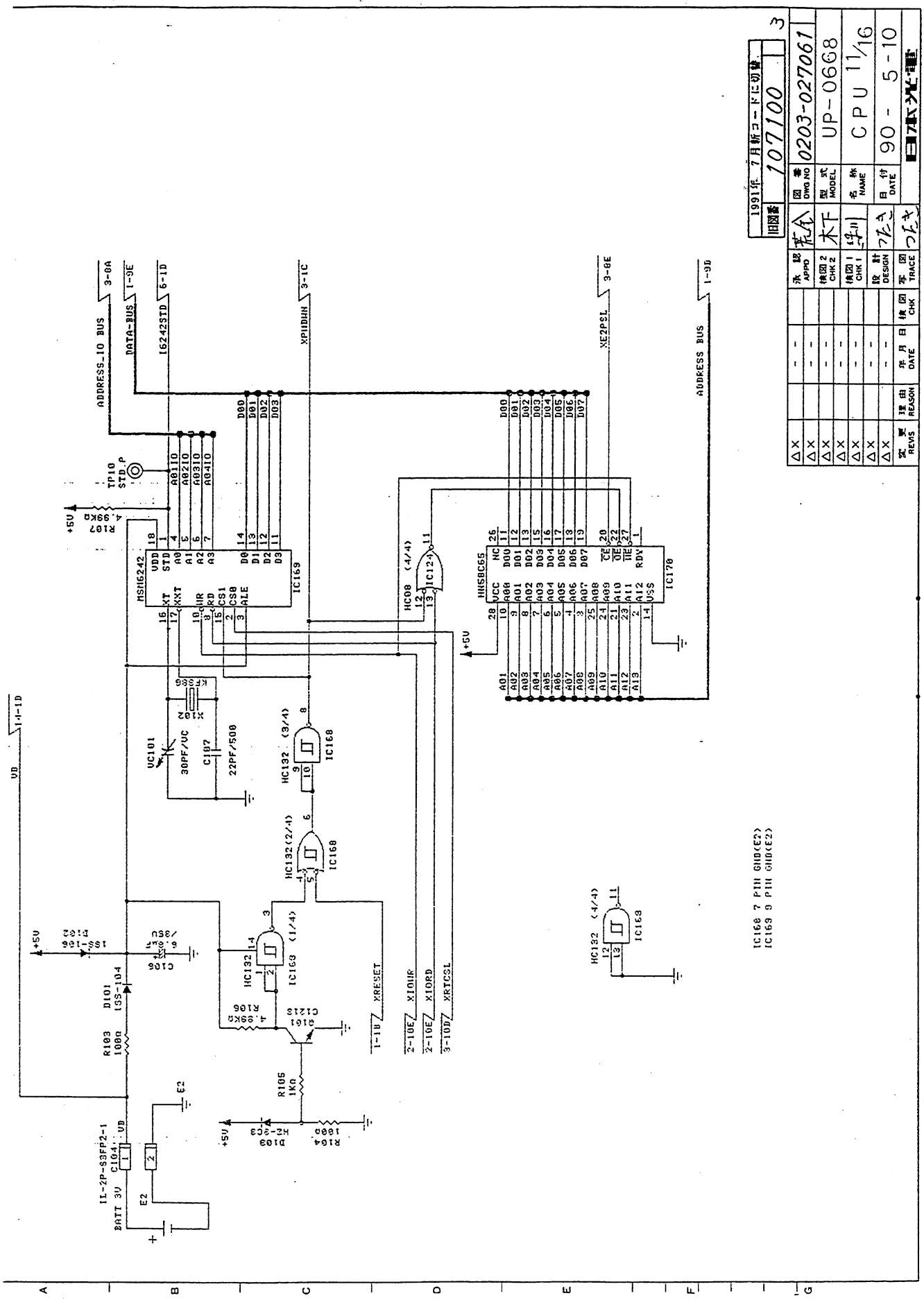

XINT2
DATA-BUS
+5V
HCT240
IC132
HCT138
IC133
HC148
IC131
HCT534
IC130
HC74
IC129
HC08
IC128
XRESET
X16CK2
X8CK
1991年 7月新コード IC切替
旧図番 107095
0203-027016
UP-0668
CPU 6/16
90 - 5 - 10
日東光電

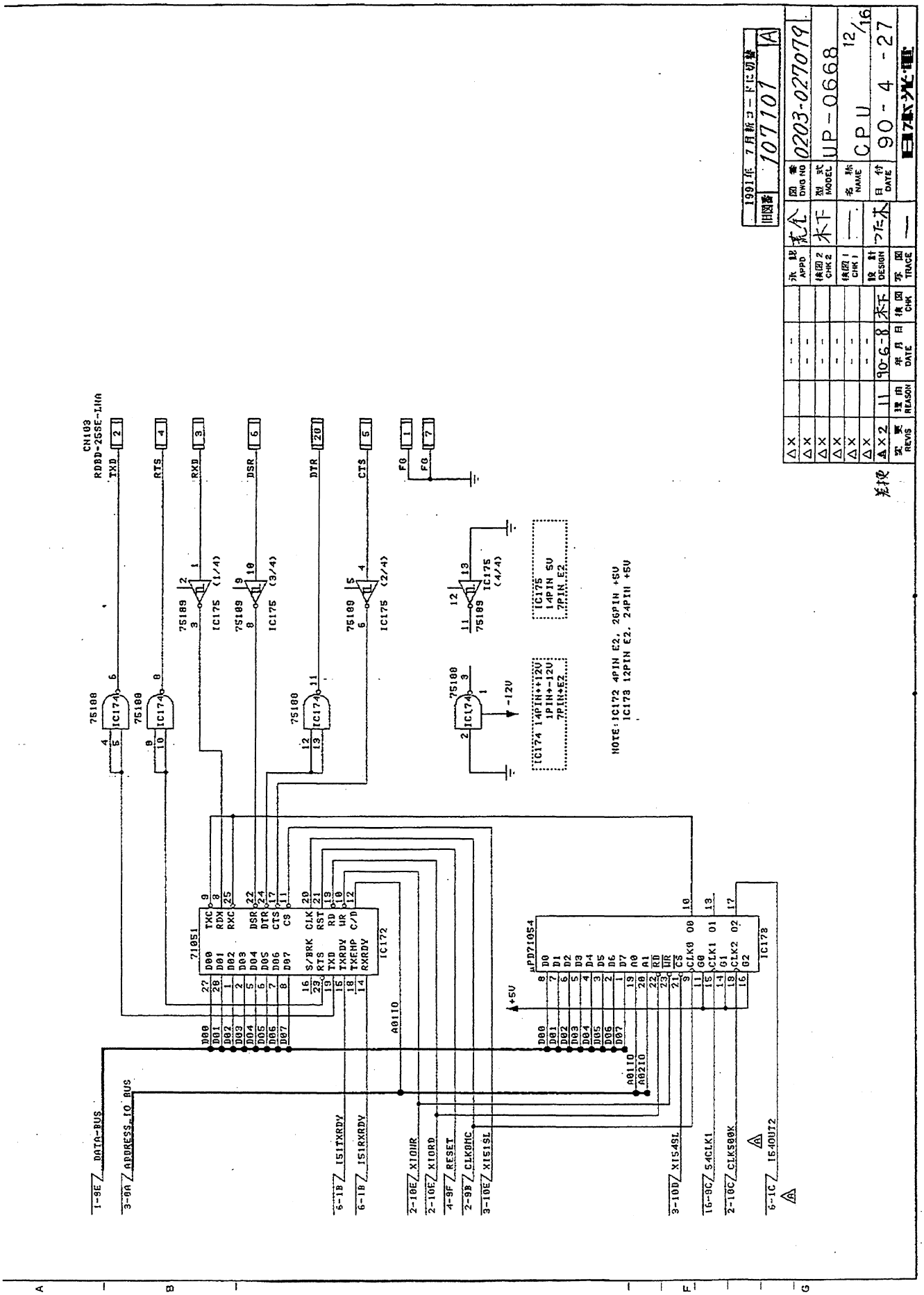

XINT1
DATA-BUS
+5V
HCT240
HCT374
HC140
HCT138
HC74
HC08 (1/4)
HC08 (2/4)
HC08 (3/4)
HC08 (4/4)
IC134,135,136,139
7 PIN GND(E2)
14 PIN +5V
IC141,143
8 PIN GND(E2)
16 PIN +5V
IC140,142
10 PIN GND(E2)
20 PIN +5V
XRESET
INT10
INT11
INT12
INT13
INT14
INT15
INT16
INT17
XIACK10
XIACK11
XIACK12
XIACK13
XIACK14
XIACK15
XIACK16
XIACK17
XIACK1
XAS
1991年 7月新コードに切替
旧図番 107096 A
0203-027025
UP-0668
CPU
90-5-10
7/16

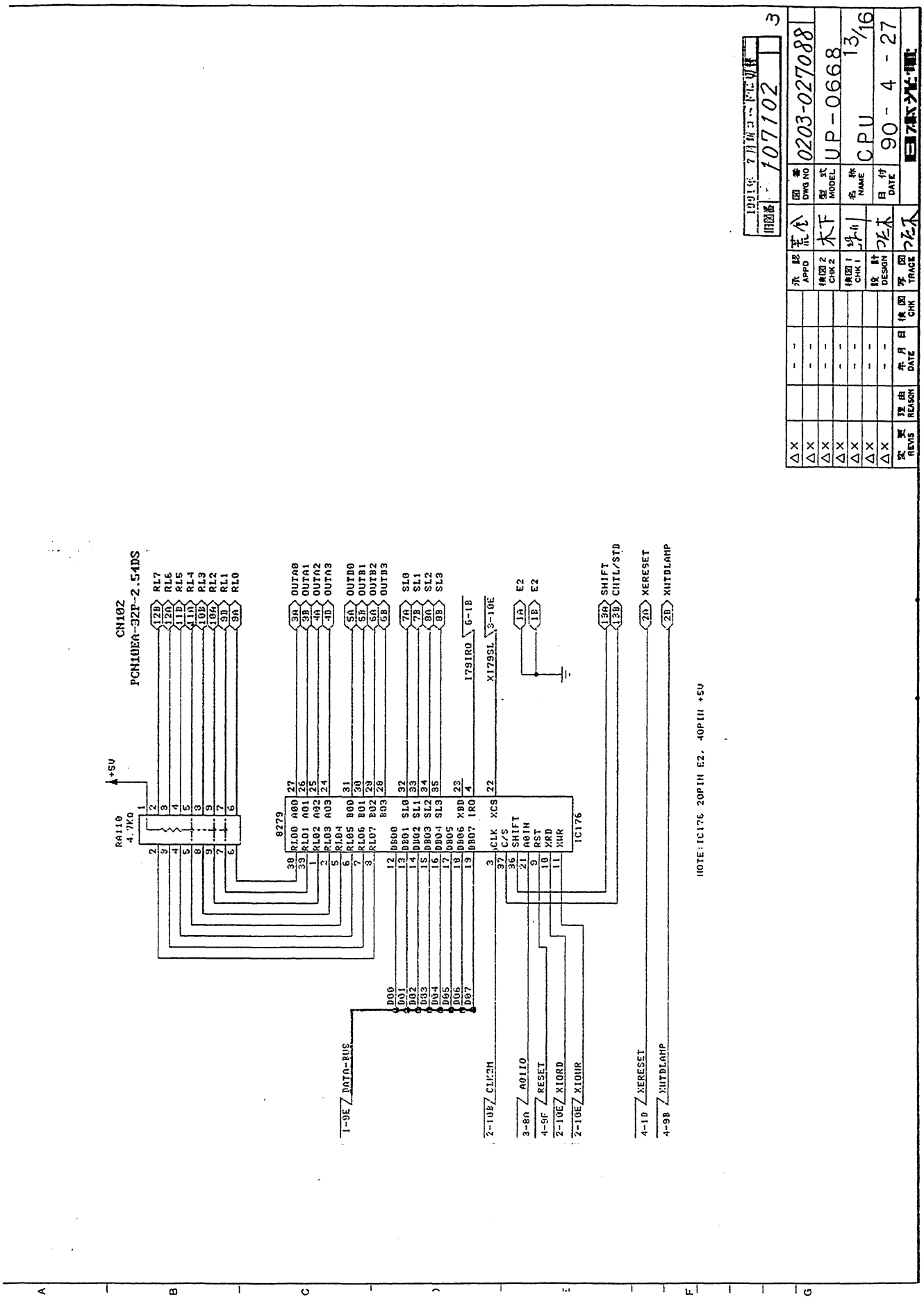

DATA-BUS
ADDRESS-BUS
XRD
XROM19L
XROM18L
XROM25L
XROM13L
IC144
IC145
IC146
IC148
IC150
+5V
NOTE: IC144, IC146, IC148 AND IC150
36 PIN NOT CONNECTED.
1901年 7月版コードに切換
旧図番 107097
3
8/16
0203-027034
UP-0668
CPU
90 - 3 - 29

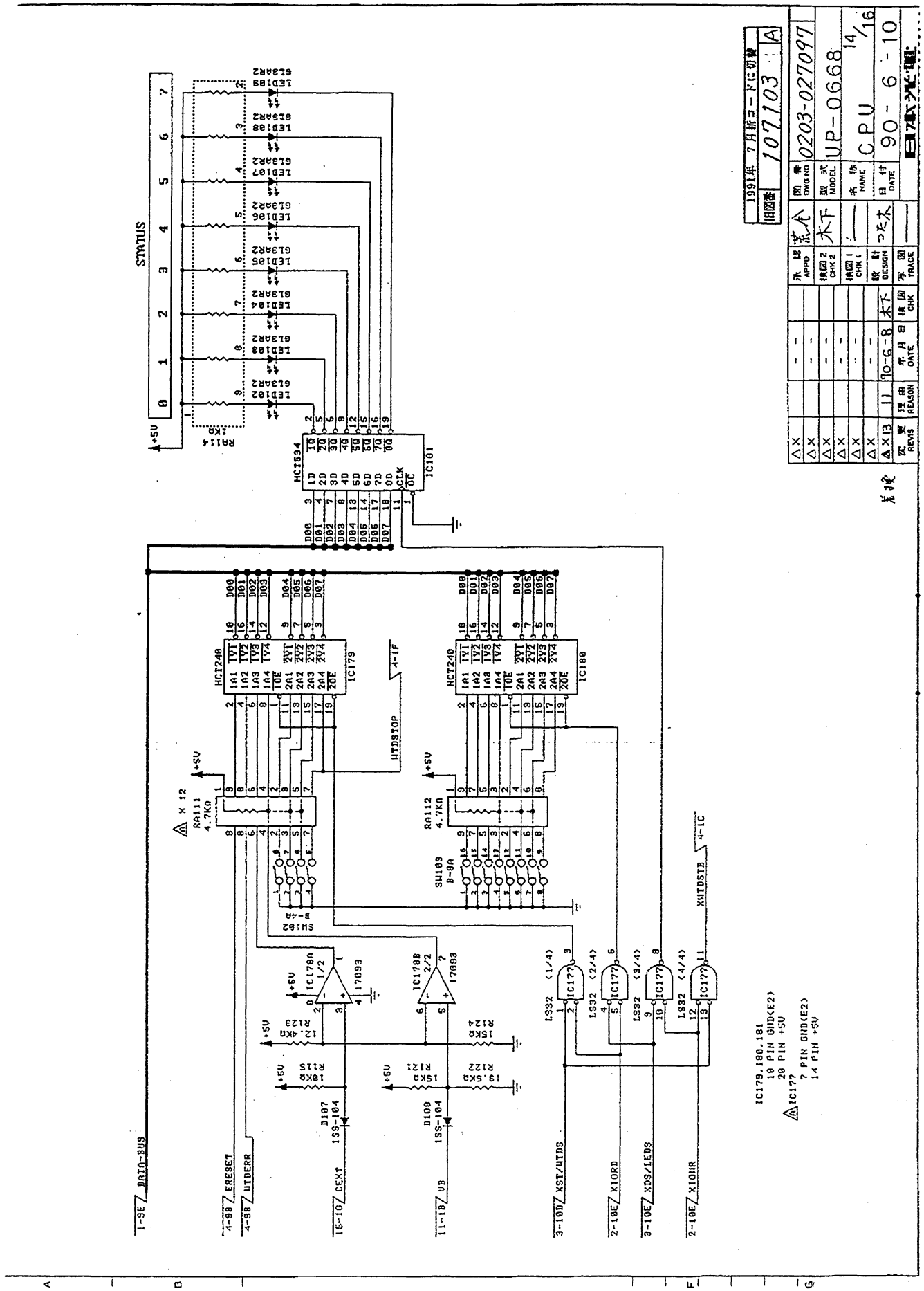

1-9E DATA-BUS
1-9B ADDRESS-BUS
2-10D XHRU
2-10C XRDU
2-10C XHRL
2-10D XRDL
3-10C XRAM0SL
3-10C XRAM1SL
3-10C XRAM2SL
3-10C XRAM3SL
IC152, 153, 154, 155, 156, 157, 158, 159
14 PIN SOCKET
ADDRESS 080000-08FFFF
ADDRESS 090000-09FFFF
ADDRESS 0A0000-0AFFFF
ADDRESS 0B0000-0BFFFF
62256
IC152
IC153
IC154
IC155
IC156
IC157
IC158
IC159
VHH
1991年 7月新コードに切換
旧図番 107098
図番 DWG NO 0203-027043
型式 MODEL UP-0668
名称 NAME CPU 9/16
日付 DATE 90 - 5 - 10
日本光電

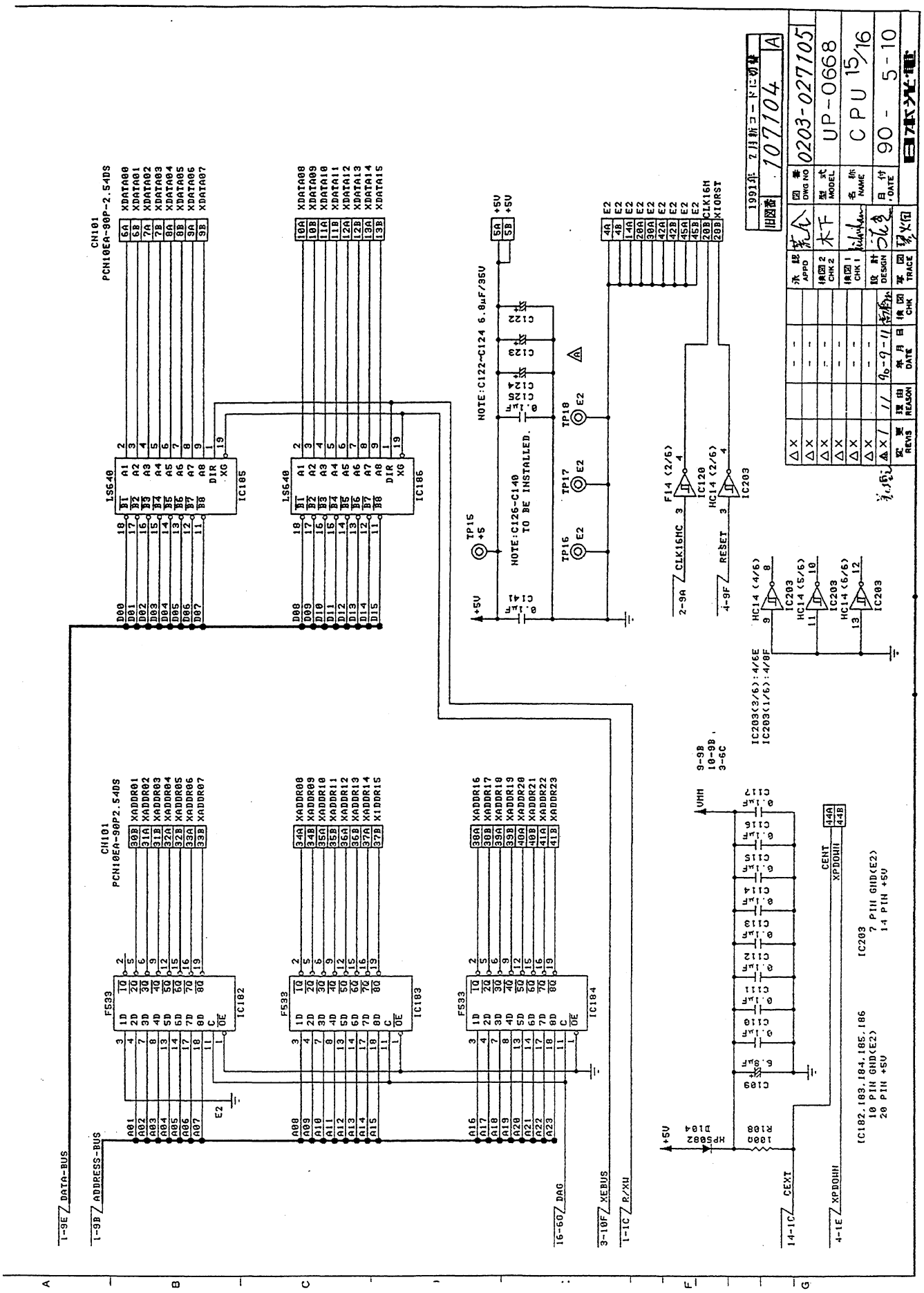

1-9E DATA-BUS
1-9B ADDRESS-BUS
2-10D XMRU
2-10C XRDU
2-10G XMRL
2-10G XRDL
3-10G XRAM4L
3-10G XRAM3L
3-10G XRAM2L
3-10G XRAM1L
IC160, 161, 162, 163, 164, 165, 166, 167
1-4 PIN GND(E2)
ADDRESS 0C0000-0CFFFF
ADDRESS 0D0000-0DFFFF
ADDRESS 0E0000-0EFFFF
ADDRESS 0F0000-0FFFFF
62256
IC160
IC161
IC162
IC163
IC164
IC165
IC166
IC167
VDD
VSS
1991年 7月作コ-FIC切替
旧図番 107099
0203-027052
UP-0668
CPU 10/16
90 - 5 - 10

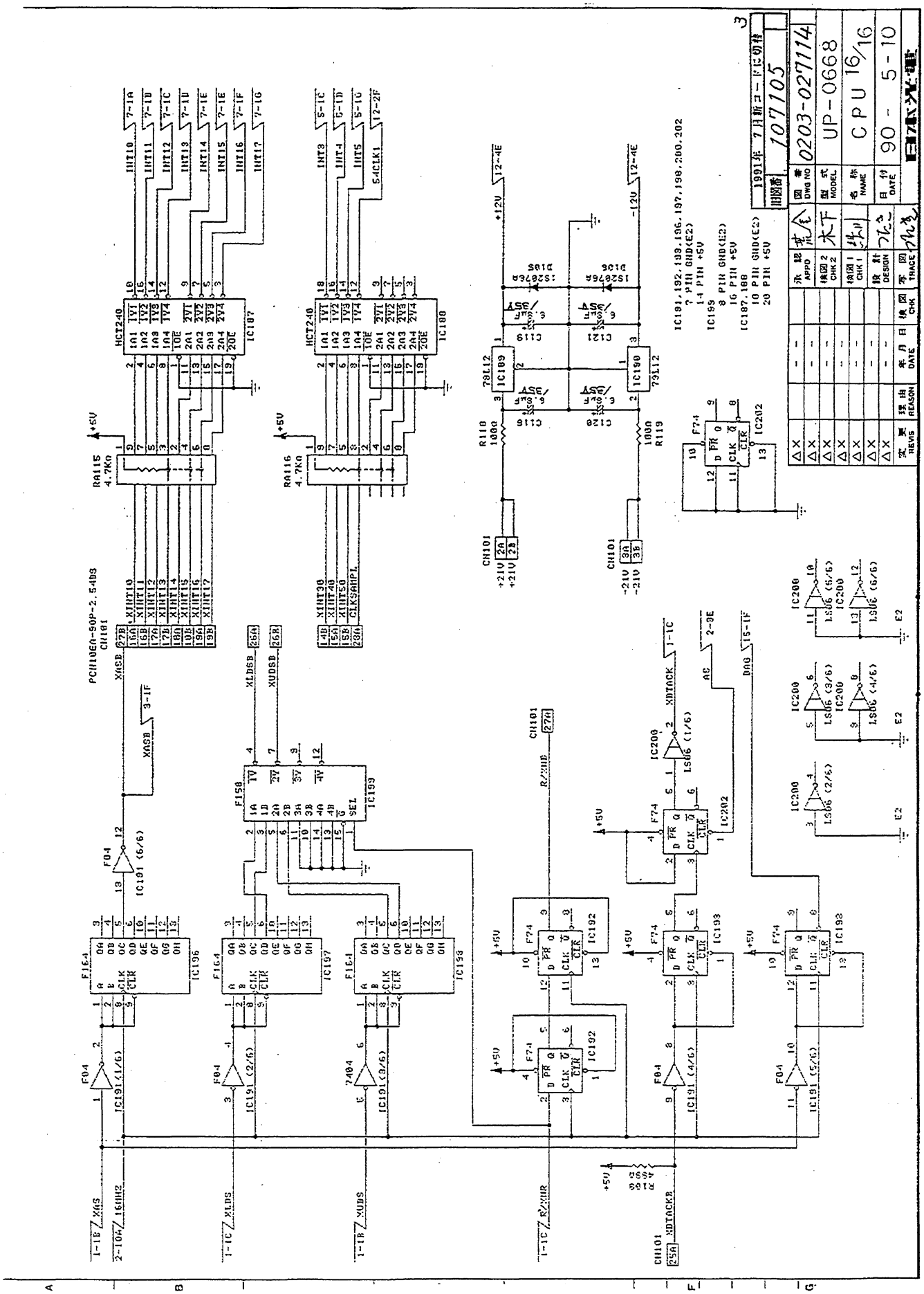

1991年 7月新コードに切替
旧図番 107100
3
0203-027061
UP-0668
CPU 11/16
90 - 5 - 10
日本光電
ADDRESS_IO BUS
DATA-BUS
I6242STD
XPIUDHN
XE2PSL
ADDRESS BUS
MSM6242
IC169
HC08 (4/4)
IC124
MM58C65
IC170
HC132 (3/4)
HC132(2/4)
HC132 (1/4)
IC168
VC101
30PF/VC
C107
22PF/500
X102
C106
R103
100Ω
D101
1SS-104
R106
4.99KΩ
C121S
R105
1KΩ
R104
180Ω
D103
RZ-4C3
E2
IL-2P-S3FP2-1
C104
BATT 3V
XRESET
XIOWR
XIORD
XRTCSL
IC168 7 PIN GND(E2)
IC169 9 PIN GND(E2)

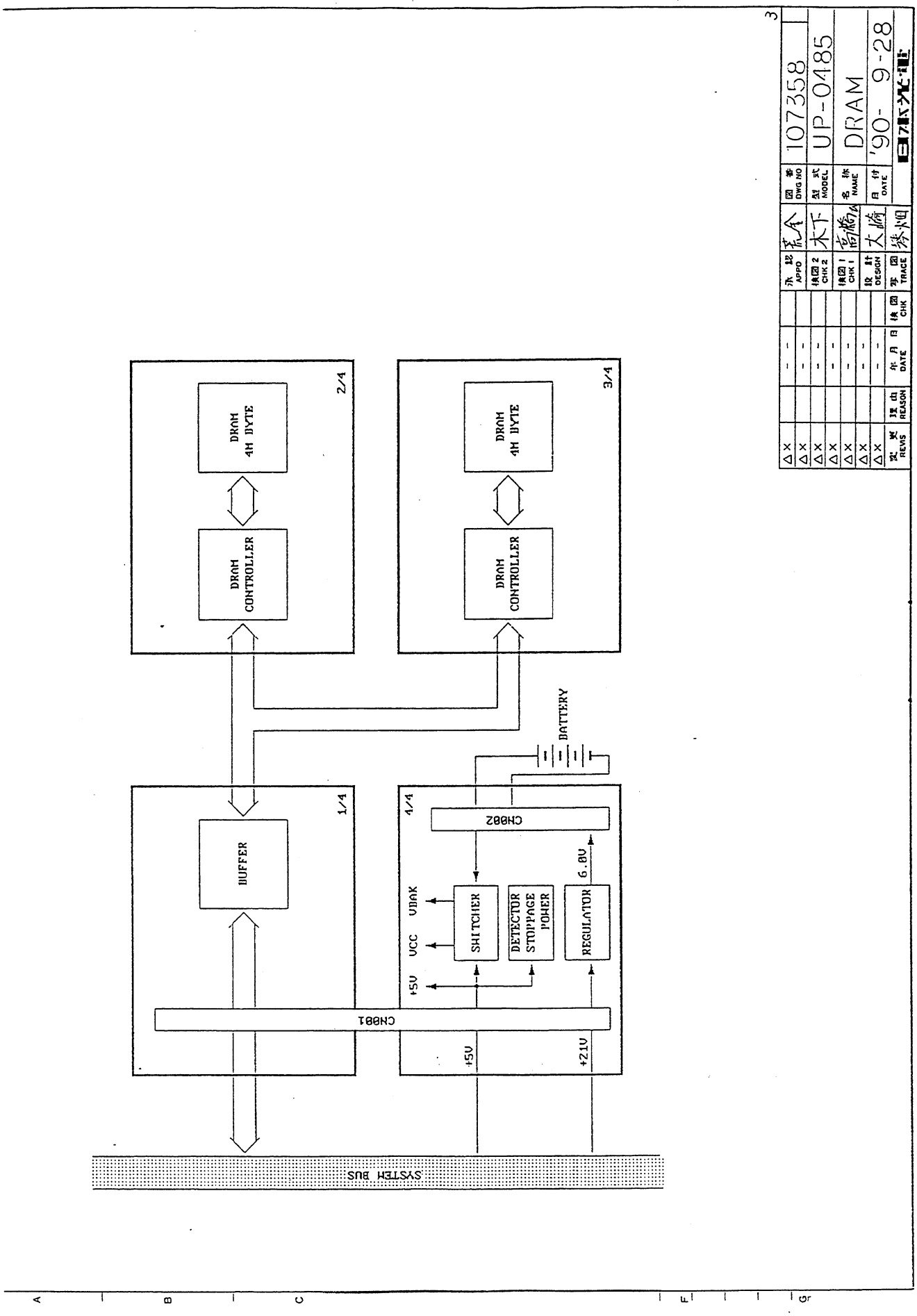

CN103
RDBD-25SE-LHA
TXD
RTS
RXD
DSR
DTR
CTS
FG
75188
75189
IC174
IC175 (1/4)
IC175 (2/4)
IC175 (3/4)
IC175 (4/4)
IC175 14PIN E2, 7PIN E2
IC174 14PIN→+12V 1PIN→-12V 7PIN→E2
-12V
NOTE:IC172 40PIN E2, 26PIN +5V
IC173 12PIN E2, 24PIN +5V
71051
IC172
μPD71054
IC173
+5V
A0110
A0210
1-9E DATA-BUS
3-9A ADDRESS_IO_BUS
6-1B IS1TXRDY
6-1B IS1RXRDY
2-10E X10WR
2-10E X10RD
4-9F RESET
2-9B CLK0MC
3-10E X1S1SL
3-10D X1S49L
16-8C 54CLK1
2-10C CLK500K
6-1C 1540UT2
1991年 7月新コード化切替
旧図番 107101 A
0203-027079
UP-0668
CPU
90-4-27
12/16
日本光電

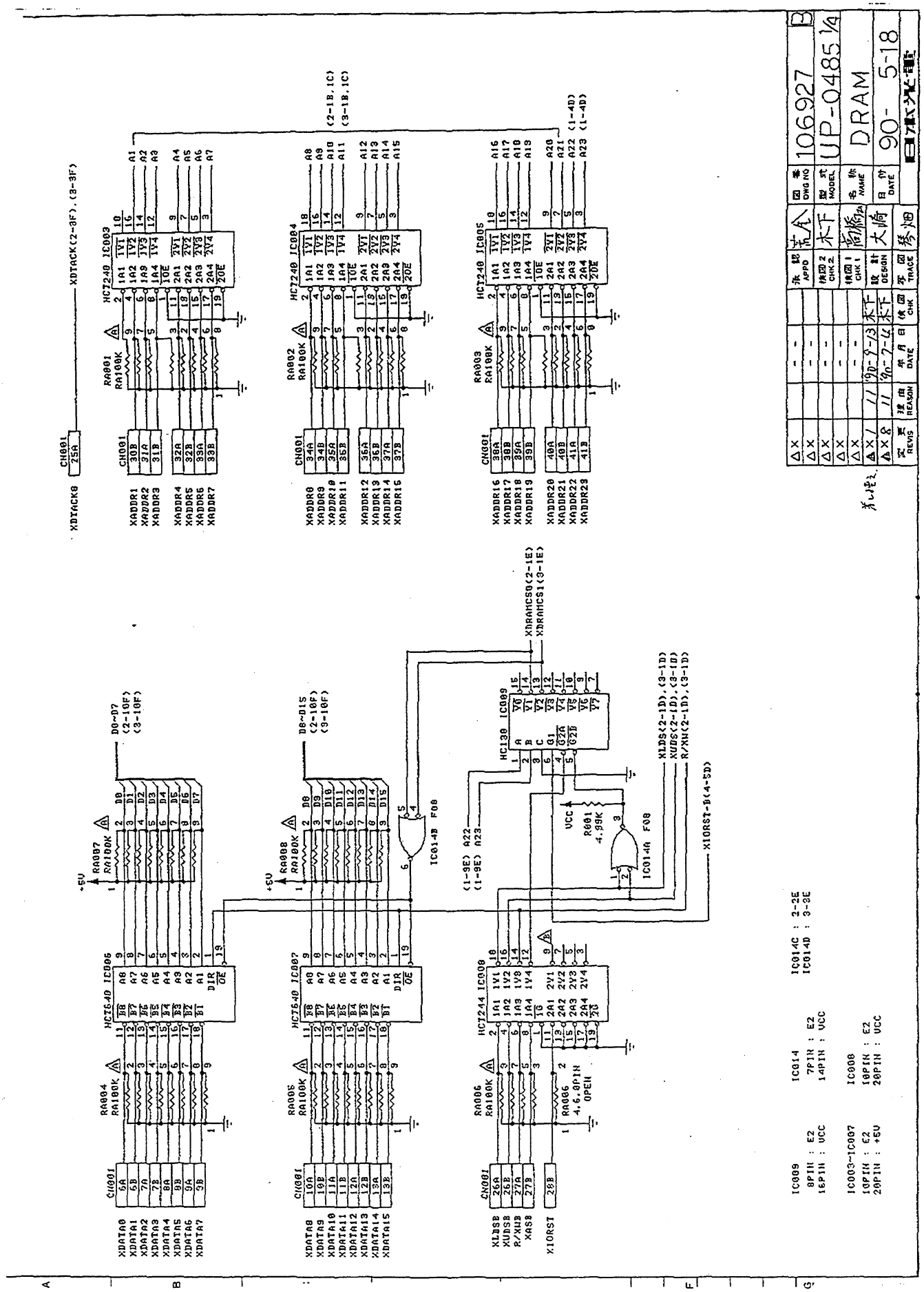

CN102
PCN10EA-32P-2.54DS
RA110
4.7KΩ
+5V
8279
IC176
DATA-BUS
CLK2M
A0110
RESET
XIORD
XIOWR
XERESET
XHITDLAMP
SHIFT
CNTL/STB
E2
E2
I791IRQ
X1795L
NOTE:IC176 20PIN E2, 40PIN +5V
107102
0203-027088
UP-0668
CPU
90 - 4 - 27
日本光電

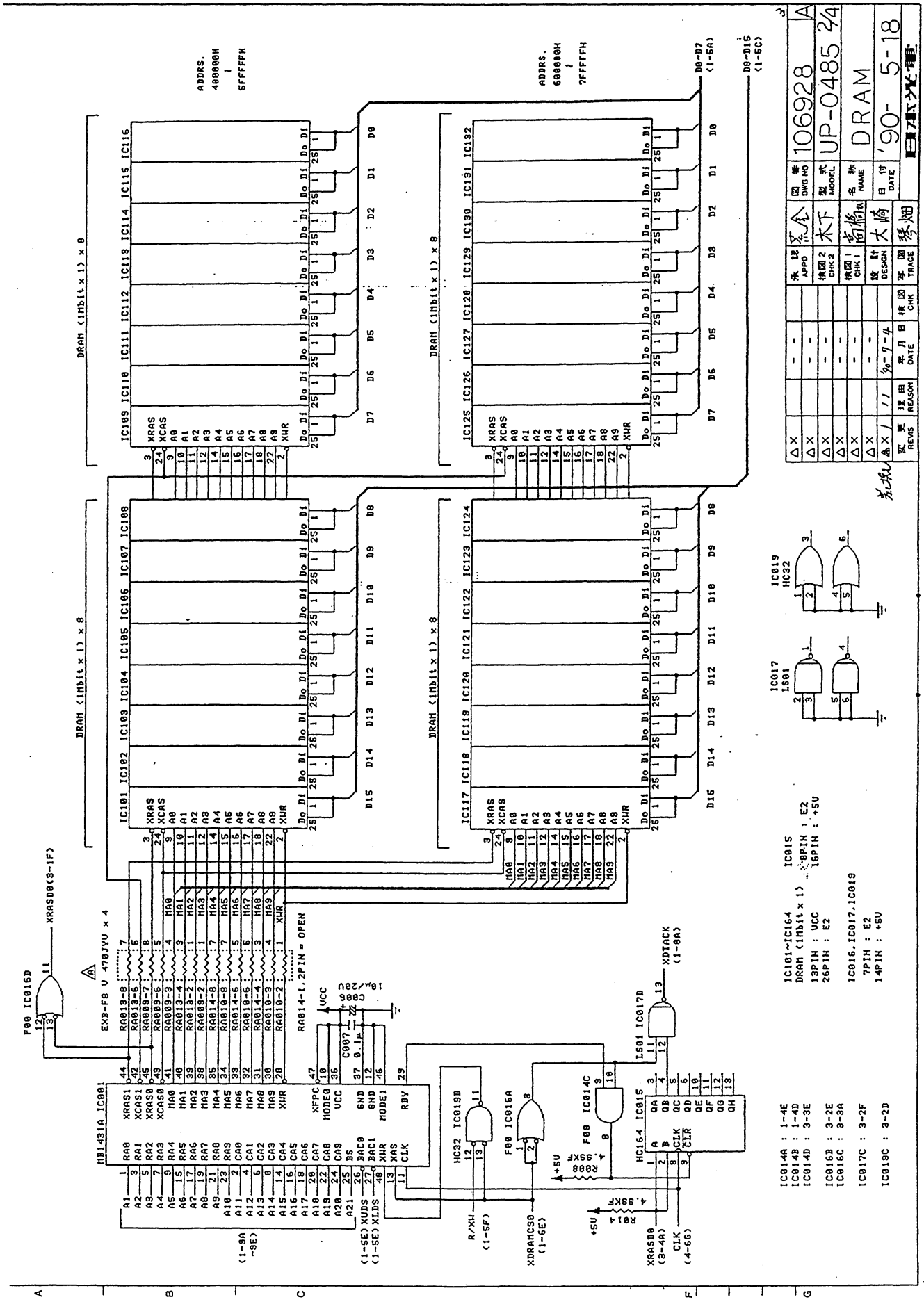

STATUS
DATA-BUS
ERESET
WTDERR
HTDSTOP
XHTDSTB
XST/HTDS
XIORD
XDS/LEDS
XIOWR
CEXT
VB
IC179,180,181
10 PIN GND(E2)
20 PIN +5V
IC177
7 PIN GND(E2)
14 PIN +5V
1991年 7月新コードに切替
旧図番 107103 A
0203-027097
UP-0668
CPU
90-6-10
14/16

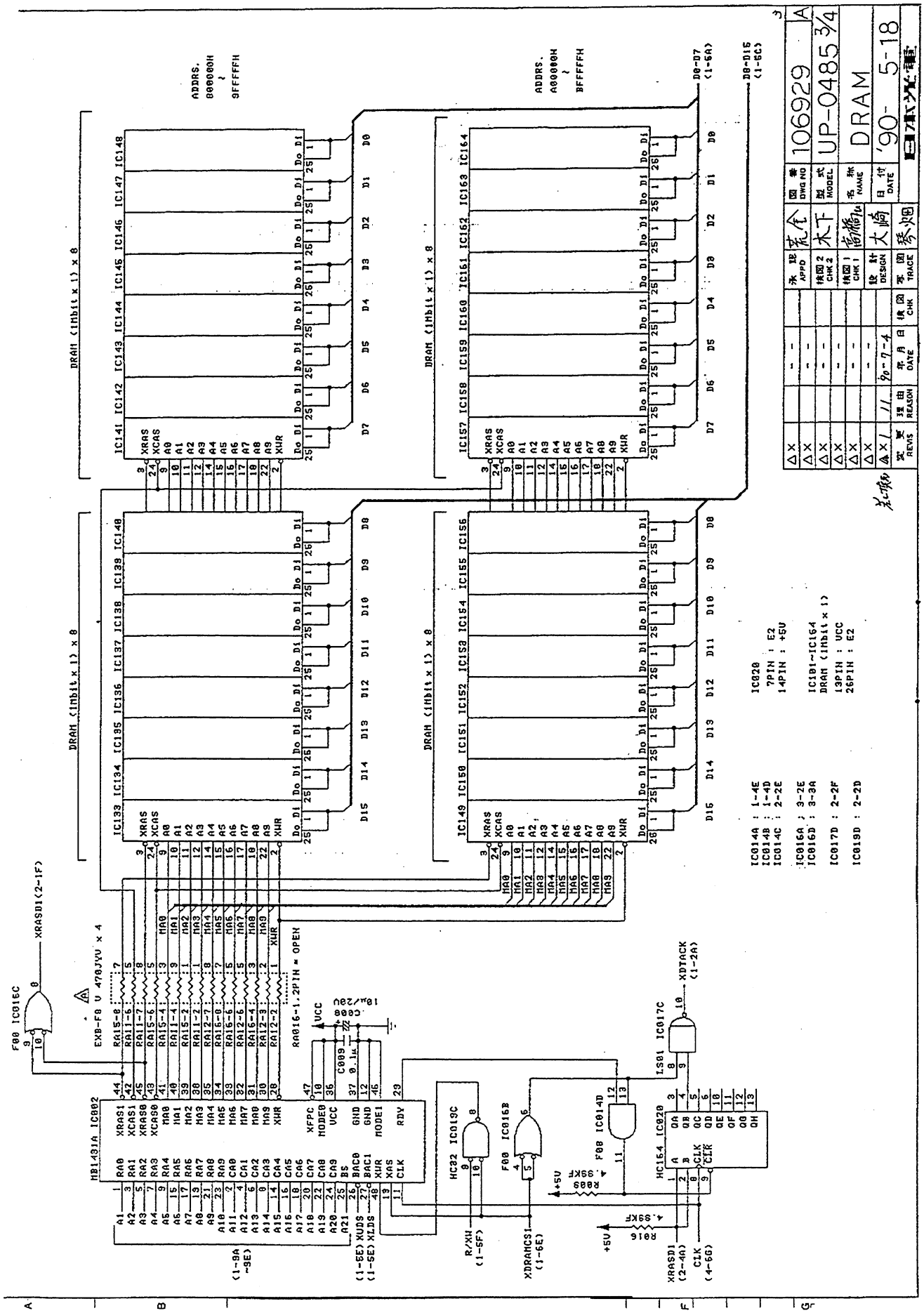

CN101
PCN10EA-90P-2.54DS
LS640
IC185
IC186
IC182
IC183
IC184
IC120
IC203
IC182,183,184,185,186
10 PIN GND(E2)
20 PIN +5V
IC203
7 PIN GND(E2)
14 PIN +5V
NOTE:C122-C124 6.8uF/35V
NOTE:C126-C140
TO BE INSTALLED.
1-9E DATA-BUS
1-9B ADDRESS-BUS
3-10F XEBUS
1-1C R/XW
16-6G DAG
14-1C CEXT
4-1E XPDOWN
2-9A CLK16MC
4-9F RESET
CLK16M
RESET
CENT
XPDOWN
+5V
E2

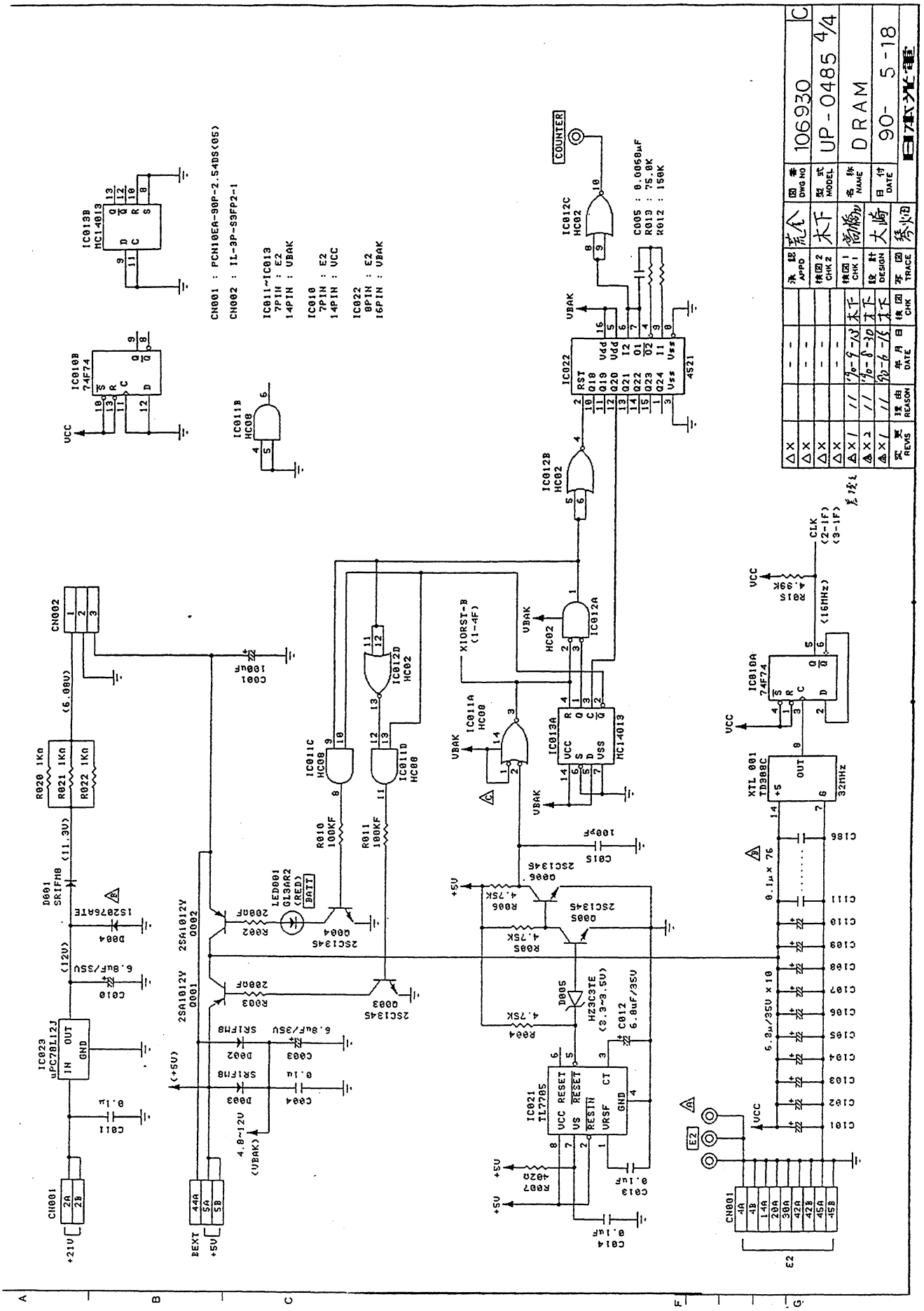



2/4
DRAM 4M BYTE
DRAM CONTROLLER
3/4
DRAM 4M BYTE
DRAM CONTROLLER
BATTERY
1/4
BUFFER
1/4
CN002
VBAK
VCC
+5V
SWITCHER
DETECTOR STOPPAGE POWER
REGULATOR
6.0V
CN001
+5V
+21V
SYSTEM BUS
3
107358
UP-0485
DRAM
'90- 9-28


XDTACK
XDTACK(2-3F),(3-3F)
CN001
25A
HCT240 IC003
HCT240 IC004
HCT240 IC005
RA001
RA002
RA003
RA100K
CN001
XADDR1
XADDR2
XADDR3
XADDR4
XADDR5
XADDR6
XADDR7
XADDR8
XADDR9
XADDR10
XADDR11
XADDR12
XADDR13
XADDR14
XADDR15
XADDR16
XADDR17
XADDR18
XADDR19
XADDR20
XADDR21
XADDR22
XADDR23
(2-1B,1C)
(3-1B,1C)
(1-4D)
(1-4D)
+5V
RA007
RA008
HCT640 IC006
HCT640 IC007
HCT244 IC008
HC139 IC009
D0~D7
(2-10F)
(3-10F)
D8~D15
(2-10F)
(3-10F)
XDRAMCS0(2-1E)
XDRAMCS1(3-1E)
(1-9E) A22
(1-9E) A23
IC014B F08
IC014A F08
VCC
R001
4.99K
XLDS(2-1D),(3-1D)
XUDS(2-1D),(3-1D)
R/XW(2-1D),(3-1D)
X10RST-B(4-5D)
RA004
RA005
RA006
RA100K
4.6.8PIN
OPEN
XDATA0
XDATA1
XDATA2
XDATA3
XDATA4
XDATA5
XDATA6
XDATA7
XDATA8
XDATA9
XDATA10
XDATA11
XDATA12
XDATA13
XDATA14
XDATA15
XLDSB
XUDSB
R/XWB
XASB
X10RST
IC009 8PIN : E2 16PIN : VCC
IC014 7PIN : E2 14PIN : VCC
IC003~IC007 10PIN : E2 20PIN : +5V
IC008 10PIN : E2 20PIN : VCC
IC014C : 2-2E
IC014D : 3-3E
106927
UP-0485 1/4
DRAM
90- 5-18
DWG NO
MODEL
NAME
DATE
APPD
CHK 2
CHK 1
DESIGN
CHK
TRACE
REVIS
REASON
DATE


DRAM (1Mbit x 1) x 8
ADDRS. 400000H / 5FFFFFH
ADDRS. 600000H / 7FFFFFH
D0~D7 (1-5A)
D8~D15 (1-6C)
XRASD0(3-1F)
F00 IC016D
EXB-F8 V 470JVU x 4
R0013-0
R0014-1.2PIN = OPEN
MB1431A IC00
HC32 IC019D
F00 IC016A
HC164 IC015
LS01 IC017D
IC019 HC32
IC017 LS01
IC015 8PIN : E2 16PIN : +5V
IC101~IC164 DRAM (1Mbit x 1) 13PIN : VCC 26PIN : E2
IC016. IC017. IC019 7PIN : E2 14PIN : +5V
IC014A : 1-4E
IC014B : 1-4D
IC014D : 3-3E
IC016B : 3-2E
IC016C : 3-3A
IC017C : 3-2F
IC019C : 3-2D
XDTACK (1-8A)
XDRAMCS0 (1-6E)
XRASD0 (3-4A)
CLK (4-6G)
R/XW (1-5F)
(1-9A ~9E)
(1-5E) XUDS
(1-5E) XLDS
DWG NO 106928
MODEL UP-0485 2/4
NAME DRAM
DATE '90- 5-18


DRAM (1Mbit x 1) x 8
ADDRS. 000000H ~ 3FFFFFH
ADDRS. 400000H ~ 7FFFFFH
ADDRS. 800000H ~ BFFFFFH
ADDRS. C00000H ~ FFFFFFH
DQ0-D7 (1-6A)
DQ8-D15 (1-6C)
IC141 IC142 IC143 IC144 IC145 IC146 IC147 IC148
IC133 IC134 IC135 IC136 IC137 IC138 IC139 IC140
IC157 IC158 IC159 IC160 IC161 IC162 IC163 IC164
IC149 IC150 IC151 IC152 IC153 IC154 IC155 IC156
XRAS
XCAS
XWR
MB1431A IC002
HC154 IC020
HC32 IC019C
F08 IC016B
F08 IC014D
LS01 IC017C
XDTACK (1-2A)
XRASDI (2-4A)
CLK (4-6G)
XDRAMCS1 (1-6E)
R/XW (1-5F)
+5V
R089 4.99KF
R016 4.99KF
C009 0.1μF
C008 10μF/25V
VCC
F00 IC016C
XRASDI(2-1F)
EXB-F8 U 470JVU x 4
RA016-1.2PIN = OPEN
IC020 7PIN : E2 14PIN : +5V
IC014A : 1-4E
IC014B : 1-4D
IC014C : 2-2E
IC016A : 3-2E
IC016D : 3-3A
IC017D : 2-2F
IC019D : 2-2D
IC101~IC164 DRAM (1Mbit x 1) 13PIN : VCC 26PIN : E2
106929
UP-0485 3/4
DRAM
'90- 5-18


CN001 : PCN10EA-90P-2.54DS(05)
CN002 : IL-3P-S3FP2-1
IC011~IC013 7PIN : E2 14PIN : VBAK
IC010 7PIN : E2 14PIN : VCC
IC022 8PIN : E2 16PIN : VBAK
C005 : 0.0058μF
R013 : 75.0K
R012 : 150K
106930
UP-0485 4/4
DRAM
90- 5-18

MANUAL CHANGE INFORMATION

UNIT	MODEL	SERIAL NO.	REVISION
Transformer unit SC-001RA/RJ/RK Regulator UP-0315	MU-820RA		
	MU-820RJ		
	MU-820RK	from 00111	D0

Section 1 Introduction (Page 1-11, 1-12, 1-19, 1-20)
Section 3 Circuit Description (page 3-79)

FROM	TO
SC-001RA/RJ/RK	SC-013RA/RJ/RK
UP-0315	UP-0654

Section 11 Electrical parts list

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Section 12 Part location guide

FROM	TO
Page 12-12	6/12

Section 13 Circuit Diagrams

FROM	TO
Page 13-3, 13-4, 13-84 to 13-87	7/12 to 12/12

COMPATIBILITY

The same unit is also used in the other instruments. Compatibility between the power supply blocks and main instruments is shown below.

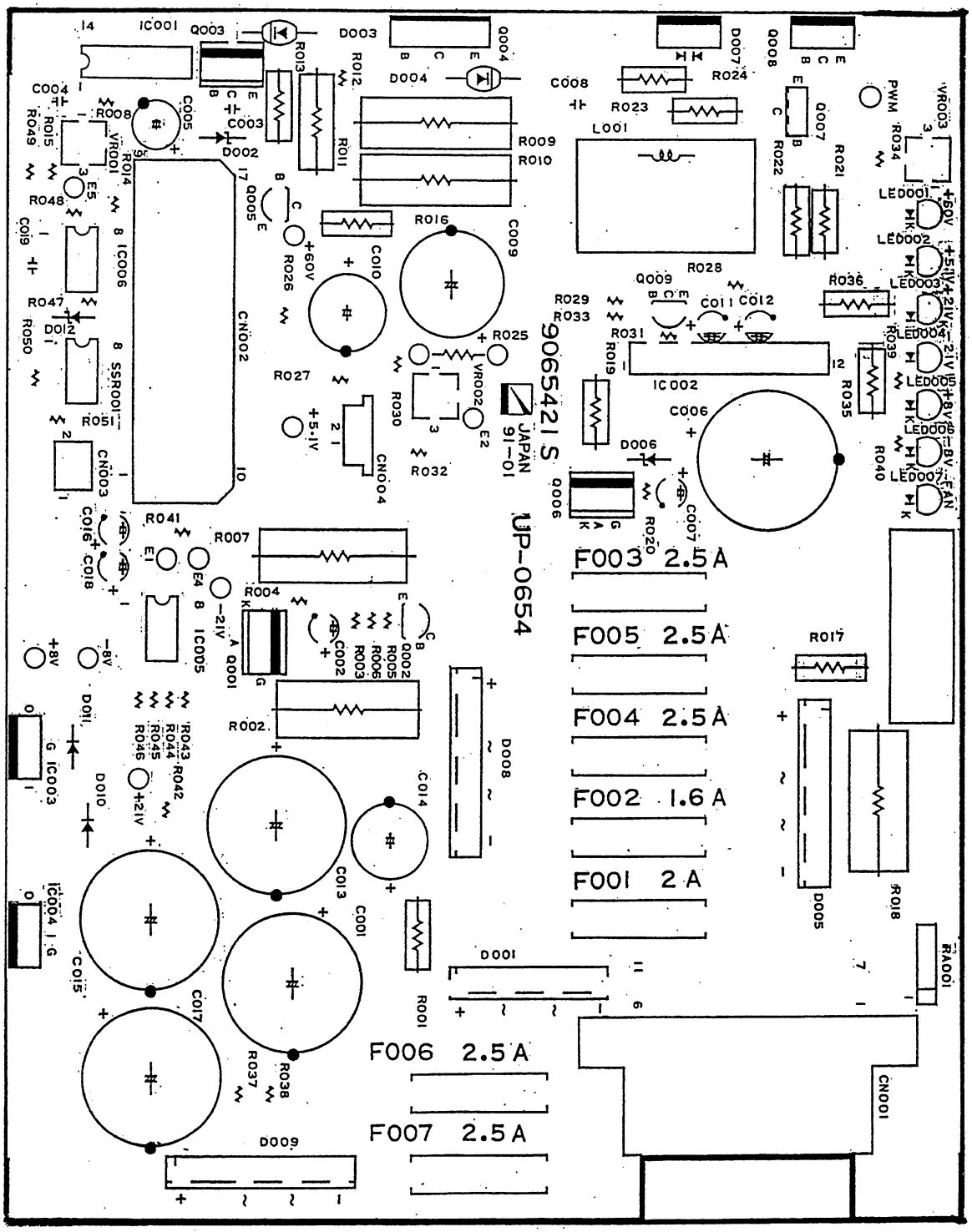
	UP-0315 (C117: 2200μF) SC-001RA/RJ/RK	UP-0315 (C117: 4700μF) SC-001RA/RJ/RK	UP-0654 SC-013RA/RJ/RK
MU-820RA/RJ/RK	NO	YES	YES
JJ-810/820RA/RJ/RK	NO	YES	YES
MU-800RA/RJ/RK	YES	YES	YES
MU-802RA/RJ/RK	NO	NO	YES
MU-841RA MU-843RA/RJ/RK	NO	NO	YES

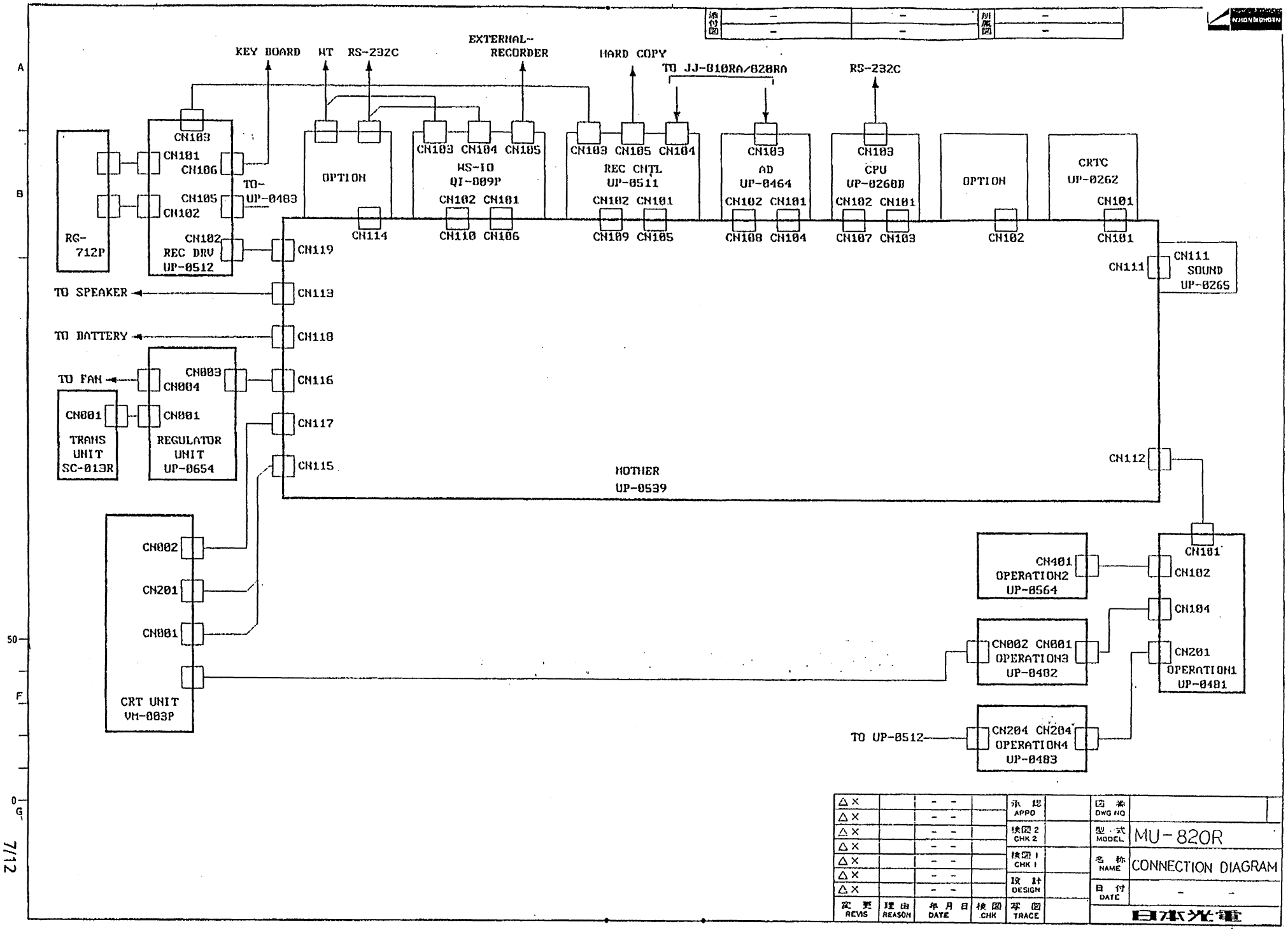
ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
SC-013RA TRANSFORMER UNIT (MU-820RA)					
SC-013RA	CN001	5415337	8	NCN	Receptacle 170458-1
SC-013RA	CN001	5415373	1	NCN	Housing 172024-1
SC-013RA	F001	5620062	1	FUSE	SAU-4A
SC-013RA	F001	5625396	1	FH	FEU 031.1681 Body
SC-013RA	F001	5625404	1	FH	FEK 031.1661 Cap
SC-013RA	F002	5620062	1	FUSE	SAU-4A
SC-013RA	F002	5625396	1	FH	FEU 031.1681 Body
SC-013RA	F002	5625404	1	FH	FEK 031.1661 Cap
SC-013RA	LF001	1706022	1	TH	SUP-E3G-E-2 Line filter
SC-013RA	SW001	3250367	1	SW	JPZ2120-0101
SC-013RA	T001	3715294	1	PT	T-3715294 117V MU-841RA
SC-013RJ TRANSFORMER UNIT (MU-820RJ)					
SC-013RJ	CN001	5415337	8	NCN	Receptacle 170458-1
SC-013RJ	CN001	5415373	1	NCN	Housing 172024-1
SC-013RJ	F001	5620062	1	FUSE	SAU-4A
SC-013RJ	F001	5625396	1	FH	FEU 031.1681 Body
SC-013RJ	F001	5625404	1	FH	FEK 031.1661 Cap
SC-013RJ	F002	5620062	1	FUSE	SAU-4A
SC-013RJ	F002	5625396	1	FH	FEU 031.1681 Body
SC-013RJ	F002	5625404	1	FH	FEK 031.1661 Cap
SC-013RJ	LF001	1706022	1	TH	SUP-E3G-E-2 Line filter
SC-013RJ	SW001	3250367	1	SW	JPZ2120-0101
SC-013RJ	TB001	5611972	1	TERM	ULC-505-3P-C
SC-013RJ	T001	3715329	1	PT	T-3715329 100V MU-841RJ
SC-013RK TRANSFORMER UNIT (MU-820RK)					
SC-013RK	CN001	5415337	8	NCN	Receptacle 170458-1
SC-013RK	CN001	5415373	1	NCN	Housing 172024-1
SC-013RK	F001	5621079	1	FUSE	179 120-2A
SC-013RK	F001	5625396	1	FH	FEU 031.1681 Body
SC-013RK	F001	5625413	1	FH	FEK 031.1663 Cap
SC-013RK	F002	5621079	1	FUSE	179 120-2A
SC-013RK	F002	5625396	1	FH	FEU 031.1681 Body
SC-013RK	F002	5625413	1	FH	FEK 031.1663 Cap
SC-013RK	LF001	1706022	1	TH	SUP-E3G-E-2 Line filter
SC-013RK	SW001	3250367	1	SW	JPZ2120-0101
SC-013RK	TB001	5611972	1	TERM	ULC-505-3P-C
SC-013RK	T001	3715338	1	PT	T-3715338 200V MU-841RK

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-0654 REGULATOR UNIT					
UP-0654	CNJ001	5413981	1	NCN	172038-1 11P
UP-0654	CNJ002	5415239	1	NCN	171363-1 17pin MALE
UP-0654	CNJ003	5428225	1	PCN	M60-02-30-114P
UP-0654	CNJ004	5424755	1	PCN	HNC2-2.5P-2DS 2P
UP-0654	CNP004	5424621	1	NCN	Contact HNC-2.5S-D-A
UP-0654	CNP004	5424657	1	PCN	Housing HNC2-2.5S-2 2P
UP-0654	C001	7415244	1		ECOS2CA821BA
UP-0654	C002	7415271	1		ECEA1HGE010
UP-0654	C003	3839757	1	FLC1	ECQ-V1H104JZ 0.1uF
UP-0654	C004	3839525	1	FLC1	ECQ-B1H102JZ 0.001uF
UP-0654	C005	7415262	1		ECEA2AGE220
UP-0654	C006	7415378	1		ECOS1VA822BA
UP-0654	C007	7415271	1		ECEA1HGE010
UP-0654	C008	3839525	1	FLC1	ECQ-B1H102JZ 0.001uF
UP-0654	C009	7415298	1		ECEA1EGE332
UP-0654	C010	7415315	1		ECEA1EGE102
UP-0654	C011-C012	7415289	2		ECEA1VGE330
UP-0654	C013	7415378	1		ECOS1VA822BA
UP-0654	C014	7415306	1		ECEA1VGE102
UP-0654	C015	7415369	1		ECOS1EA822BA
UP-0654	C016	7415289	1		ECEA1VGE330
UP-0654	C017	7415369	1		ECOS1EA822BA
UP-0654	C018	7415289	1		ECEA1VGE330
UP-0654	C019	3820795	1	FLC1	ECQ-B1H 103JZ 0.01uF
UP-0654	D001	7415476	1		D3SB40
UP-0654	D002	1090089	1	ZD3	HZ12LA2 Orange
UP-0654	D003-D004	7400198	2		V06E
UP-0654	D005	7415467	1		D5SB20
UP-0654	D006	7400126	1		HZ6LB2
UP-0654	D007	0910561	1	DP	S10SC4M 10A40V
UP-0654	D008-D009	7415467	2		D5SB20
UP-0654	D012	7400135	1		HZ6LA2
UP-0654	F001	5620044	1	FUSE	GDL-2
UP-0654	F001	7415413	1		F4034P
UP-0654	F002	5620472	1	FUSE	GDL-2 1/2
UP-0654	F002	7415413	1		F4034P
UP-0654	F003	5620062	1	FUSE	SAU-4A
UP-0654	F003	7415413	1		F4034P
UP-0654	F004	5620062	1	FUSE	SAU-4A
UP-0654	F004	7415413	1		F4034P

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-0654	F005	5620053	1	FUSE SAU-3A (GDL-3)
UP-0654	F005	7415413	1	F4034P
UP-0654	F006	5620053	1	FUSE SAU-3A (GDL-3)
UP-0654	F006	7415413	1	F4034P
UP-0654	IC001	1250219	1	REG HA17723 (723CJ.G)
UP-0654	IC002	1601893	1	MD SWC-01
UP-0654	IC003	1253305	1	REG uPC7808H Regulator
UP-0654	IC004	1253288	1	REG uPC7908H Regulator
UP-0654	IC005-IC006	1204867	2	AIC HA17903PS Comparator
UP-0654	LED001-LED007	1102246	7	LED GL-3AR2 Red
UP-0654	L001	7415431	1	EN4-120-0090
UP-0654	Q001	5601323	1	SOCKET RT807
UP-0654	Q001	7415387	1	3P4uH
UP-0654	Q003	5601323	1	SOCKET RT807
UP-0654	Q003	7400162	1	2SD1135(C)
UP-0654	Q004	7400153	1	2SD1090
UP-0654	Q006	0950615	1	SCR 5P4M (5A400V)
UP-0654	Q006	5601323	1	SOCKET RT807
UP-0654	Q007	7415449	1	2SA1244
UP-0654	Q008	7415396	1	2SC3693
UP-0654	RA001	4090582	1	RM EXB-P84-103J
UP-0654	SSR001	7415458	1	S12MD22
UP-0654	TSW001	7415422	1	OHD3-90MU
UP-0654	VR001	4160809	1	TPOT GF06P 2KOHM
UP-0654	VR002	4160613	1	TPOT GF06P 10KOHM
UP-0654	VR003	4160907	1	TPOT GF-06S(ET-6S) 1KOHM

UP-0654 Regulator board





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△X		- -		検図2 CHK 2		型 式 MODEL	MU-820R
△X		- -		検図1 CHK 1		名 称 NAME	CONNECTION DIAGRAM
△X		- -		設 計 DESIGN		日 付 DATE	- -
△X		- -					
変 更 REVIS	理 由 REASON	年 月 日 DATE	検 図 CHK	写 図 TRACE			

日本光電

7/12

添付図	-	-	所属図	-
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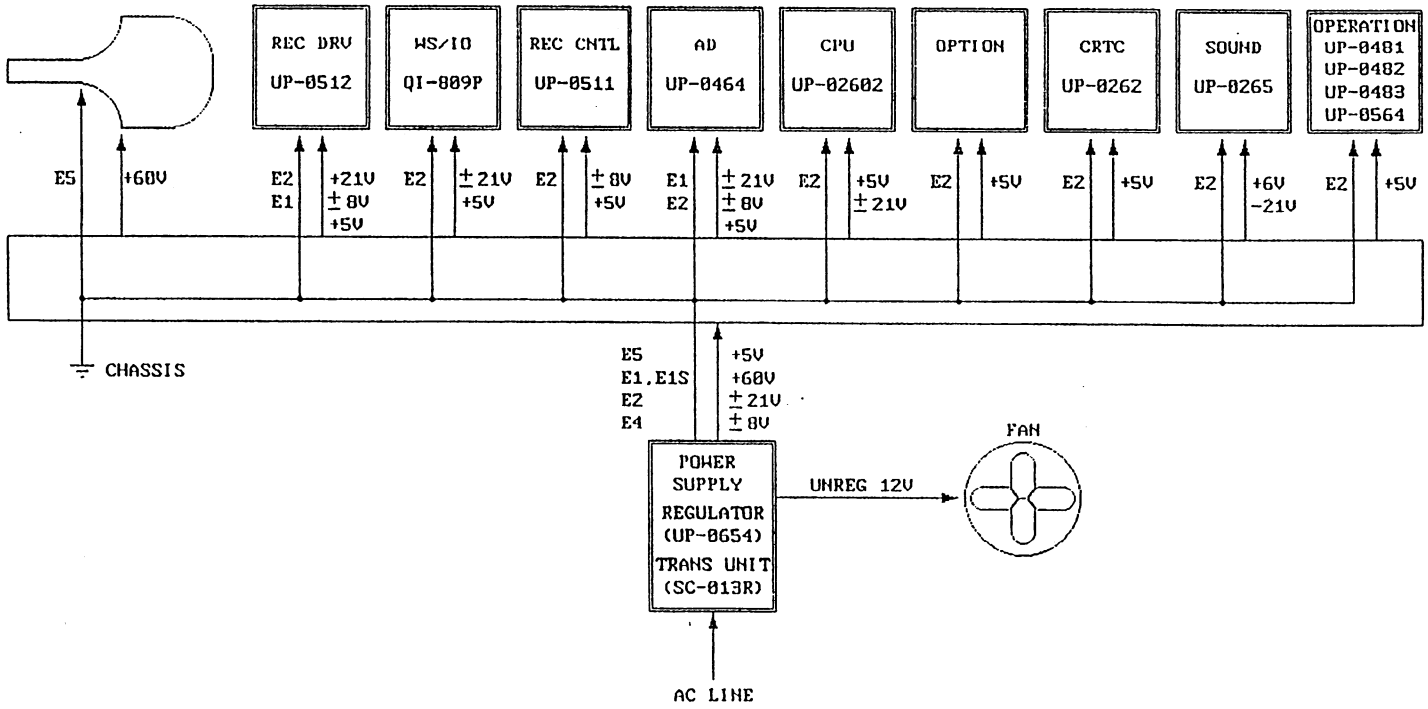

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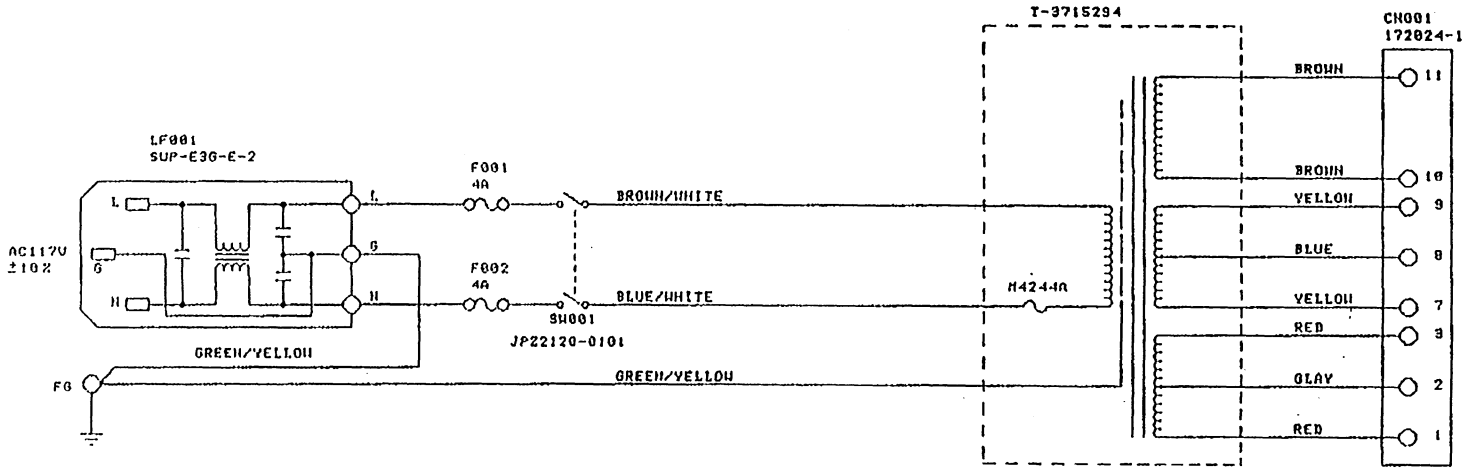

1991年 7月版コードに切替

旧図番 107144 3

変更 REVIS	理由 REASON	年月日 DATE	検図 CHK
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承認 APPD	荒金
検図2 CHK 2	木下
検図1 CHK 1	六井
設計 DESIGN	坂野
製図 TRACE	秀樹

図番 DWG NO	0203-027257
型式 MODEL	SC-013RA
名称 NAME	TRANS UNIT
日付 DATE	90-6-20

三洋次電機

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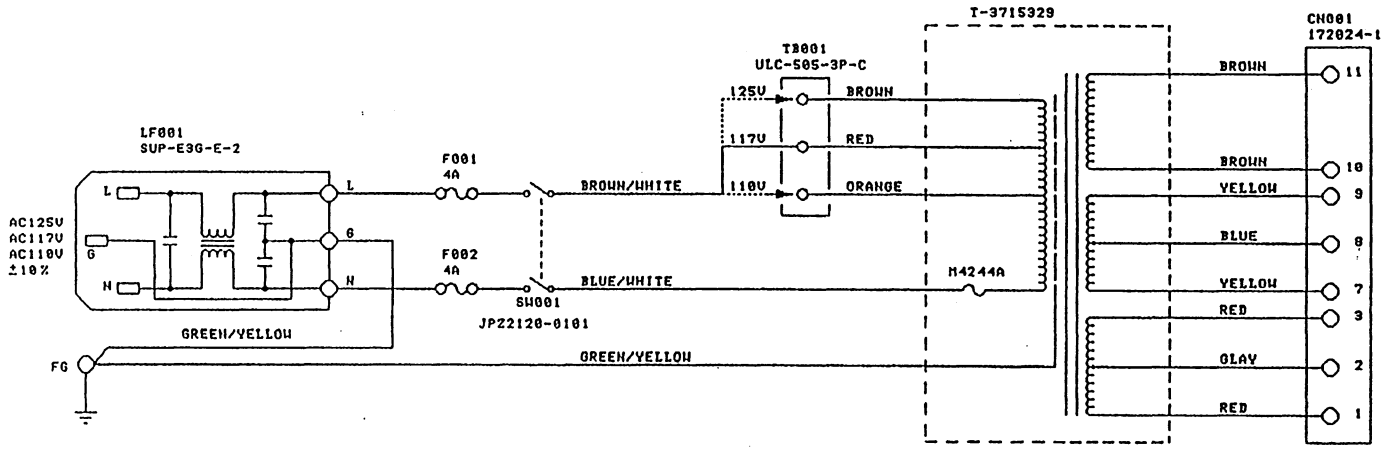

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旧図番 107145

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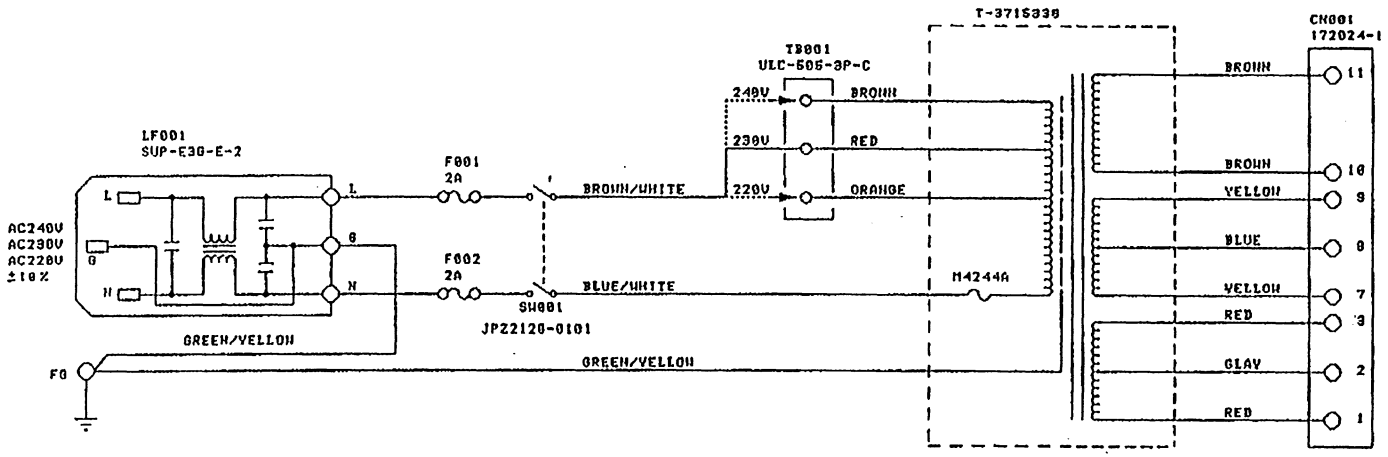
承認 APPD	谷与	図番 DWG NO	0203-027266
検図2 CHK 2	木下	型式 MODEL	SC-013RJ
検図1 CHK 1	市井	名称 NAME	TRANS UNIT
設計 DESIGN	牧野	日付 DATE	90-6-20
写図 TRACE	秀畑	日本光電	



1991年 7月新コードに切替
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△X		- -		検図1 CHK 1	高井	名称 NAME	TRANS UNIT
△X		- -		設計 DESIGN	牧野	日付 DATE	90-6-2(
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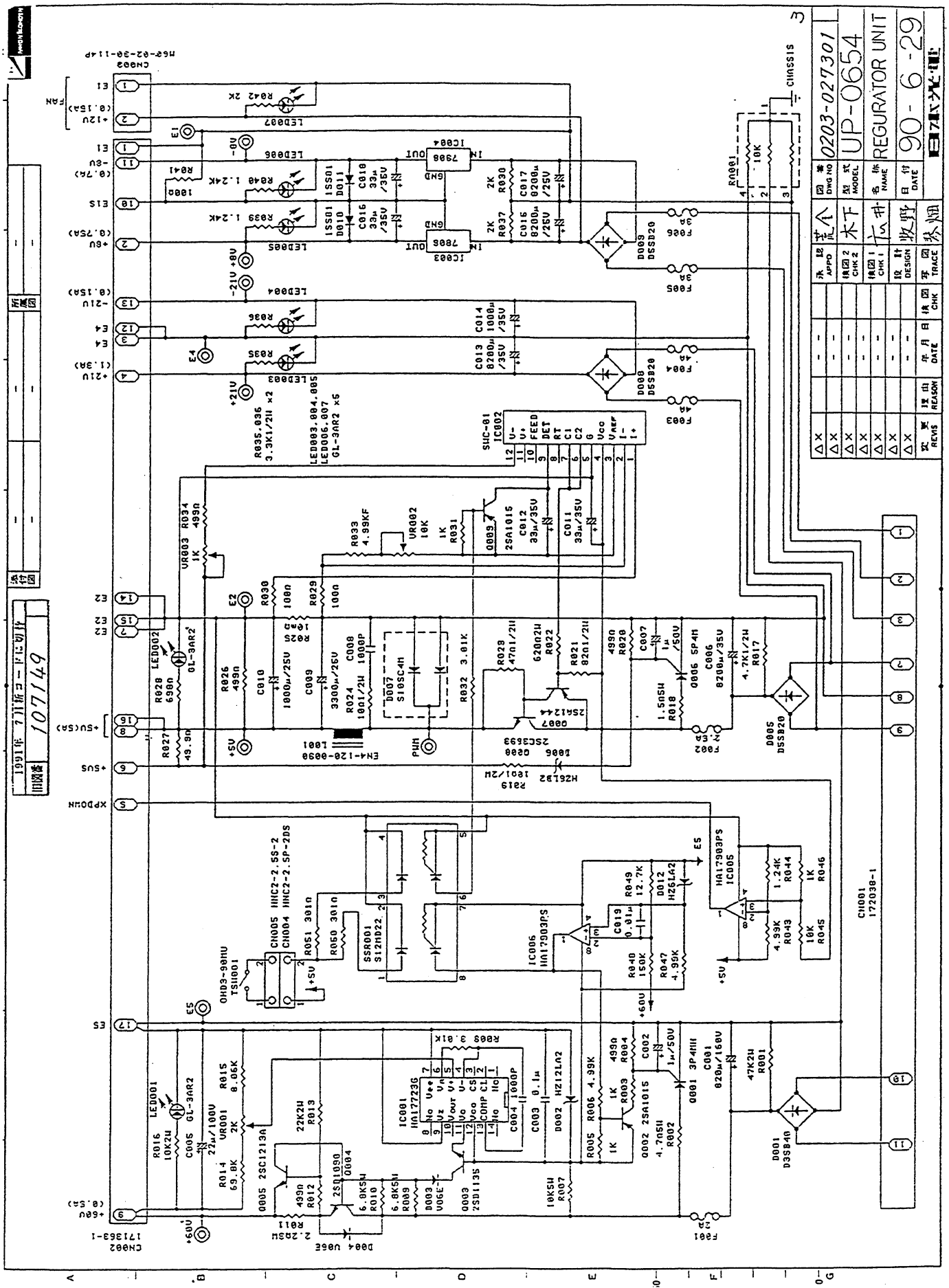
0203-027301
UP-0654
REGURATOR UNIT
90-6-29
107149

MU-820RA
MU-820RJ
MU-820RK

QM-800P

CENTRAL MONITOR MAIN UNIT

MU-820R

CNS-8200 SYSTEM

0634-000103

CAUTION

Risk of Fire, Replace Battery as Marked.

Refer to page 11-17 for marked battery.

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Section 1

1. Introduction

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1.1 General

CNS-8200A/J/K series central monitoring system is designed to be used widely in ICU, CCU, recovery room, etc.

The CNS-8200A/J/K system consists of MU-820RA/J/K central monitor main unit and JJ-810R/820RA/J/K signal exchanger.

Refer to the sepaately provided Service Manual for the JJ-810R/820RA/J/K.

In the MU-820RA/J/K central monito main unit, a number of LSC chips such as CPU chip 68000 and muti-layer PC boards. Servicing of this unit is basically done by replaceing each PC board.

For easy servicing, self check program is provided with this unit and when a trouble is found, error code is stored in the error code history which focuses the board with trouble.

Please read this manual careful before attempting to service the instrument.

1.2 SPECIFICATIONS (total specifications of the MU-820RA connected with BSM-8500A)

1.2.1 CRT screen

1)	CRT used	12 inch, electromagnetic deflection type
2)	Waveform display	Non-fade, moving method or fix mode(all beds' screen mode)
3)	Number of waveform traces	maximum 8 (all beds' data display mode screen)
4)	Sweep speed	25mm/sec +10%
5)	Sweep time	3.92 sec.(8 beds' ECG screen) 8 sec.(4 beds' ECG screen) 6 sec. (individual bed's waveform screen)
6)	Trace brightness control	2 steps

1.2.2 Waveform display

- ECG1, 2
- BP1, 2, 3, 4
- Respiration
- CO2 curve
- Aux. input
- EEG

1.2.3 Numerical data display

- HR, VPC rate, respiration rate
- BP1 (SYS/MEAN/DIA)
- BP2 (SYS/MEAN/DIA)
- BP3 (SYS or MEAN or DIA)
- BP4 (SYS or MEAN or DIA)
- T1, T2, deltaT, Tb
- ETCO2, tcPO2, tcPCO2
- SaO2, ST level

1.2.4 Trendgraph

1)	Items	HR, VPC rate, resp. rate, apnea(T), apnea(F), BP1, 2, 3, 4(SYS/MEAN/DIA) T1, T2, Tb ETCO2, tcPO2, tcPCO2, SaO2, ST level
2)	Event marks	Asystole, V.Fib., V.Tachy, VPC run, Couplet, noise/off, mark from BSM, mark from CNS
3)	Trend time	8 + 1 hours, 24 + 1 hours

1.2.5 Alarm function

1) Alarm items	High/Low limits; Heart rate Respiration rate BP1/2/3/4 (SYS/MEAN/DIA) T1/T2/deltaT/Tb SaO2 Others Apnea time Arrhythmias
2) Alarm indication	Blinking of red alarm lamp Alarm tone generation
3) Alarm suspension	Suspension of alarm tone for a specified time of period
4) Alarm recording	Automatic (available on/off control)

1.2.6 ECG sensitivity control x1 (10mm/mV), X0.5, x0.75, x1.5, x2, x4

1.2.7 Respiration waveform sensitivity control x0.5, x1, x2, x4

1.2.8 BP waveform scale ..... Separated for P1 and P2/P3/P4 or common

1.2.9 Overview function ..... Waveform screen display of outside continuous monitoring beds

1.2.10 Remote funtion setting of the bedside monitor ..... Alarm limits
Personal setup items
VPC learn actrivation

1.2.11 Bedside monitor file transfer ..... Arrhythmia recall data
ST level data
Hemodynamics list

1.2.12 Built-in recorder

1) Recording method ..... Thermal array recording

2) Number of channel 1

3) Paper speed ..... 25mm/sec.

4) Annotation printing ..... Bed ID, patient's name, time and date, reason of recording activation, numerical value data, etc.

1.2.13 Others

Operating environmental conditions

1) Temperature ..... 10- 40°C

2) Humidity 30- 85%RH

3) Atmospheric pressure 70- 106kPa

Storage environmental conditionds

1) Temperature ..... -10- +60°C

2) Humidity 15- 95%RH

3) Atmospheric pressure 70- 106kPa

Power requirement

MU-820RA ..... AC 117V, 50/60Hz, 190VA
MU-820RJ ..... AC 110, 117, 125V, 50/60Hz, 190VA
MU-820RK ..... AC 220, 230, 240V, 50/60Hz, 190VA

Safety

1) Withstanding voltage ..... AC1.5kV for one minute

2) Ground leakage current .... Less than 100uA

3) Chassis leakage current ... Less than 100uA

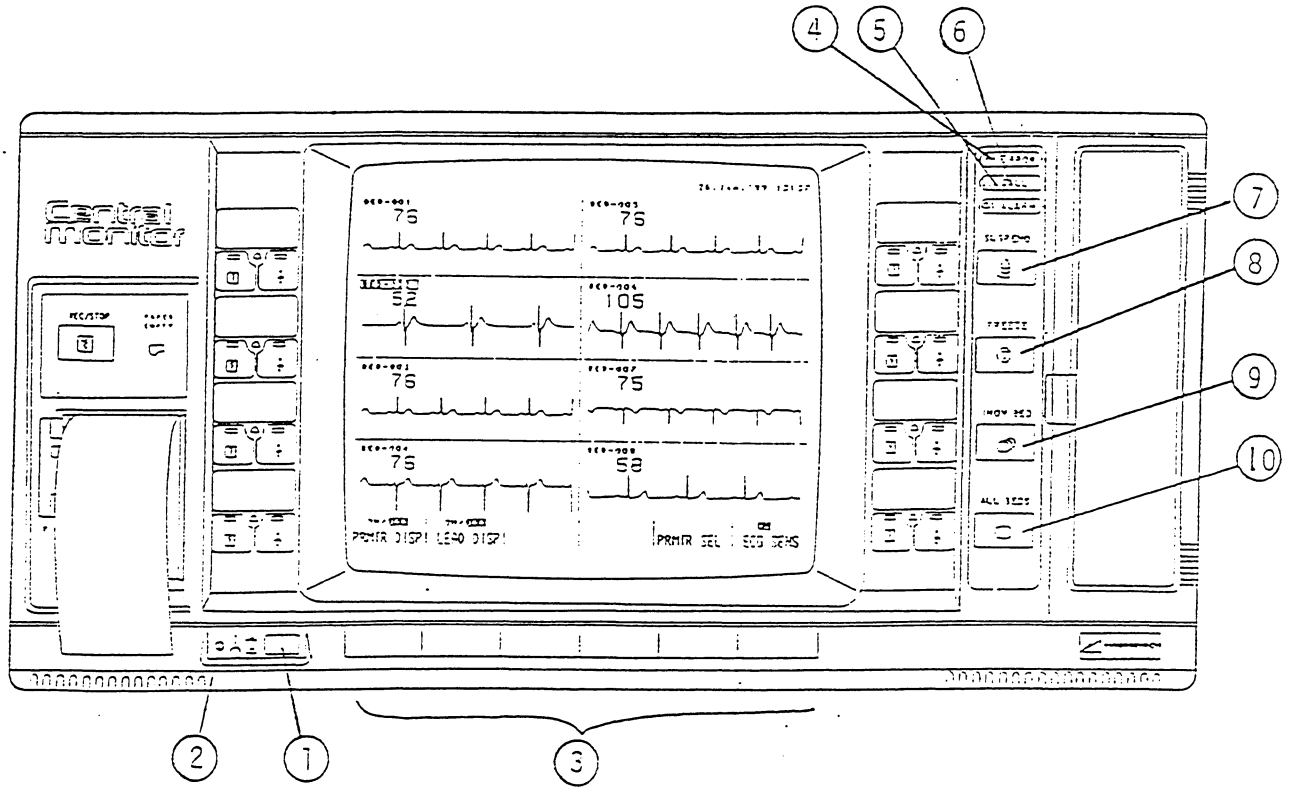
4) Safety standard ..... IEC601-1 Class I, type B
CSA (MU-820RA)

1.2.14 Dimensions and net weight

. MU-820RA/J/K .. 535W x 268H x 382D (mm), approx. 27kg

1.3 Explanation of panel and controls

1.3.1 Front



1 Power switch ..... Pressing the key once turns the power on, pressing again turns the power off.

2. Power indication lamp .... Lights up to indicate that power is on.

3. Multifunction keys ..... Change the functions according to the screen mode.

4. ERROR indication lamp .... Lights up to indicate an equipment error detected by the built-in self-check system.

5. CALL indication lamp ..... Lights up when the nurse call signal comes from a bedside monitor (telemetry monitor OEC-6201, OE-6301).

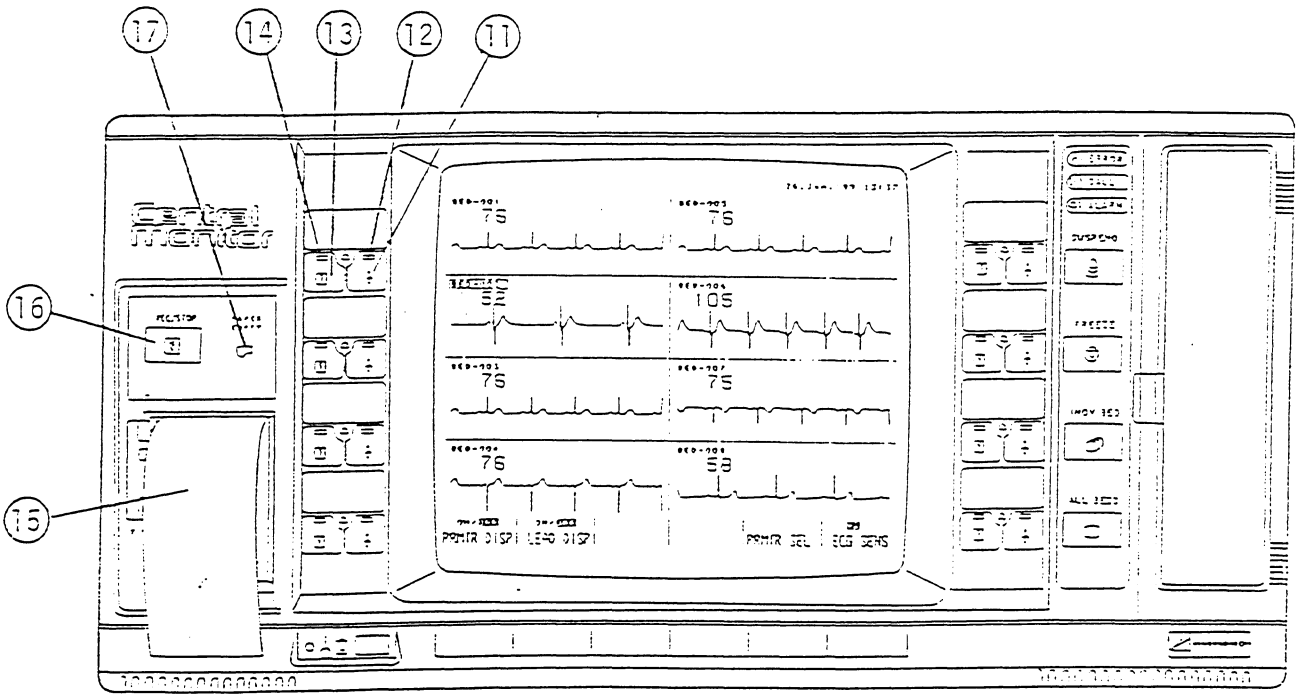
6. ALARM indication lamp .... Lights up when an alarm occurs.

7. SUSPEND key ..... Used to suspend the alarm tone.

8. FREEZE key ..... Used to freeze/release waveforms on the screen.

9. INDIV BED key ..... Calls up an individual bed's screen.

10. ALL BEDS key ..... Calls up the all beds screen.



11. Bed select key ..... Selects a bed.

12. Bed select indication lamp ..... Lights up when the corresponding bed is being selected.

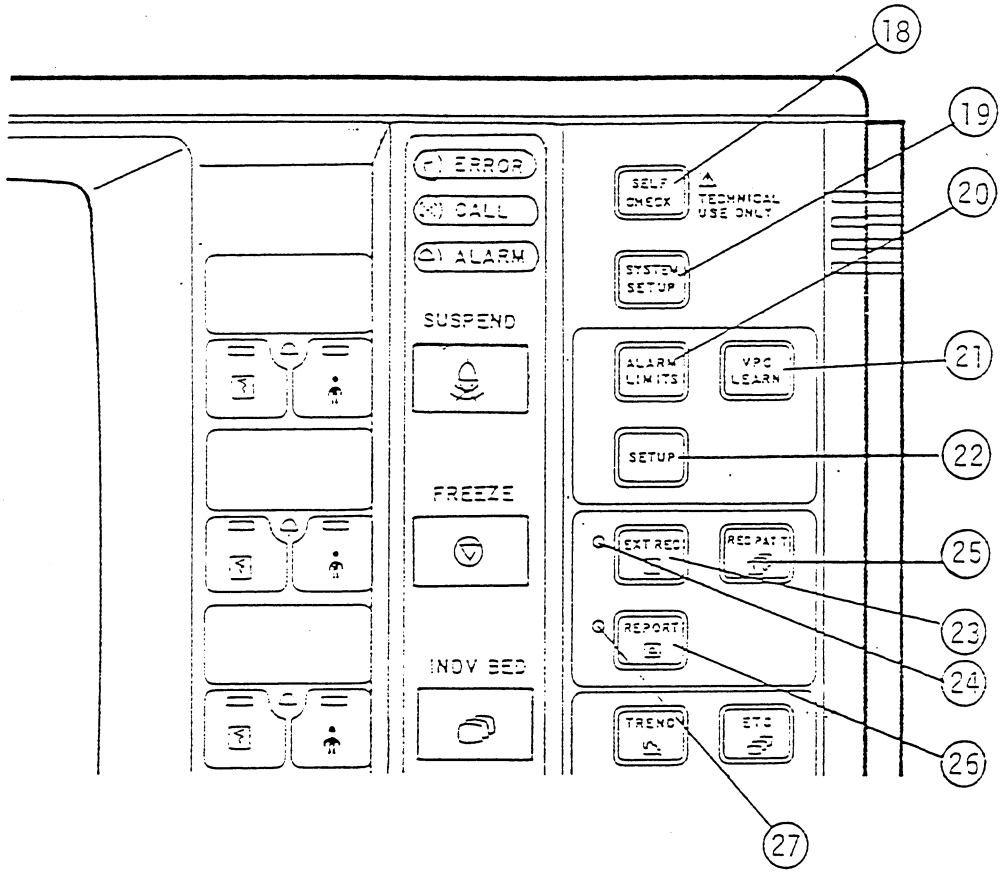
13. Record key ..... Starts recording of the corresponding bed data.

14. Recording indication lamp ..... Lights up when the recorder has been activated by the corresponding record key and is recording the corresponding bed's data.

15. Recorder ..... Built-in 1-channel thermal array recorder 50mm wide.

16. REC/STOP key ..... Starts and stops recording.

17. PAPER EMPTY indication lamp ..... Blinks when the paper is gone and lights up when the paper magazine is open.



18. SELF CHECK key ..... Calls up the self-check program.

19. SYSTEM SETUP key ..... Calls up the system setup screen.

20. ALARM LIMITS key ..... Calls up the alarm limits screen for setting high/low limits and arrhythmia related items.

21. VPC LEARN key ..... Used to relearn the dominant QRS complex of the selected bed.

22. SETUP key ..... Calls up an individual bed's setup mode screen.

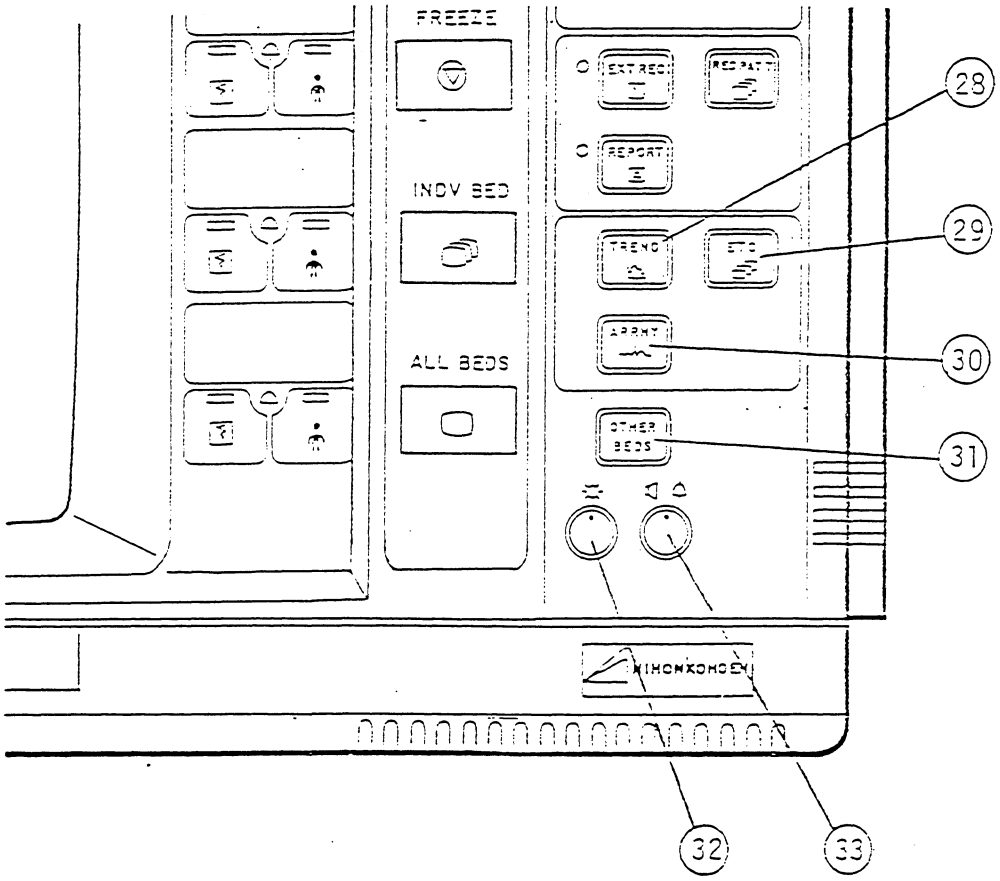
23. EXT REC key ..... Controls start/stop of the externally connected recorder.

24. EXT REC indication lamp ..... Lights up while the external recorder is running.

25. REC PATT key ..... Selects the waveform pattern for the external recorder.

26. REPORT key ..... Activates the external recorder to print the trend or list format data.

27. REPORT printing indication lamp ..... Lights up while the external recorder is printing the report.



28. TREND key ..... Calls up the trendgraph screen.

29. ETC key ..... Calls up the ST level and hemodynamics list screens.

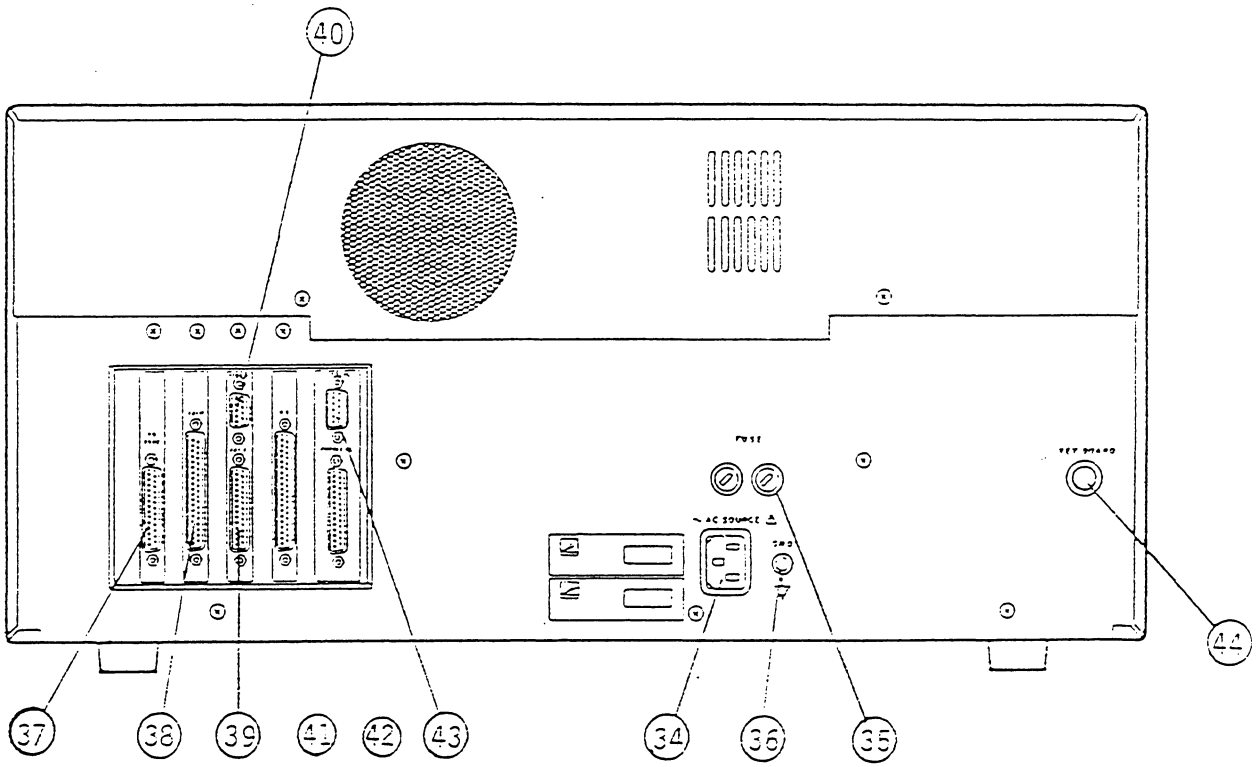
30. ARRHY key ..... Calls up the arrhythmia recall screen.

31. OTHER BED key ..... Calls up an unmanaged bed's waveform screen.

32. Brightness control switch ..... Controls screen brightness.

33. Alarm tone volume ..... Controls alarm tone volume.

1.3.2 Rear



34. AC connector ..... AC power source

35. Fuse holder ..... Fuse holder for a 2A or 4A time-lag fuse

36. Potential equalization terminal ..... A terminal to equalize the electrical potential when a number of units of medical equipment are used simultaneously

37. RS-232C connector..... Connector for RS-232C communication with other equipment

38. JJ-W connector ..... Connector for analog waveform input from the signal exchanger

39. JJ-S connector..... Connector for digital communication with the signal exchanger

40. VIDEO connector ..... Connector for output to the external recorder

41. WS connector ..... Connector for output to the external recorder

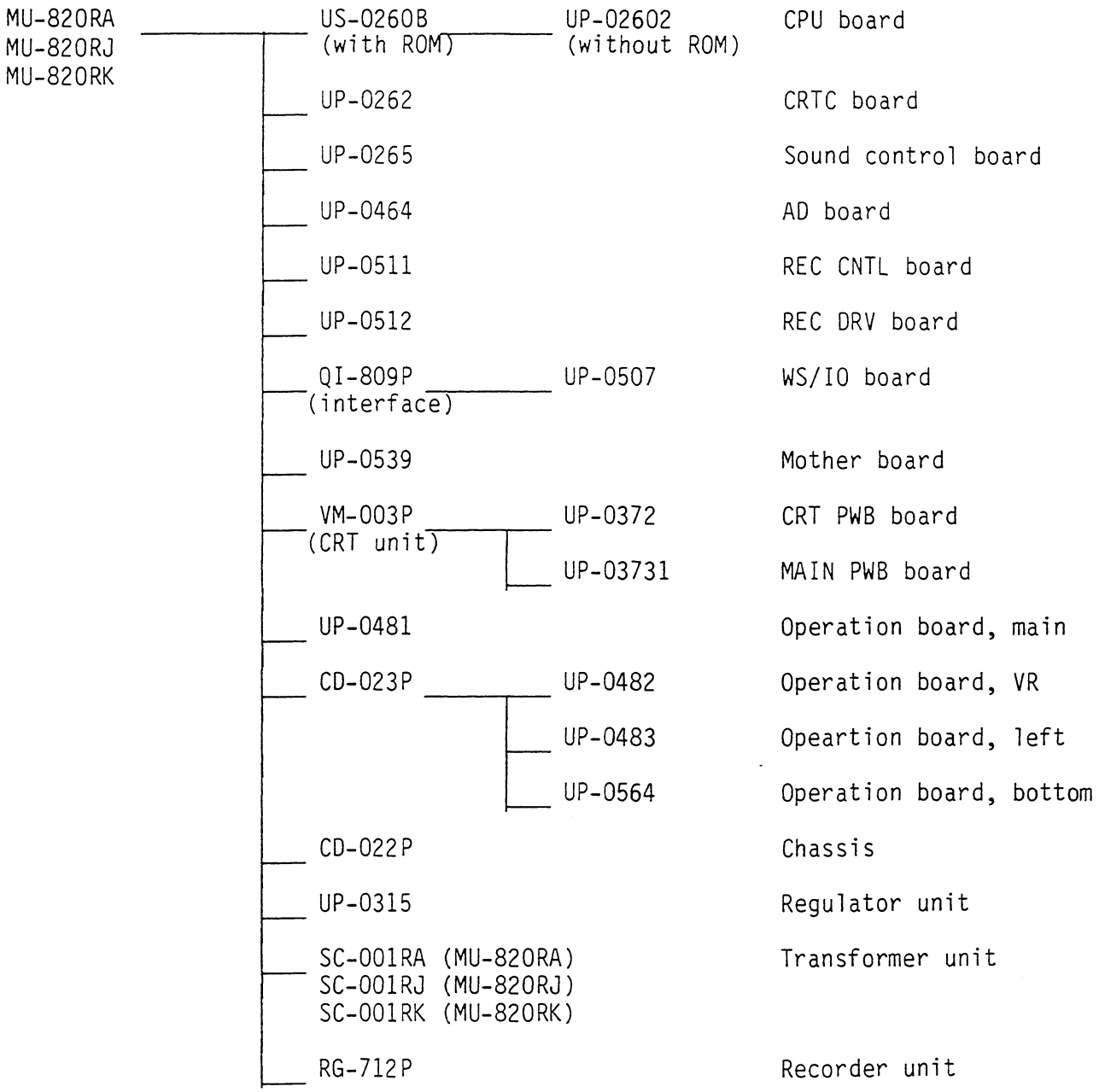
42. PARALLEL connector ..... Connector for output parallel format data

43. SERIAL connector ..... Connector for output serial format data

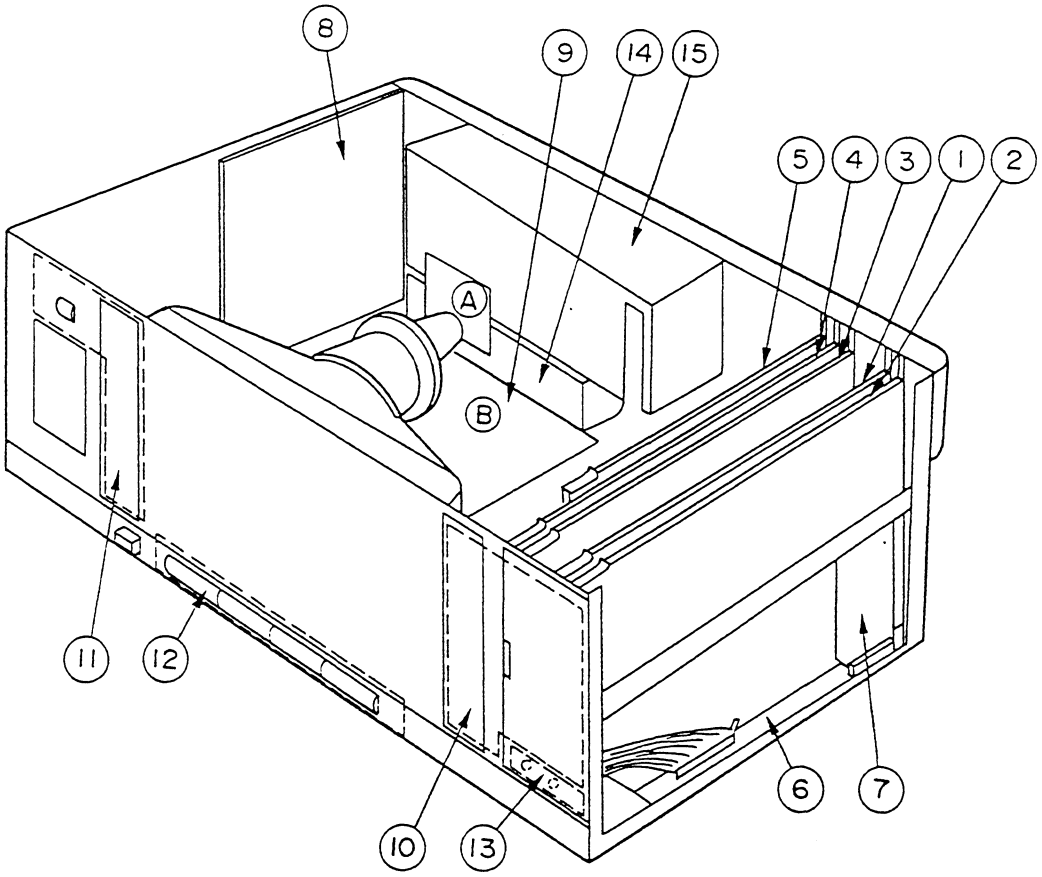
44. Keyboard interface connector ..... Connector for the keyboard

1.4 Composition

Central monitor main unit



1.5 Component location



Index No.	Model	Dscription
1	UP-02602	CPU board
2	UP-0262	CRTC board
3	UP-0464	AD board
4	UP-0511	REC CNTL board
5	UP-0507	WS/IO board
6	UP-0539	Mother board
7	UP-0265	Sound control board
8	UP-0512	REC DRV board
9	VM-003P	CRT unit
10	UP-0481	Operation board, main
11	UP-0483	Operation board, left
12	UP-0564	Operation board, bottom
13	UP-0482	Operation board, VR
14	SC-001RA/J/K	Transformer unit
15	UP-0315	Regurator unit
16	RG712P	Recorder unit

1.6 Explanation of system block

MU-820RA/J/K consists of the following blocks as shown on the next page.

1) CPU block (UP-02602)

Controls entire unit by the Micro Processing Unit (MPU) type 68000 mounted on the UP-02602 CPU board. Controls include AD block, COM (communication) block, Sound control block, operation block. Control of the built-in recorder and external recorder is done via the Global Memory.

2) AD block (UP-0464)

A/D converts analog waveform signals from the JJ-810R/820RA/J/K signal exchanger by the UP-0464 AD board. This A/D conversion is independent of the MPU on the CPU board and is always done automatically.

3) RECORD/COM block (UP-0511, UP-0512, RG-712P)

Communication between the JJ-810R/820RA/J/K signal exchanger is done by the UP-0511 REC CNTL board and RECORD block is composed of UP-0511 REC CNTL board and UP-0512 REC DRV board.

4) DISPLY block (UP-0262, VM-003P)

UP-0262 CRTC board generates video signals of waveforms, graphics, and characters for the display on the 12 inch vertical raster scanning CRT unit VM-003P.

5) POWER block (SC-001PA/J/K, UP-0315)

Supplies DC power voltages and an AC voltage to drive cooling fan.

<MU-820RA/J/K major board functions>

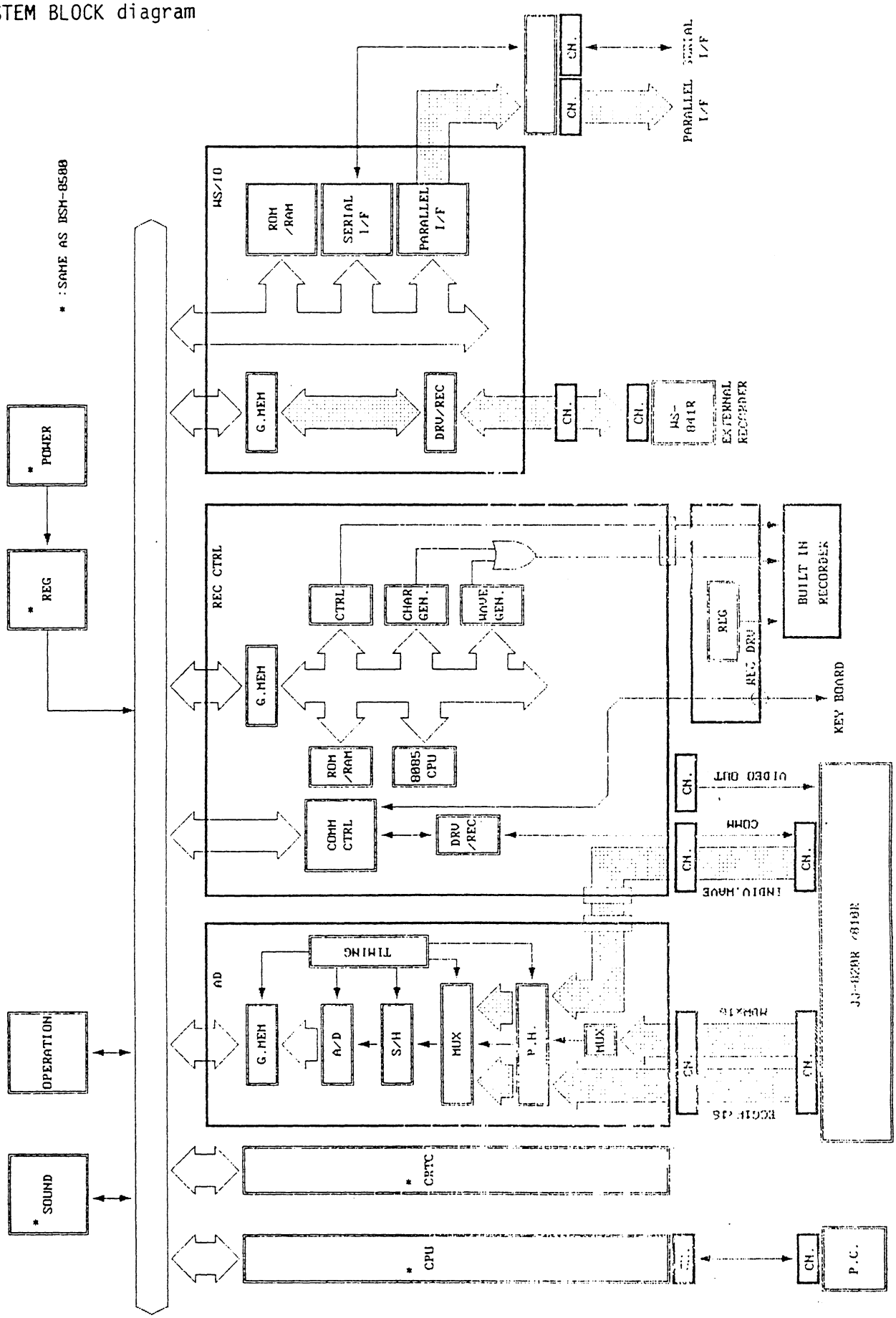
UP-0464 AD board ..... A/D conversion of analog waveforms from the signal exchanger

UP-0511 REC CTRL board . Control of the built-in recerder under the control of 8085 Sub CPU

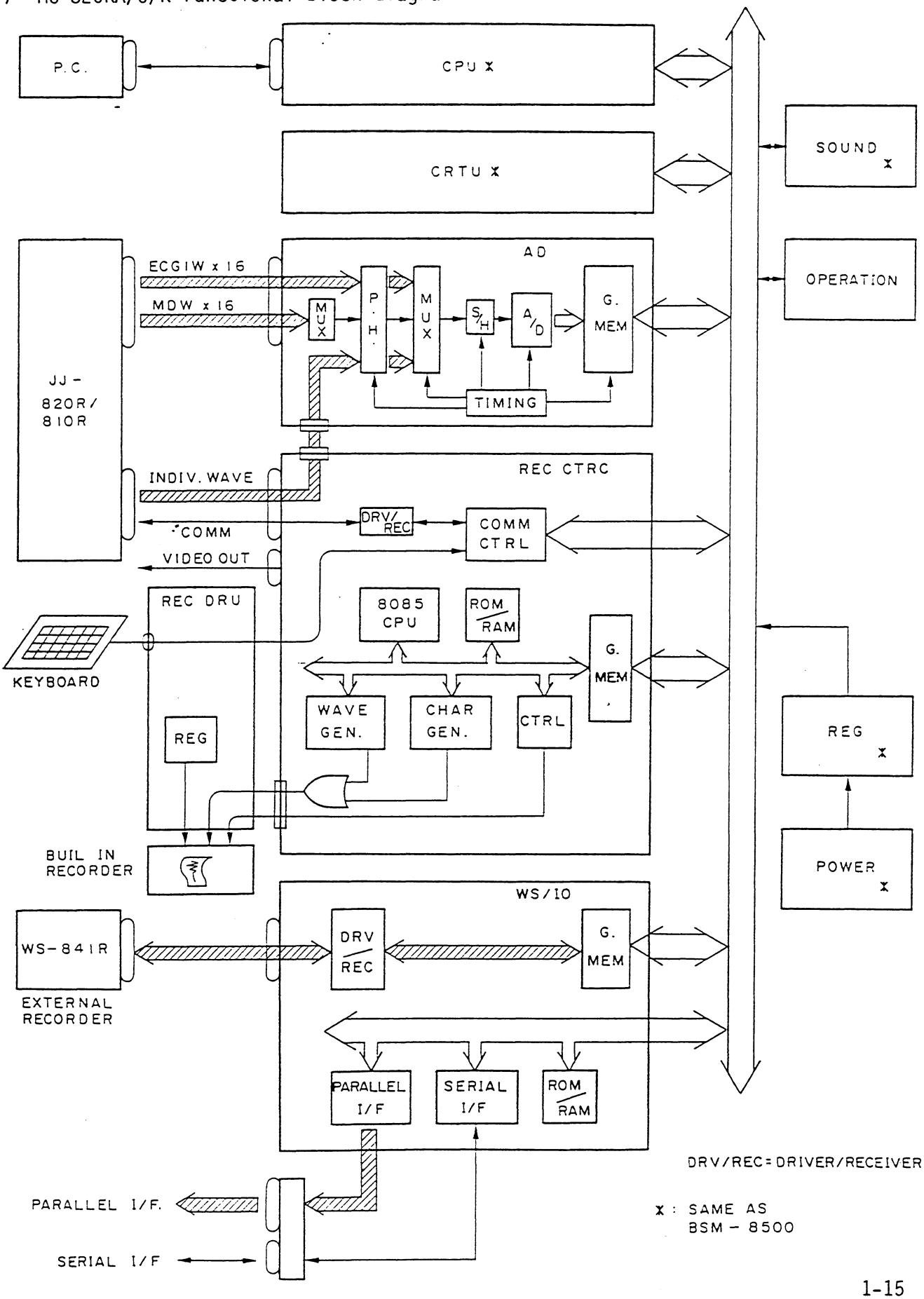
UP-0507 WS/IO board
(QI-809P interface) .... Interface between the unit and WS-841RA/J/K external thermal array recorder.
Control of parallel/serial Interface

UP-0512 REC DRV board .. Generation of regulated voltate for thermal head.
Generation of motor drive signal.
Sensing recorder status

SYSTEM BLOCK diagram



1.7 MU-820RA/J/K functional block diagram



1.8 signal flow

1.8.1 Analog waveform signal flow

1) Individual bed's waveforoms

Individual bed's waveform selected by the signal exchanger are transferred from the REC CNTL board and by the AD board slected on/off of peak hold, multiplexed and then A/D converted.

2) 16 beds' real time ECG1W signals

ECG1W waveforms from the 16 bedside monitors pass through the JJ without amplification to the MU central monitor main unit and by the AD board they are peak held, multiplexed and then A/D converted.

3) 16 beds' MDWs (delay ECG signals)

MDW waveforms from the 16 bedside montors pass through the JJ without amplification to the MU central monitor main unit and by the AD board one of the 16 MDW signals is selected and peak held, multiplexed and then A/D converted.

1.8.2 CRT display data signal flow

1) Waveforms

The formatted wave data on the DPU is converted to wave display data on the CPU board. the wave display data is written into the WAVE RAM on the CRTC board and displayed on the CRT screen through the video signal processor.

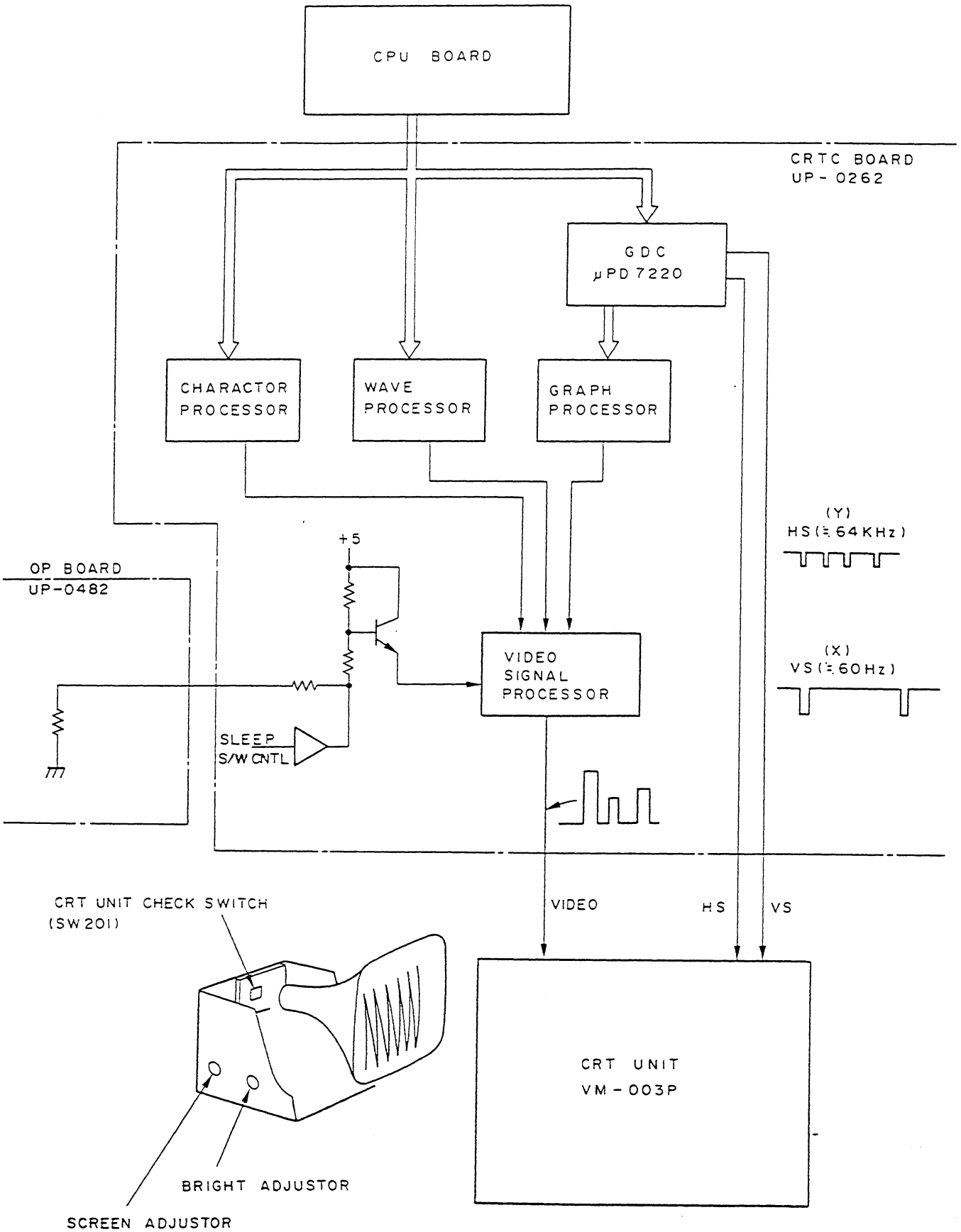
2) Graphics

The graphic display data is rwitten into the GRAPH RAM with the graphic display controller (GDC) on the CRTC board and displayed on the CRT screen through the video signal processor.

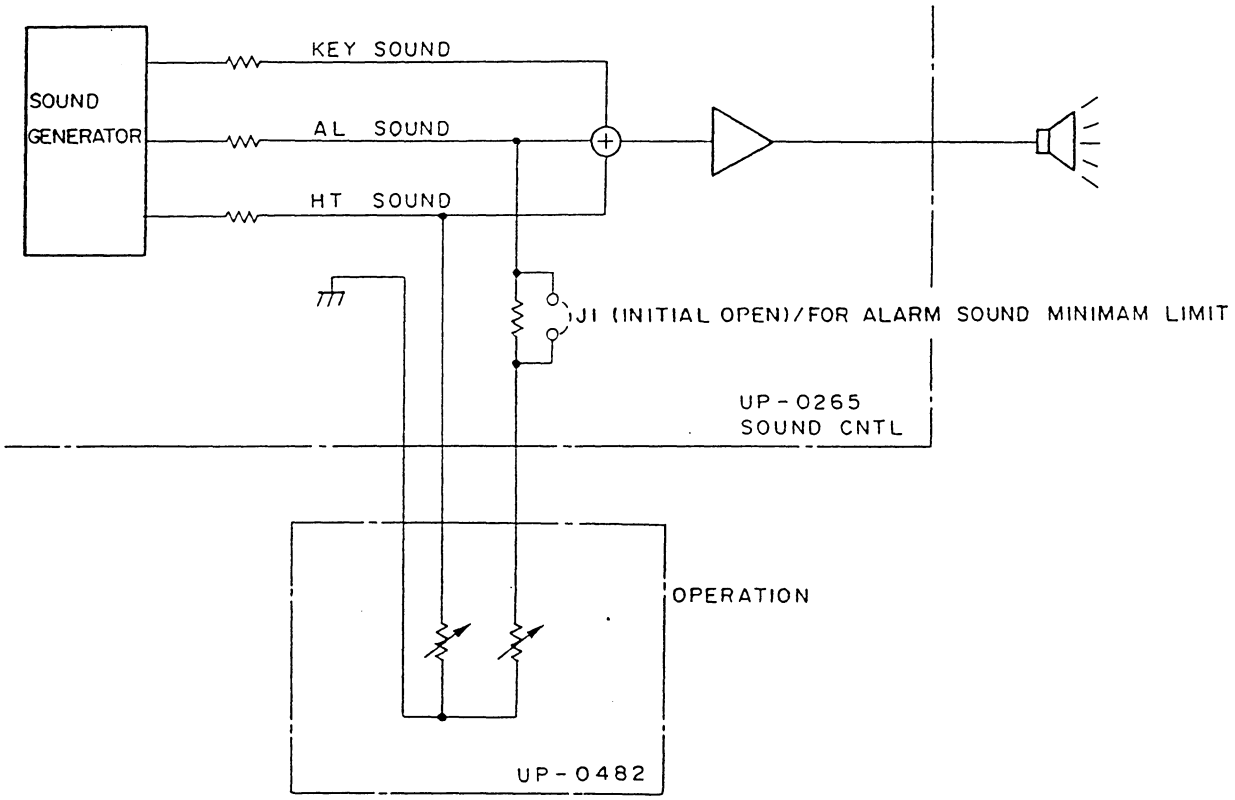
3) Characters

The character display data is directly written into the CHARACTER RAM on the CRTC board and displayed on the CRT screen through the video signal processor.

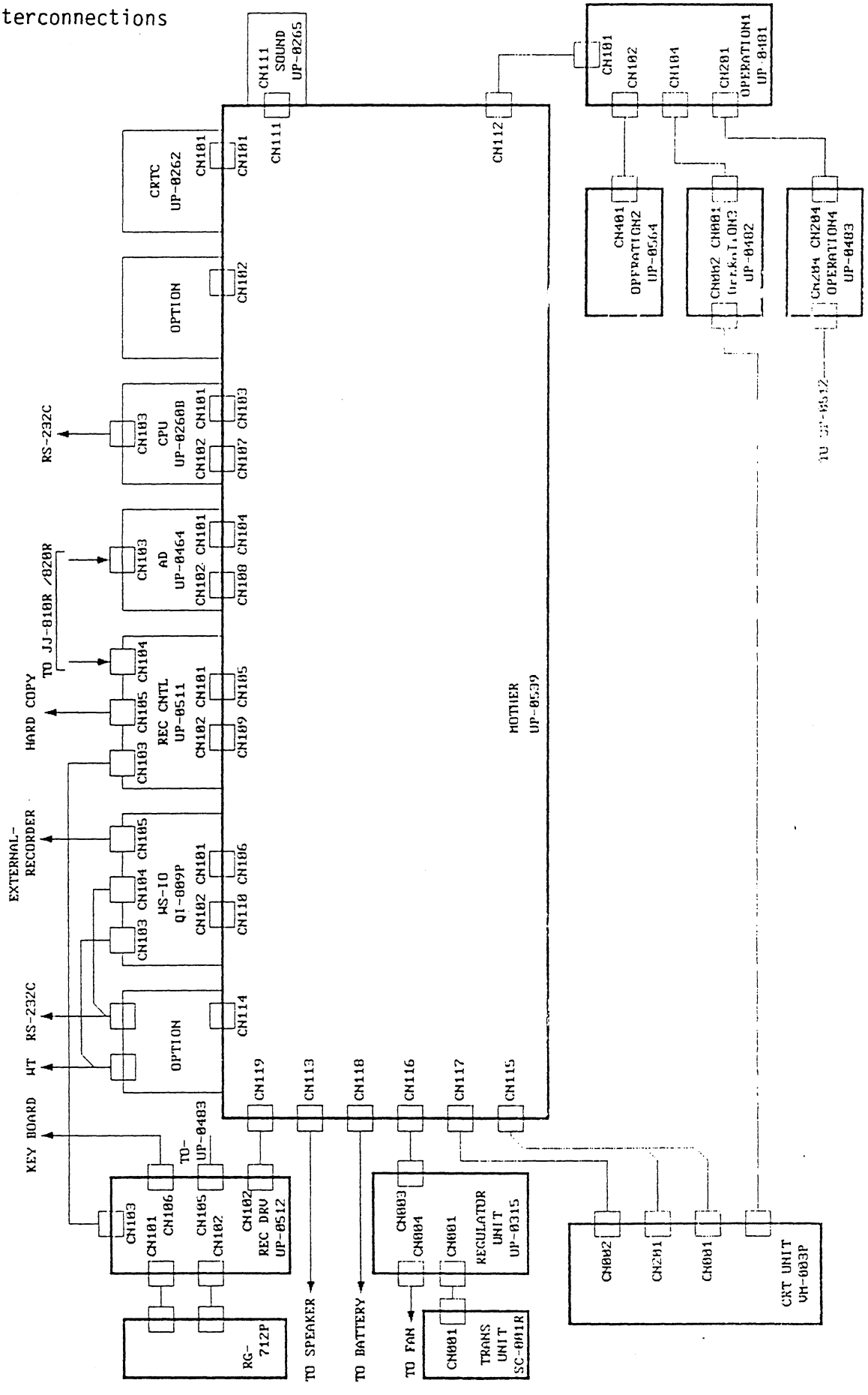
1.8.3 CPU-CRT signal flow



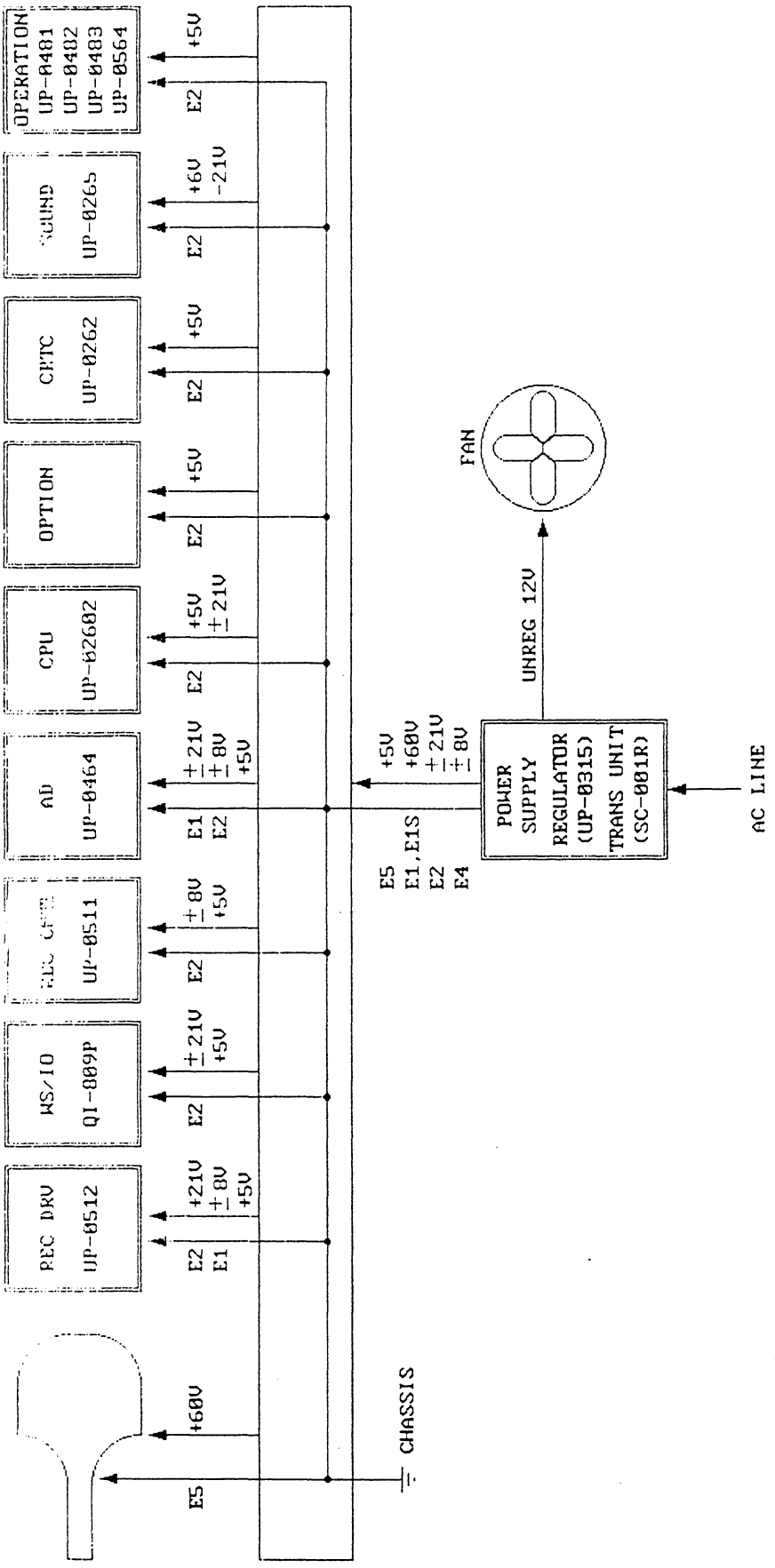
1.8.4 Sound signal flow



1.9 Interconnections



1.10 Power supply diagram



Section 2

2. Signal list

Symbol	Description
CPU board circuit diagram page 1/16	
CLK 8M	8MHz system clock
XIPL0-2	Interrupt Priority Level 0-2
XBERR	Buss Error
XRESET	Reset
XHALT	Halt
FC0-2	Interrupt encode signal of the MPC 68000
XAS	Address Strobe
R/XW	Read/Write signal HIGH: Read, LOW: Write
XUDS	Upper Data Strobe
XLDS	Lower Data Strobe
XDTACK	Data Acknowledge
XVPA	Valid Peripheral Address
D00-D15	Data bus 0-15
A01-A23	Address bus 1-23
CPU board circuit diagram page 2/16	
CLK 16M	16MHz clock
CLK 2M	2MHz clock
CLK 500K	500kHz clock
XASD	Delayed Address Gate
XRDU	Upper Byte Read control signal for ROMs & RAMs
XRDL	Lower Byte Read control signal for ROMs & RAMs
XWRU	Upper Byte Write control signal for SRAMs
XWRL	Lower Byte Write control signal for SRAMs
XIORD	Read control signal for SRAMs
XIOWR	Write control signal for SRAMs

CPU board circuit diagram page 3/16

IACK	Interrupt Acknowledge
VPP	Terminal for writing into ROM
XROMOSL-XROM3SL	ROM0 Select- ROM3 Select
A01D0-A03D	Address1-3 through D-type Flip-Flop (IC110)
XRAM0SL-XRAM7SL	RAM0 Select- RAM7 Select
XE2PSL	EEPROM slect
XRTCSL	Real Time Clock Select
XST/WTDS	Status or Watch Dog Timer Strobe Select
X179SL	8279 Select
X151SL	71051 Select
X154SL	71054 Select
XDS/LEDS	DIP Switchor LED Select
XIO	Gate control signal for I/O port selection decoder
XRAM	Gate control signal for SRAM selection decoder
XROM	Gate control signal for ROM selection decoder
XEBUS	System data Bus selct

CPU board circuit diagram page 4/16

XERESET	External Reset (Negative logic)
XWTDSTB	Watch Dog Strobe
XPDOWN	Power Down sigal (geneteted in UP-0315)
WTDSTOP	Watch Dog Stop
XWTDLAMP	Watch Dog Lamp
ERESET	External Reset
WTDERR	Watch Dog timer Error
XINT1-XINT7	Interrupt 1-7

CPU board circuit diagram page 5/16

XIACK1-2	Interrupt Acknowledge1-2

CPU board circuit diagram page 6/16

I79IRQ	Interrupt Request signal from 8279 (IC176)
151RxRDY	Receive Ready of 8251
151TxRDY	Transmit Ready of 8251
154OUT2	71054 counter Out 2
XI54ACK	Acknowledge from 71054
I6242STD	Standard clock of Timer 6242
XI62ACK	Acknowledge from 6242
INT10-INT17	Interrupt 10-17
XIACK10-XIACK17	Interrupt Acknowledge 10-17

CPU board circuit diagram page 11/16

VB	Batery Voltage
XRTCSL	Select signal for Real Time Clock (IC169)
XE2PSL	EEPRPM Select
XPWDWN	Power Down (generated in UP-0260)

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TxD	Transmit Data
RTS	71051 Request to Send (IC172)
RxD	Receive Data
DSR	71051 Data Set Ready signal (IC172)
DTR	71051 Data Transmit Ready signal (IC172)
CTS	71051 Clear To Send signal (IC172)
FG	Frame Ground
SG	Signal Ground

CPU board circuit diagram page 13/16

RL0-RL7	8279 Return Line 0-7
OUTA0-3	8279 Out data line A0-A3
OUTB0-3	8279 Out data line B0-B3
SL0-SL3	8279 Scan Line 0-3
SHIFT	8279 Shift signal
CNTL/STB	8279 Control or Strobe

CPU board circuit diagram page 14/16

CEXT	Terminal of power backup capacitor

CPU board circuit diagram page 15/16

XDATA00- XDATA16	System Data bus
XADDR01- XADDR23	System Address bu (negative logic)

CPU board circuit diagram page 16/16

XINT10- XINT50	Interrupt 10-50
CLKSAMPL	Timing Clock to synchronize wave data transfer (CPU-CRTC)
XDTACKB	Data Acknowledge (system bus)
XASB	Address Strove (system bus)
XUDSB	Upper Data Strobe (system bus)
XLDSB	Lower Data Strobe (system bus)
R/XWR	Read/Write signal (system bus)

CRTC board circuit diagram page 1/11

XHS	Horixzontal synchronizing signal for IC401
XVS	Vertical synchronizing signal for IC401
XA17	Address-17 to generate control signals
XINT40-50	Interrupt 40-50
XHSYNC	Horizontal synchronizing signal for IC401
XVSYNC	Vertical synchronizing signal for IC401
XCRTCS	CRTC board select signal

CRTC board circuit diagram page 2/11

XFLD	Field signal
2VS	30Hz clock (approx. 30Hz)
INTRC	Control signal to generate address signal for wave RAMs
XWBLINK	Wave Blank signal
XCRADTK	Character Data Transfer acknowledge signal
OE1	Wave Output Enable signal from wave composite
RDCLK	Address to Read Wave RAM
WSEL1-3	Select signal for 3 pcs. of Wave RAMs
HGATE	Gae control signal for horizontal synchronization
XWCE	Chip Enable signal for Wave RAMs
XWOE	Output Enable sigal for Wave RAMs
WA12	Address terminal (A12) of 3 pcs. Wave RAMs
WA14	Address terminal (A14) of 3 pcs. Wave RAMs
WA131	Address terminal (A13) of Wave RAM1 or Wave RAM3

CRTC board circuit diagram page 2/11

WA133	Address terminal (A13) opf Wave RAM3
XWWE1-3	Write Enable signal for Wave RAMs
XWG1-3	Gate control signal for Wave RAM buffer IC407-IC409
XGDCWR	Write control signal for GDC
XCGDISP	Clock to latch Character/Graphic Display control signal
XWDISP	Wave Sisplay control signal for IC501
XSTREG	Register Start signal for addredd controller (IC401)
XGDCRD	Read control signal for GDC

CRTC board circuit diagram page 3/11

GD0-GD15	Bit name of Graph Data (2 byte)
BLANK	Blank signal on GDC for CRT sceeen
VSYNC	Vertical Synchronization signal
HREF	Hsync/Refresh GDC output
DCLK	Dot Clock (64MHz)
2DCLK	32MHZ Clock
XWE	Graph data Write Enable signal

XOE	Output Enable signal for Graph RAM (IC210-IC213)
XG	Graph Gate control signal
X8M	8MHz clock (inverted 8M)
GLD	Graph Load (positive logic)
XGLD	Graph Load (negative logic)
LRAS	Latched RAS
WLD	Timing control signal for Wave data Load
XBLNKD	Delayed Blank signal

CRTC board circuit diagram page 4/11

HS	Horizontal Synchronzation signal
XCRLD	Character Data Load signal
VS	Vertical Synchronization signal

CRTC board circuit diagram page 5/11

XRAS	
GRDISP	Control signal for Graphic Display (P/S converter)
GRAD	Serial format Graphic Data for video signal
SL	Control signal for Select address for display or access
QA-QE	Clock for character control
CC0-CC11	Address line for Character RAM
L1-L9	timing control signal from Counter (IC317)

CRTC board circuit diagram page 7/11

CHLD	Control signal for serial Character Data Load
XCOE	Character Output Enable signal
XCWE	Character Write Enable signal
XCG	Character Gate control signal
CAB	Gate control signal for Character data
QC	4MHz clock for Character control
RV	Reverse control signal for character
BL	Blink control singal for character
HT	Half Tone control signal fo rcharacter

CRTC board circuit diagram page 8/11

CH0-CH7	Parallel format Character data
CD0-CD15	Data line for Character RAM
CA3-CA14	Address line for Character generator ROM
CB12-CB15	Data for Character attribute control

CRTC board circuit diagram page 9/11

WD11-WD28	Wave Data line for wave composite (IC501)

CRTC board circuit diagram page 10/11

WH	Serial format Wave data with normal (High) intensity
WL	Serial format Wave data with Low intensity

CRTC board circuit diagram page 11/11

BRITE	Intensity level from Brightness control on UP-0482
GRAD	Serial format Graphic Data for video signal
VIDEO	Video signal for CRT unit

Operation board circuit diagram page 1/1

LPTSW1-4	Left patient switch1-4
RPTSW1-4	Right patient switch1-4
LOSSW1-4	Left record switch1-4
ROSSW1-4	Right record switch1-4
XLOS1-4	Left record LED drive signal1-4
XROS1-4	Right record LED drive signal1-4
XLAL1-4	Left alarm LED drive signal1-4
XRAL1-4	Right alarm LED drive signal1-4
XLPT1-4	Left patient LED drive sgnal1-4
XRPT1-4	Right patiet LED drive signal1-4

AD board circuit diagram pages 1/19 - 12/19

W1- W28	Waveform1-28 after filter
MDW1-16	Delayed ECG1-16
W1A-W25A	Switch line1-25 to discharge capacitor of peak hold circuit
W1B-W25B	Switch line1-25 to discharge capacitor of peak hold circuit
PW1-PW25	Waveform 1-25 after peak hold circuit

AD board circuit diagram page 13/19

XDPSEL	Chip select signal of dual port RAM (IC801, IC802)
XCNRD	Read signal of IC803
XIOWR	Write signal of IC804 output port

AD board circuit diagram page 14/19

64K	64kHZ clock
32K	32kHz clock
28K	28kHz clock
8K	8KHz clock
MA0-MA10	Divided clock signals of 16kHz (Ex. MA0;4kHz)

A/DC	Symbol of A/D convert Control signals
XADWR	Write signal to A/D converter
S/XH	Sapmle/Hold signal to A/D converter
R/XC	Read/Convert signal to A/D converter
SMAA-SMAD	Switch signalA-D to discharge capacitor of pelk hold circuit
LMA0-LMA2	Switch signal0-2 to discharge capacitor of peak hold circuit

AD board circuit diagram page 16/19

P2-P6	MDW1-MDW16
M2-M6	Level shifted signal of P2-P6
SEL1-SEL3	Multiplexer control singal1-3
LMA0-LMA2	Multiplexer control signal0-2

AD board circuit diagram page 17/19

+5VREF	+5V reference voltage
-5VREF	-5V reference voltage

AD board circuit diagram page 18/19

DB0-DB11	Data bus between A/D and dual port RAM
X	Time shared output signals of PW1-PW25
P0	Synchronization signal XHT

WS/IO board circuit diagram page 1/6

A0-A23	Address bus A0-A23 inside WS/IO board
D0-D15	Data bus D0-D15 inside WS/IO board
XCS2	Chip select signal of IC301 (uPD72001C)
XCS1	Right port chip select signal of IC401 (MB8421)
XCS0	Chipselect signal of IC201 (uPD71055C)
XCS3	Chip select signal of IC201, IC211 (27C512)
XCS4	Chip select signal of IC212, IC213 (62256)
XCS5	Chip select signal of IC214, IC215 (62256)
CS	Chip select signal of IC307 (assert)
IORST	Reversed XIORST signal

WS/IO board circuit diagram page 2/6

XRDL	Lower byte read signal
XRDU	Upper byte read signal
XWRL	Lower byte write signal
XWRU	Upper byte write signal

WS/IO board circuit diagram page 3/6

DATA0-7	Data bus for parallel printing
XSTROBE	Strobe signal for printer
XACK	Acknowledge sigal of printer
BUSY	Busy signal of printer
PE	Paper Empty signal of printer
XERROR	Error signal of printer
SELECT	On-line command signal
XRST	Reset signal line of WS printer

WS/IO board circuit diagram page 4/6

XBUSY	Right port Busy signal of IC401 (MB8421)
TxDA	Transmit line of serial data
RxDA	Receive line of serial data
RTSA	Request To Send signal line
CTSA	Clear To Send signal line
DCDA	Data Carrier Detect sigal line

WS/IO board circuit diagram page 5/6

A0L-A10L	Left port Address bus of IC401 (MB8421)
XRAMC	Left port Chip select signal of IC401 (MB8421)
XMEMR	Left port Read signal of IC401 (MB8421)
XCOMW	Left port Write signal of IC401 (BM8421)
XBUSY	Left port Busy signal of IC401 (MB8421)
XINT	Left port Interrupt signal of IC401 (MB8421)
XRESET	Reversed XRST signal
+12V	+12V power voltage
-12V	-12V power voltage

REC CNTL board circuit diagram page 1/8

XDPSEL	Dual Port select signal
XCOMRD	Communication controller Read signal
XCOMWR	Communication controller Write signal
XIORST	Reset signal from main CPU to IO
XRD	Read signal
XWR	Write signal
XBUSYR	Busy signal from right dual port
8M	8MHz clock signal

REC CNTL board circuit diagram page 2/8

TxD	Transmit Data signal for keyboard
RxD	Receive Data signal for keyboard
XRTY	Retry signal for keyboard
XDSR	Data Set Ready signal for keyboard
XRDY	Ready signal for key board
XA/B	New/Old comunication signal switch signal
A/XM	Address/Message signal
ENABLE	New communication system Enable signal
XHSCLR	hand Shake Clear signal
XERST	Reset signal to slave CPU
XRST	Reset signal to keyboard
RD	Receive Data line
RD RET	Receive Data Return line
XBUSY2	Busy2 line
XBUSY2 RET	Busy2 Return line
XBUSY1	Busy1 line
XBUSY1 RET	Busy1 Return line

REC CNTL board circuit diagram page 3/8

RST7.5	Reset7.4 to 8085
XDPINT	Interrupt signal from dual Port RAM
DMAWAIT	Print signal
XCS	Symbol of Chip Select signals
XBUSYL	Busy signal from left dual port
XRAM1-2	Chip Select signal 1-2 of RAM
XDPRAM	Chip Select signal of Dual Port RAMN
XIRAM	Chip Select signal of print RAM
XSEL1-2	Chip Select signal 1-2 of I/O
XTIM1-2	Chip Select signal 1-2 of uPD71054
DOS-D7S	Data bus of Sub CPU (8085)
AOS-A15S	Address bu of Sub CPU (8085)
SOD	Serial Out Data of Sub CPU (8085)
XSRD	Read signal of Sub CPU (8085)
XSWR	Wtite signal of Sub CPU (8085)
IO/XM	I/O or Memory select signal

REC CNTL board circuit diagram page 4/8

TC	Terminal count signal
OUTO	Count output sinal of uPD71054 (original of entire system timing)
XRST7.5	Interrupt sigal to Sub CPU (8085)
QA	Couter output signal
XSHIFT	Shift clock sigal of record data
XQA	Reversed QA signal

DMACLK	Clock signal for DMA
XSRLD	Load signal of Shift Register
XDMAWAIT	Wait signal to 8085 at DMA operation
DMAWAIT	Reversed XDMAWAIT signal
XYO	RCLK of Shift register with latch
ADCLK	Clock signal for A/D (500kHz)
XSTB	Strobe signal to thermal head
G1	Gate signal for OUTO signal generation by uPD71054
2M	2MHz clock

REC CNTL board circuit diagram page 5/8

VTEMP	Thermal head temperature signal
EOC	End Of Conversion signal of A/D conveter

REC CNTL board circuit diagram page 6/8

DATA	Data for thermal head
DW1-DW2	Wave Data1-2

REC CNTL board circuit diagram page 7/8

BSTPSW	Record Switch signal
MK	Mark detect signal
XOPN	Magazine Open detect signal
XPE	Paper Empty detect signal
ENB	Thermal head Enable signal
XSTART	Record Start signal
XSPD25	Paper Speed 25, 50mm/sec select signal

REC CNTL board circuit diagram page 8/8

XHS	Horizontal Synchronization signal
XVS	Vertical Synchronization signal
VIDEO	Video signal
+21VP	+21V output voltage protected by resistor
-21VP	-21V output voltage protected by resistor

REC DRV board circuit diagram page 1/4

S+5	+5V voltage for revolution sensing circuit
SEN	Revolution sensing singal
PCNT	Revolution Control Pulse
PLED	Drive signal for Paper detect LED
MLED	Drive signal for Mark detec LED

PAPER	Paper detect signal
TOP	Mark on paper detect signal (Top Of File)
SW	Magazine open Switch sigal
SPD25	25mm/sec paper feed Speed signal
XSTART	Recorder Start signal
STPSW	Stop Switch signal
BSTPSW	REC/STOP Switch signal
XPE	Paper Empty detect signal
XLED	Drive signal ofpaper empty indicator LED
MK	Mark detect signal
XOPN	Magazine Open detect signal
XREC	Record ready signal
VTH	Thermal head power voltage

REC DRV board circuit diagram page 2/4

ETH	Thermal head ground
M+	Plus terminal of DC motor
M-	Minus terminal of DC motor
XRST	Keyboard Reset signal
XRDY	Ready signal for keyboard
RxD	Reveive Data signal for keyboard
TxD	Transmit Data signal for keyboard
XDSR	Data Set Ready signal

REC DRV board circuit diagram page 3/4

XSTB	Strobe signal for thermal head
ENB	Enable signal for thermal head
DATA	Data for thermal head
XSHIFT	Shift clock signal for thermal head
TH1-TH2	Thermistor resistance1-2
HSTB	Buffed XSTB signal
XHENB	Buffed ENB signal
XSIN	Buffed DATA signal
CLK	Buffed SHIFT signal
VDD	+5V thermmal head power voltage
VTEMP	Thermal head temperature signal

Section 3

3. Circuit descriptions

		Page
3.1	US-0260B (UP-02602) CPU board	3-2
3.2	UP-0262 CRTC board	3-13
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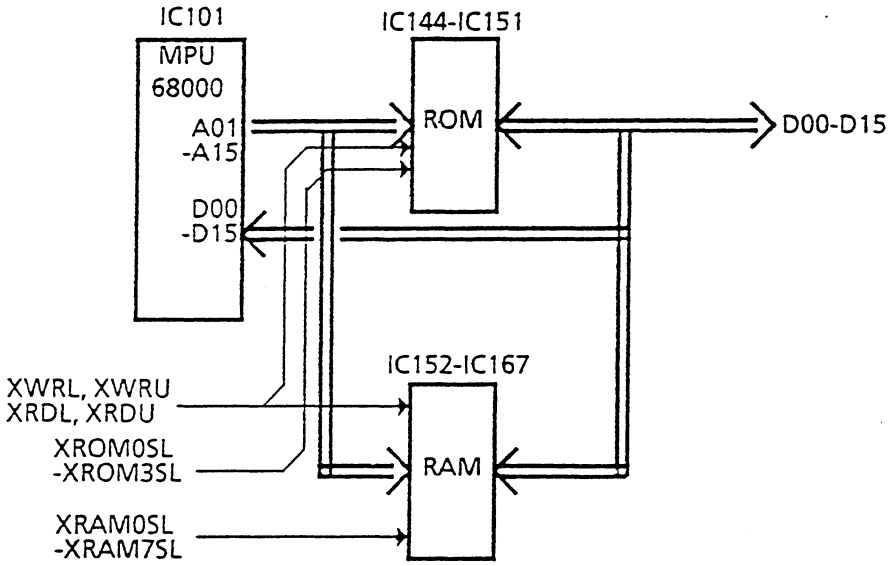
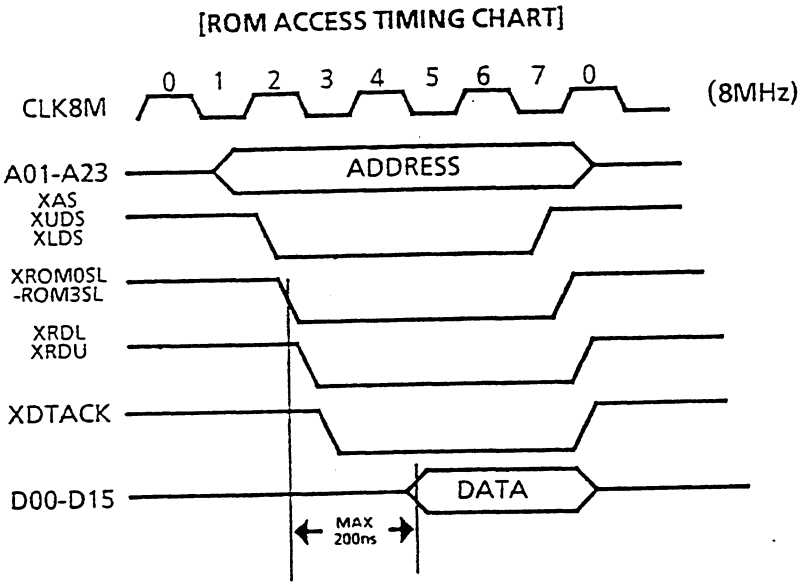
3.1 US-0260B CPU board

3.1.3 MPU/ROM/RAM cirucit

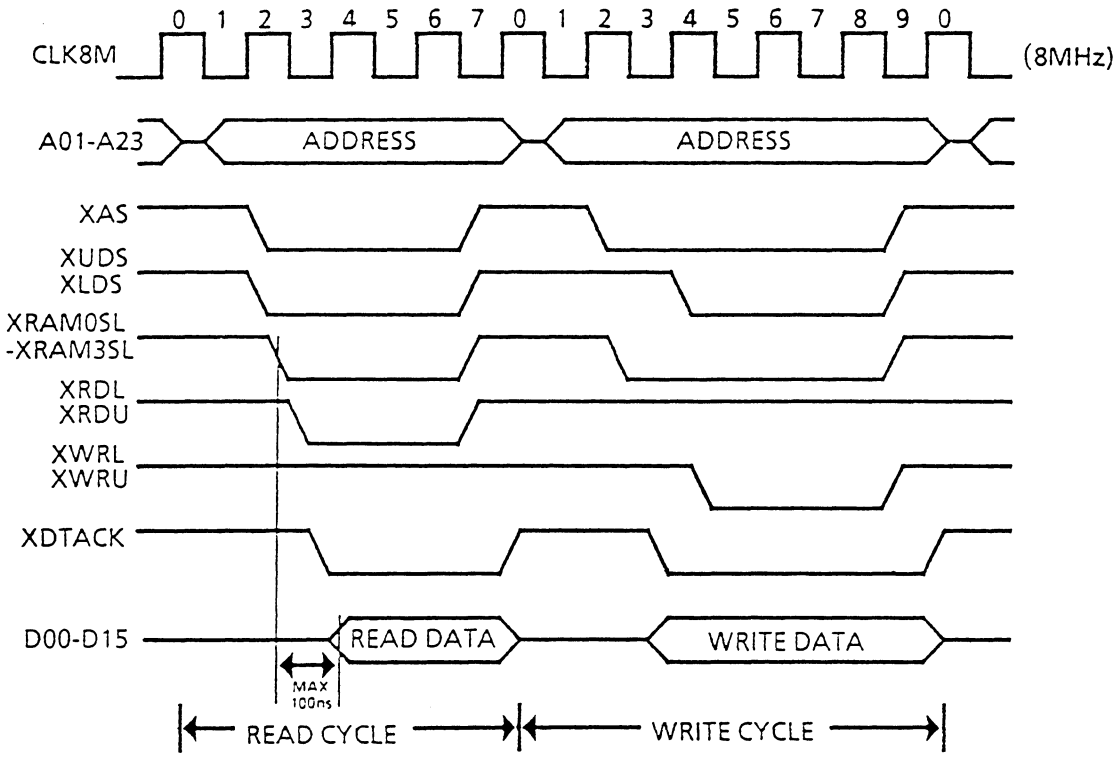


The Micro Processor unit MPU(IC101, 68000) accesses RMs (IC-144-151) or RAMs (IC152-167) as follows:



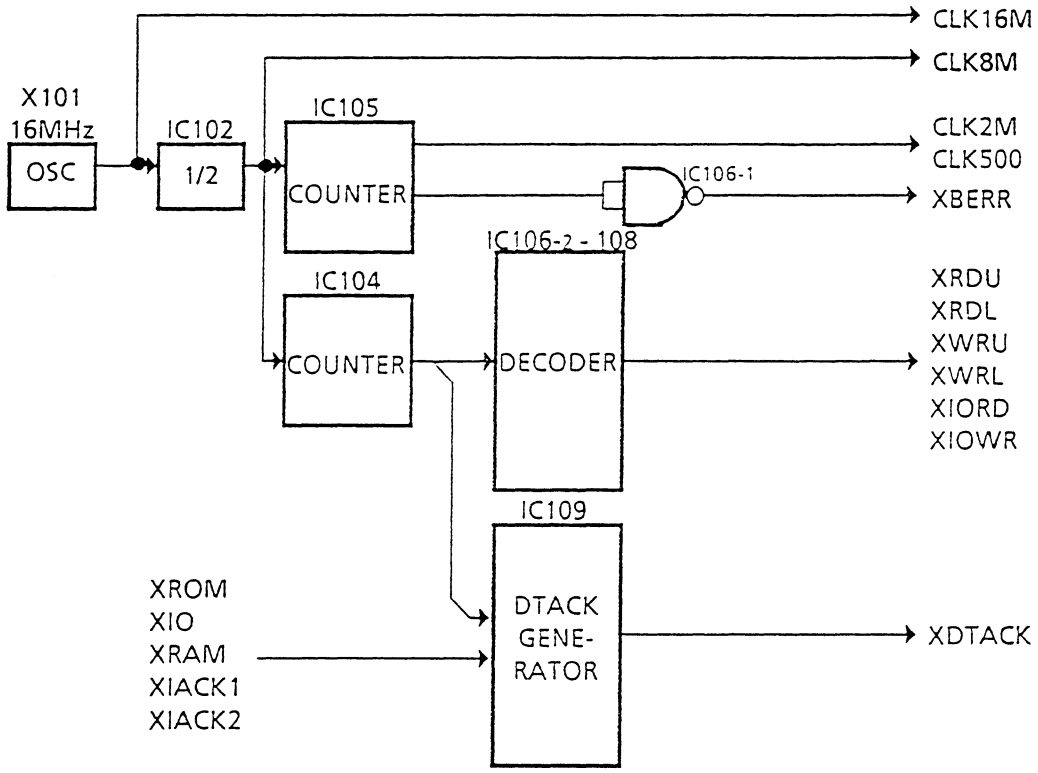
The ROM provides 512kbyte memoty and 200ns access time. The total memory capacity of the ROMs (IC144-151) is 256kwords.

[RAM ACCESS TIMING CHART]



The RAM provides 256kbyte memory and 100ns access time. The RAMs (IC152-159) of which the total capacity is 128kwords, are actually mounted. The RAMs (IC160-167), of which the cadditional capacitry is 128kwords, can be mounted in memory expansion.

3.1.2 Timing control circuit

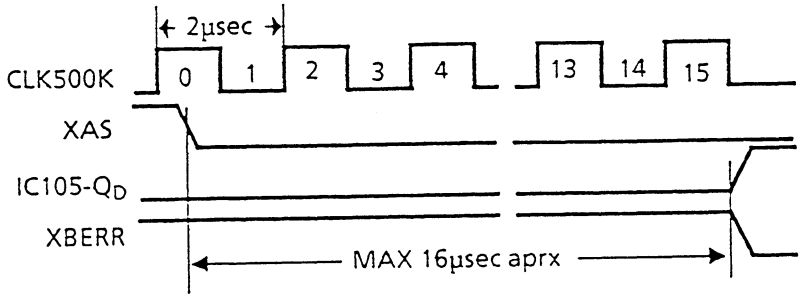


The above circuit generates clock signals, Read/Write control signals, and Data Trasnfer Acknowledge signals. Moreover, the circuit provides a Bus Eror Detector (IC105, 106-1).

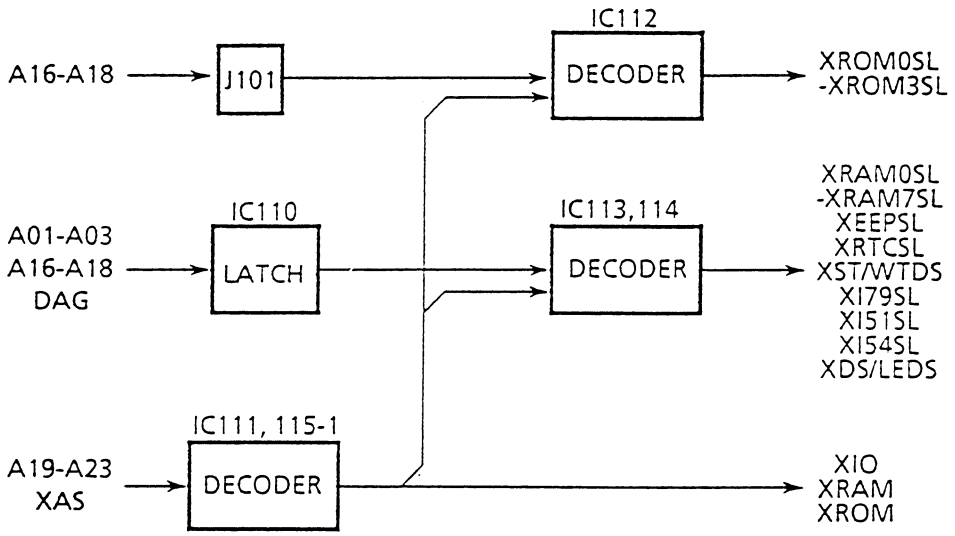
[Bus Error Detector]

The detector informs the MPU (IC1010) on this board of any trouble found in the bus cycle during an execution. If Address Strobe signal XAS is not negated on Counter (IC105-2) within 16usec due to the following condition, Buss Error signal XBERR is outputted to the MPU through the IC106-1.

DTACK signal is not asserted.
VPA signal is not asserted.



3.1.3 Address decoding Circuit



Address signals A01-03 and A16-21 are decoded by the following decoders:

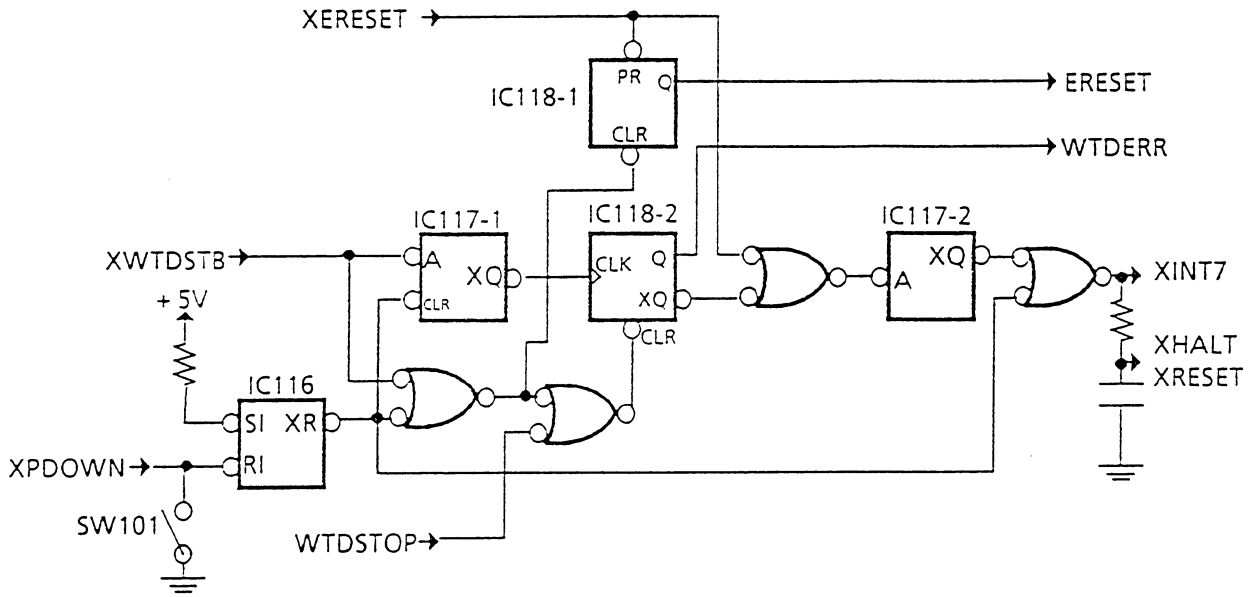
IC112 generates ROM selection signals XROM0SL-XROM3SL.

IC113 generates RAM selection signals XRAM0SL-XRAM37L.

IC114 generates the other I/O chip selction signals.

IC111 generates the above gate control signals, X10, XRAM, or AROM, which are elements ofthe XDACK signal.

3.1.4 Reset/Watch Dog Timer/Power Down detector circuit



1) Reset circuit

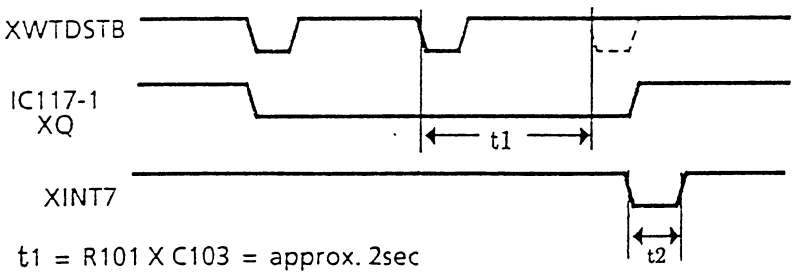
When external reset signal XRESET is asserted by pressing the SELF CHECK key on the operation panel, the following signals are generated:

The output (Q) on External Reset Satatus Flip/Flop (IC118-1) is set to high, assertion of ERESET sigal.

Interrupt request signal to MPU (IC101), XINT7 is asserted for 50usec.

Reset signal to MPU (IC101), XRESET (XHALT) is asserted for 50usec after 10usec delay from XINT7 assertion.

2) Watch Dog Timer circuit



t1 = R101 X C103 = approx. 2sec

t2 = (RA109-5) X C104 = 47µsec

If MPU (IC101) runs away, this circuit resets the MPU as follows:

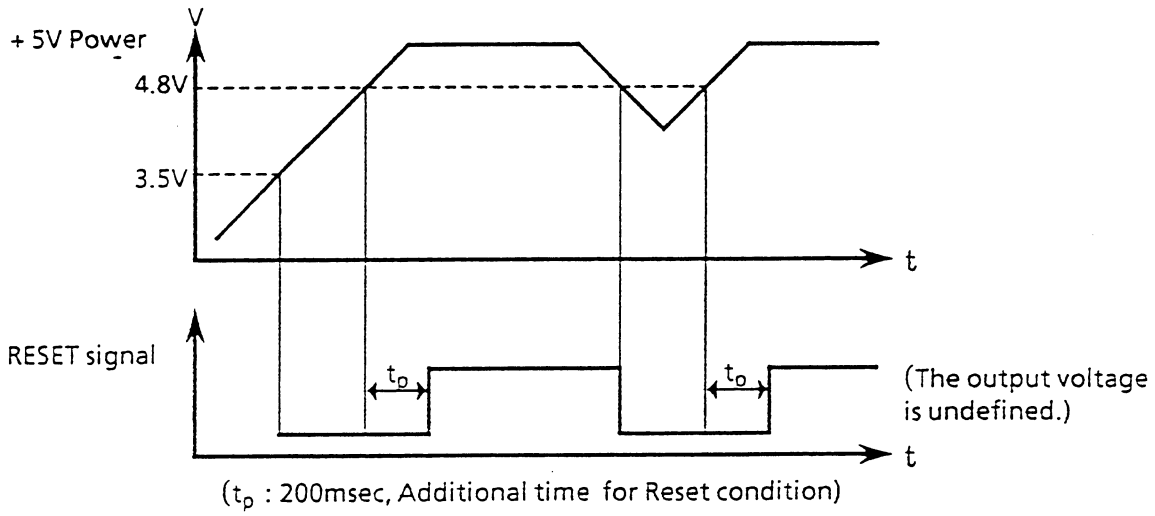
Under normal conditions the output (XQ) on One-shot multi. (IC117-1) keeps low since IC117-1 receives the Watch Dog Strobe signal from MPU XWTDSTB within 2sec. however, under abnormal conditions, XQ on IC117-1 is charged to high since IC117-1 dose not receiver XWTDSTB signal. The following signals are generated:

The output (Q) on Watch Dog Timer Error Status F/F (IC118-2) is set to high (assertion of WTDERR signal).

XINT7 signal is asserted for 50usec.

XRESET (XHALT) signal is asserted for 50usec after 10usec delay from XINT 7 assertion.

3) Power Down detection circuit



(t_D : 200msec, Additional time for Reset condition)

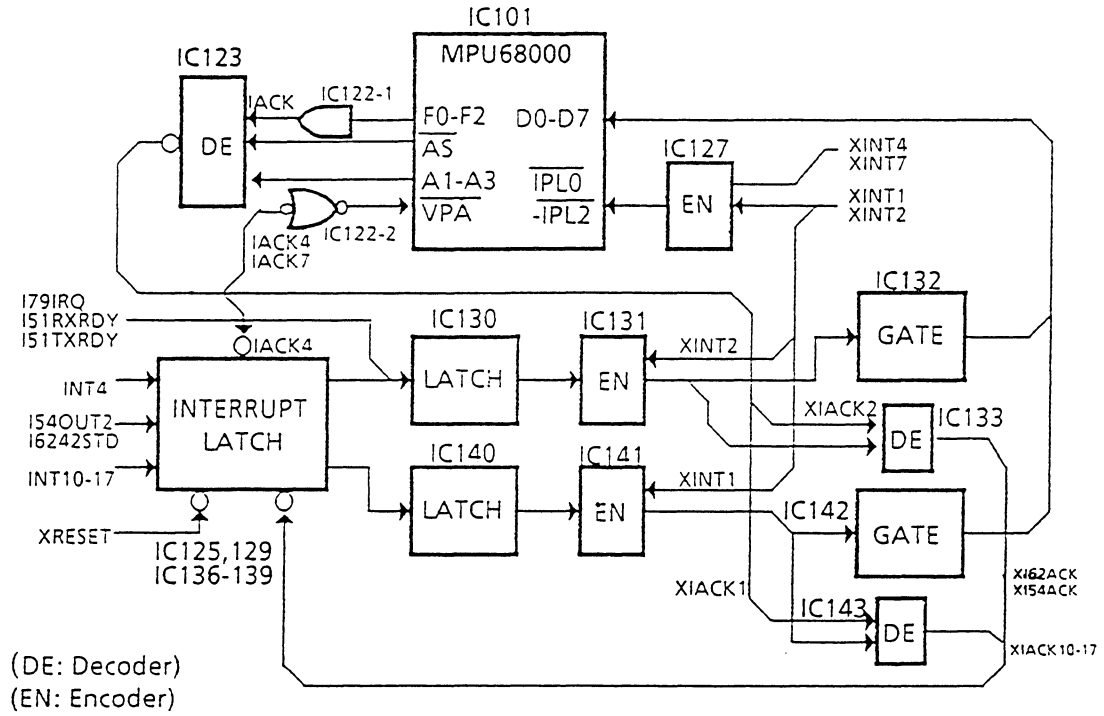
If the +5V power charges to 4.8V or less in Power Down signal, XPDOWN is set to low and Power Down detector (IC116) generates reset signal (active-low) ro IC118-1 & 2 until 200msec passes after the +5V power returns to 4.8V.

When the power is turned on, XPDOWN signal is set to low level and IC116 keeps reset signal until 200msec passes after the +5V comes to 4.8V.

In the both cases, INT7 signal is asserted for 50usec and XRESET isngal is also asserted for 50usec after 10usec delay from XINT7 assertion.

When the switch (SW101) is turned on, SW101 functions as XPDOWN signal is inputted since the reset input (RI) on IC116 is active-low.

3.1.5 Interrupt control circuit



The interrupt request signals are divided into Auto-vectored interrupt and Vectored interrput while being divided into seven levels according to the fllowing table. Level-7 provides the highest priority.

Table of interrupts

Prioity	Vector No.	Intrerrupt	Explanation	Generated in
7	Auto	XPDOWN WTDERR XERESET	Power down Watch dog error External reset	CPU board
6			No use	
5			No use	
4	Auto	INT40	CRT frame Sync (16msec)	CRTC board
3	Auto	INT30	Communication	REC CNTL board
2	4D 4C 4B 4A 49	16242ST 1540UT2 151TxRDY 151RxRDY 179IRQ	Real time (1sec) 71054OUT2 (10msec RS232C TxRDY RS232C RxRDY key-in	CPU board
1	47 46 45 44 43	INT17 INT16 INT15 INT14 INT13	HS A/D INTR Global memory Keyboard	REC CNTL board AD board REC CNTL board REC CNTL board REC CNTL board

1) Auto vectored interrupt

The Interrupt is processed by using a vector generated in the MPU. The interrupt request signal INT4 or INT7 is inputted to the Interrupt Control terminals IPL0-2 on the MPU through Interrupt Latch (IC125) or Priority Encoder (IC127).

The IC 125 latches the INT4 signal by triggering the positive-going edge of the signal and resets th output with XRESET or Interrupt Acknowledge signal IACK.

The IC127 generates the interrupt request to the IPL0-2 on the MPU whenever a higher interrupt priority level than before is inputted.

The IC122-1, IC123 and IC-122-2 generate Interrupt Acknowledge signals IACK and XIACK1/2 and Auto-vector recognition signal XVPA.

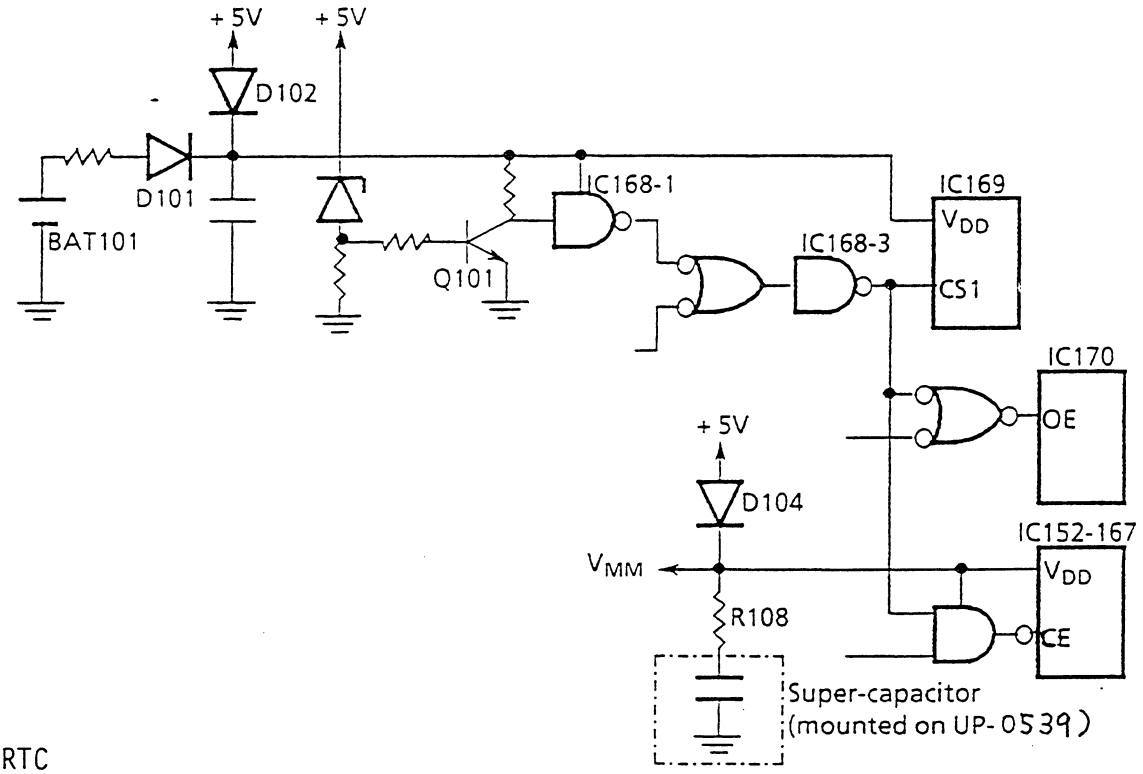
2) Vectored Interrupt

The interrupt is processed by acquiring a vector number from the others by the MPU. The interrupt level signal XINT1 or XINT2 is inputteed to IPL0-2 on the MPU through the Priority Encoder (IC127). An interrupt request signal is changed to vector number signal(D0-7) through IC129/136-139, IC130/140, IC131/141 and Gate (IC132/142).

The AND (IC122-1) and Decoder (IC123, 133/143) generate interrupt acknowledge signals. The interrupt latch (IC129, 136-139) resets the output by triggering the positive-going edge of the XRESET signal or each interrupt acknowledge signal.

The IC132/142 generates the vector number according to an interrput request signal and then the vector number is aquired by the MPU.

3.1.6 Real Time Clock (RTC)/Battery/EEPROM



1) RTC

The real time clock IC (IC169) can be read or written by the MPU from second to year. IC169 provides four data lijnes, four address lines, three control lines and two lines of chip select signal for comunication with the MPU.

2) Battery & Super-capacitor

The lithium battery (BAT101) provides a backup function to prevent a data break in IC169 due to a power failure. The BAT101 supplies the IC169 through D101 with the +3V power instead of the +5V power when the +5V power is lower than the battery power. the super-capacitor (C101, 102) mounted on the mother board (UP-0539) is always charged by the +5V power. The super-capacitor provides a backup function to prevent a data break in Static RAMs (IC152-167) when power fails. The super-capacitor supplies the Static RAMs through D104 with the charged power instead of the +5V power when the +5V power is lower than the charged power. When the +5V power starts to drop, the transistor (Q101) reaches cut-off condition and NAND IC (IC168-3) outputs low (0V) through IC168-1, 2. therefore, IC169, IC152-167 and IC170 work as follows:

IC169: The write mode is disabled since chip enable terminal CS1 is set to Low, Nagation.

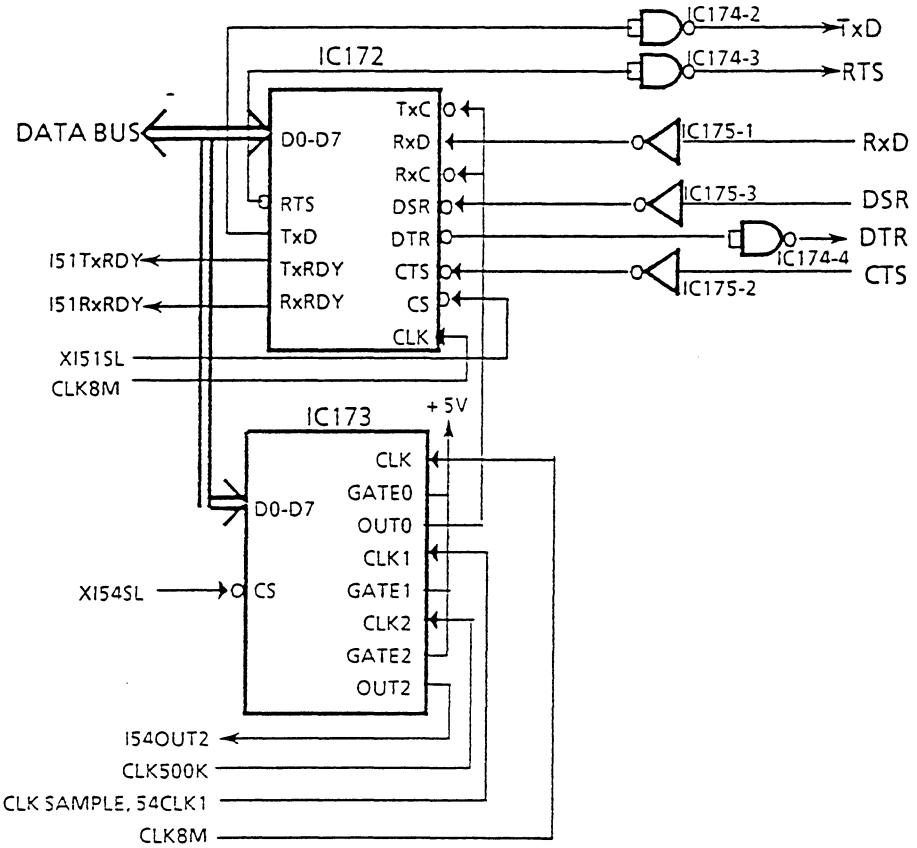
IC152-167: The write mode is disabled since chip enable terminal CE is set to High, negation.

IC170: When the power is within 3.0V to 4.85V, the write mode is disabled since output enable terminal OE is set to Low, assertion. When the power is between 0V to 3V, the write mode is disabled owing to itself.

3) EEPROM

The Electrically Eraseable Programmable ROM (IC170), X2816A, provides 2kbyte memory capacity and 300nsec access time.

3.1.7 RS232C Control circuit



1) Serial Interface Controller (IC172) uPD71051C

The followiing items are controlled by software:

Baud rate; 1200, 2400 or 9600 bits/sec
Data length; 7 or 8 bits
Number of stop bit; 1 or 2 bits
Operation mode; Synchronous or Asynchronous mode
Parity bit; Even or Odd

[Transmit operation]

When a parallel data is inputted at D0-7 on IC172, the data is converted to serial data. The serial data is transmitted from Transmit Data terminal TxD. When the data trasnmission is completd, TRansmit Ready terminal TxRDY is set to High so as to interrupt the MPU operation and wait for the next parallel data.

[Receive operation]

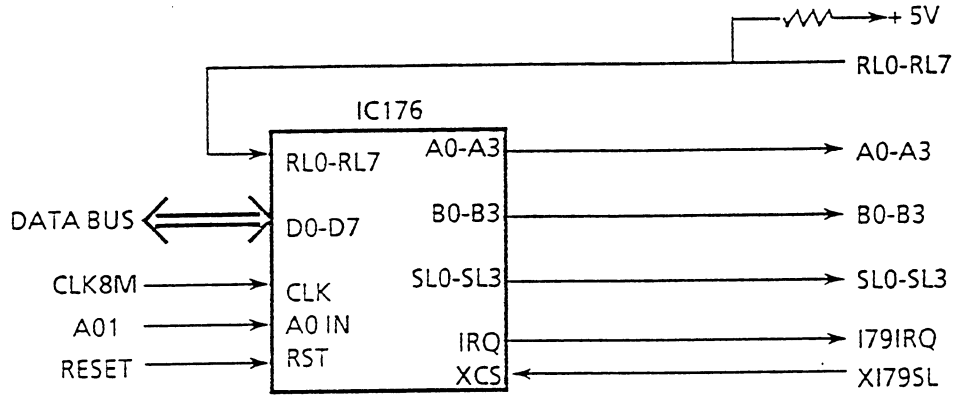
When a serial data is received at Receive Data termianl RxD, the data is converted in parallel data for the MPU. When the data reception is completed, Receive Ready terminal RxRDY is set to High so as to interrupt MPU operation and request the reception of the parallel data of the MPU.

2) Programmable Intermal Timer (IC173), uPD71054C

The IC173 consists of three sets of 16-bit counters controlled by software. The IC173 is used for the following purposes:

To control baud rate for RS232C communication,
To generate periodic interrupt to the MPU (10msec interval),
To synchronize data transfer timing with wave display timing on CRTC board (UP-0262) by counting 8msec interval clock, 154CLK1.

3.1.8 Key/Sound Control circuit



The keyboard/Display controller (IC176) 8279 controls the UP-0265 sound control board and UP-0481, UP-0483, and UP-0564 operation boards.

The opearation mode is controlled by sofware. In MU-820RA/J/K, the opeartion mode is fixed to Decode, Scan, and Sensor Matrix mode.

Scan lines SL0-SL3 are outputted to scan key switches on the UP-0481/0483/0564. Moreover, SL0-SL2 are branched to latch B0-B3 signals on the UP-0481.

Return lines RL0-RL7 are inputted to inform the MPU of each key switch status on the UP-0481. Output signals A0-A3 are outputted to control LEDs on the UP-0481. Output signals B0-B3 are outputted to generate each sound on the UP-0265.

3.2 UP-0262 CRTC board

3.2.1 General

The CRTC board consists of the following circuits:

1) Buffer circuit
The circuit is composed of a buffer for the system bus.

2) Decoder circuit
The circuit generates signals to select each IC and to control Wave RAMs.

3) Graph Processing circuit

3-1) Graph Timing-1/2 circuit
The circuit generates sweep signals and control signals for the Graph circuit with the Graphic Display Conroller (GDC).

3-2) Graph circuit
The circuit generates grapic display data (serial data) for Graphic display on CRT.

4) Character Processiing circuit

4-1) Char.-1 circuit
The circuit selects addresses (Display address or System address to be accessed by the MPU on CPU board).

4-2) Char.-2 circuit
The circuit generates control signals for Char.-3 circuit.

4-3) Char.-3 circuit
The circuit generates character display data (serial data) according to data in the Character RAM.

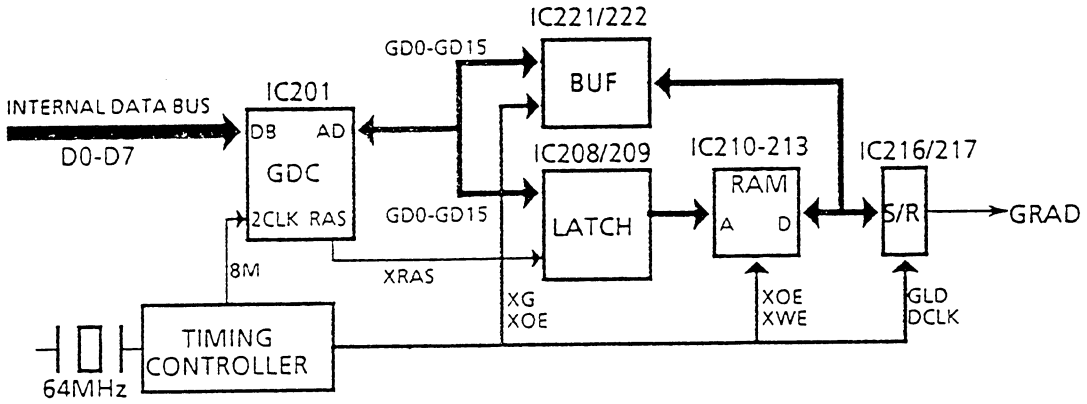
5) Wave Processing circuit

5-1) Wave-1 circuit
The circuit selects address (Display address or System address).

5-2) Wave-2 circuit
The circuit generates wave display data (serial data) accrding to data in Wave RAM.

6) Video Signal Processing circuit
The circuit generates Video signal by mixing the graphic display data, character display data, and wave display data.

3.2.2 Graph Processing circuit



The circuit provides Bitmap Graphics to store the bits according to each display dot (pixel). The operation cycle consists of Display cylce and Read/Modify/Write cycle. In the Display cylcle, the circuit reads graphic data on the Graphic RAM (IC210-213) under control of the GDC (IC201) and converts the graphic data (parallel data) to graphic display data (serial data) with the Shift Register (IC216/217).

In the Read/Modify/Write cycle, the circuit reads/modifies/writes the graphic data on the Graph RAM unde control of the GDC with Command & Parameter transferred from the MPU on the CPU board to the GDC.

The Graphic Display Controller (GDC) provides the following functions:

1) DISPLAY
To calculate the address for display on CRT and read out the graphic data after transfering the calculated address to Graph RAM.

2) READ/MODIFY/WRITE Preprocessing
To calculate the address for the process according to Command & Parameter from the MPU.

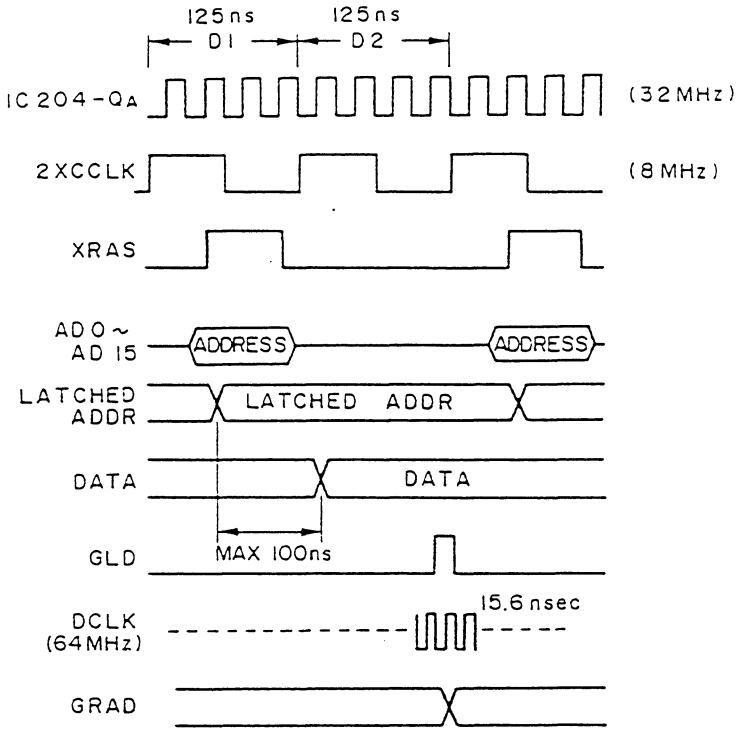
3) READ/MODIFY/WRITE Execution
To read/modify/write the graphic data after transfering the calculated address to Graph RAM.

4) Synchronizing Signal Generation (VSYNC/BLANK/HREF)
To generate the synchronizing signals for display to be XHS/XVS signals and to control the timing of the display cycle or Read/Modify/Write cycle.

a) Display cycle

The timing chart is shown below. The operation cycle needs 2 clocks (D1 and D2) of 2XCCLK in the 2 clocks, 16 dots are displayed on the CRT.

The GDC (IC201) outputs an address for the cycle to the Graph RAM through the Address/Data bus line (GD0-GD15). The display address is latched by IC208/209 with the Row Address Strobe (R.A.S.) signal. The latched address specifies a graphic data on the Graph RAM. The graphic data is acquired by the Shift Register ((IC216/217) synchronized with the Load sigal GLD. The acquired daa is converted to graphic display data (serial data) GRAD by the Shift Resister.

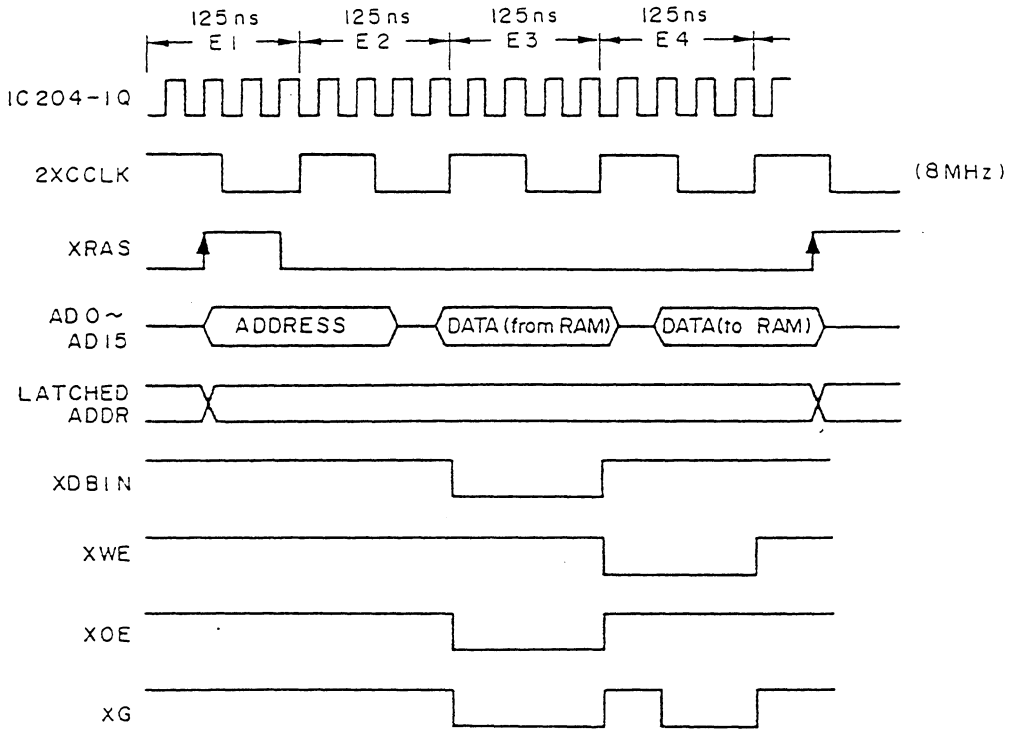


b) Read/Modify/Write cycle

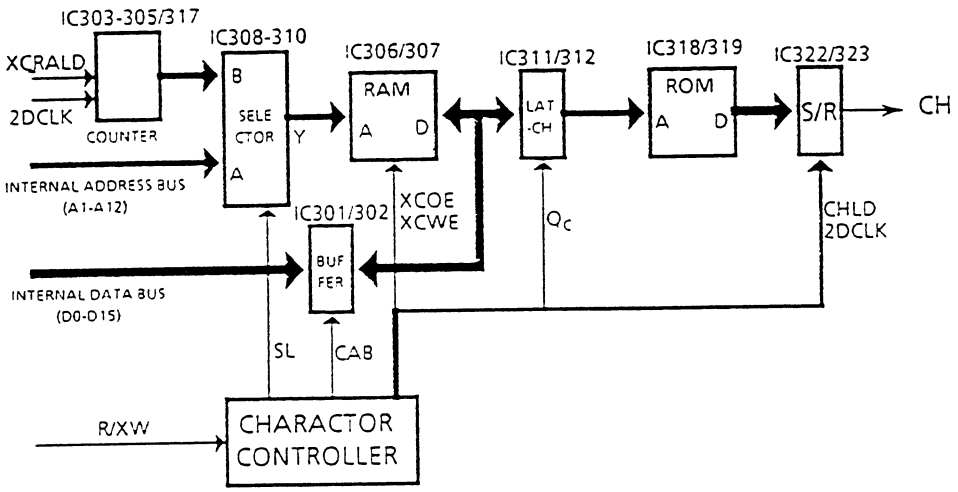
The timing chart is shown below. The operation cylce needs 4 clocks (E1 to E4) of 2XCCLK.

The GDC (IC201) outputs an address for the cycle to the Graph RAM through the Address/Data bus line (GD0-GD15). The GDC outputs an XRAS signal to latch the address and an XDBIN signal to transfer the data on the address to the Address/Data bus line synchronously. The GDC acquires the data at a middle point in the XDBIN signal during low level and modifies the data and writes the modified data into the Graph RAM with an XWE signal.

When the modification is needed, the GDC writes the same data into the Graph RAM as the readout data.



3.2.3 Character Processing circuit



The circuit transfers character display data to the CRT unit (VM-003P) by reading out character bit patterns stored in the Character Generator ROM (C.G.ROM), IC318/319 according to character code data written into the Character RAM (IC306/307).

One code data (2 bytes) is related on one character (20 lines x 32 dots). The code data is directly written into the RAM by the MPU on the CPU board. The operation cycle consists of a Display cycle and Read/Modify/Write cycle. the timing chart is shown in the next page.

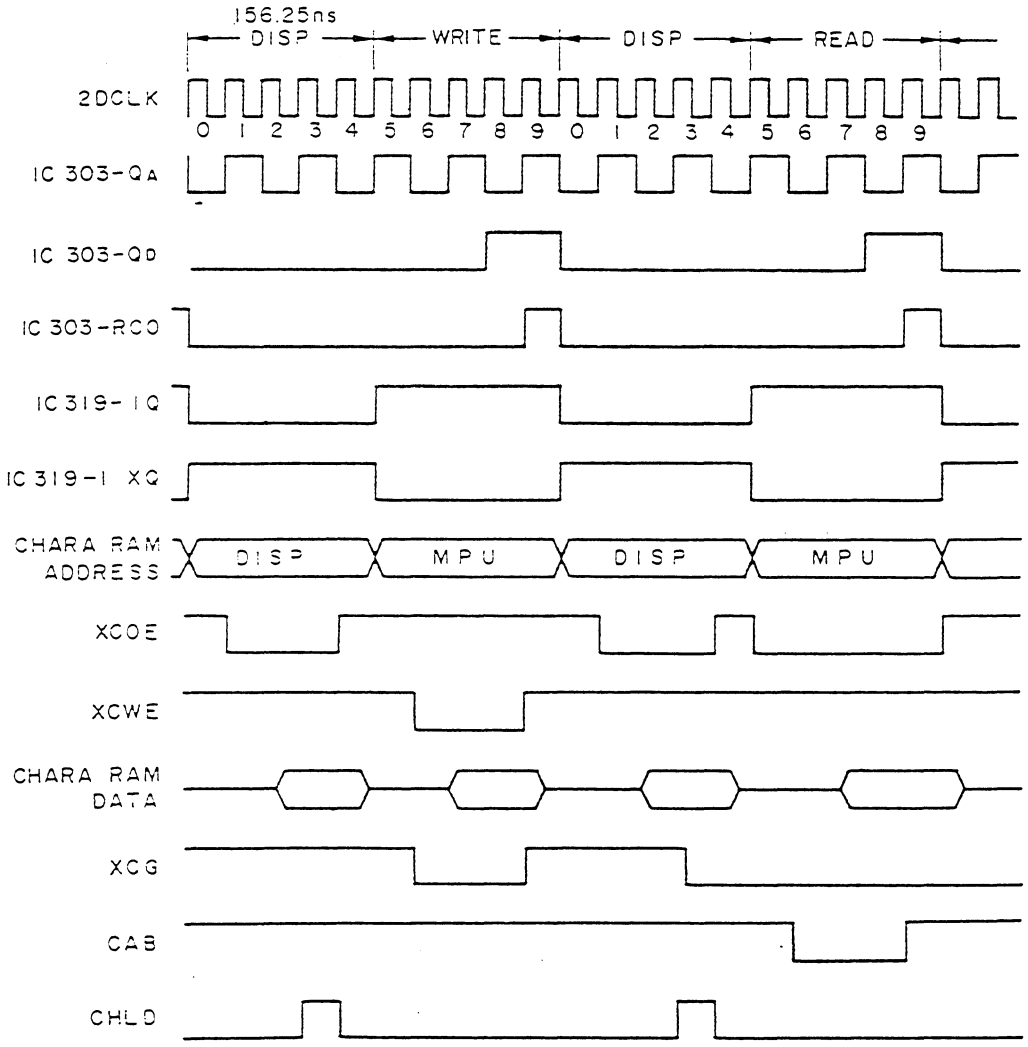
1) Display cycle

The counter ((IC317/303-305) generates an address for display on the CRT. The address specifies a character code on the Character RAM. The character code is transferred to the CGROM as the address through the Latch (IC311/312). The CGROM outputs a character pattern data according to the character code. The character pattern data (parallel data) is converted to the character display data (serial data) by the Shift Register (IC322/323) synchronized with the Load signal CHLD.

2) Read/Write cycle

The address specified by the MPU board is transferred to the Character RAM every 5 clocks of 2DCLK through the Selector (IC308-310). The character code data is transferred through the Buffer (IC301/302).

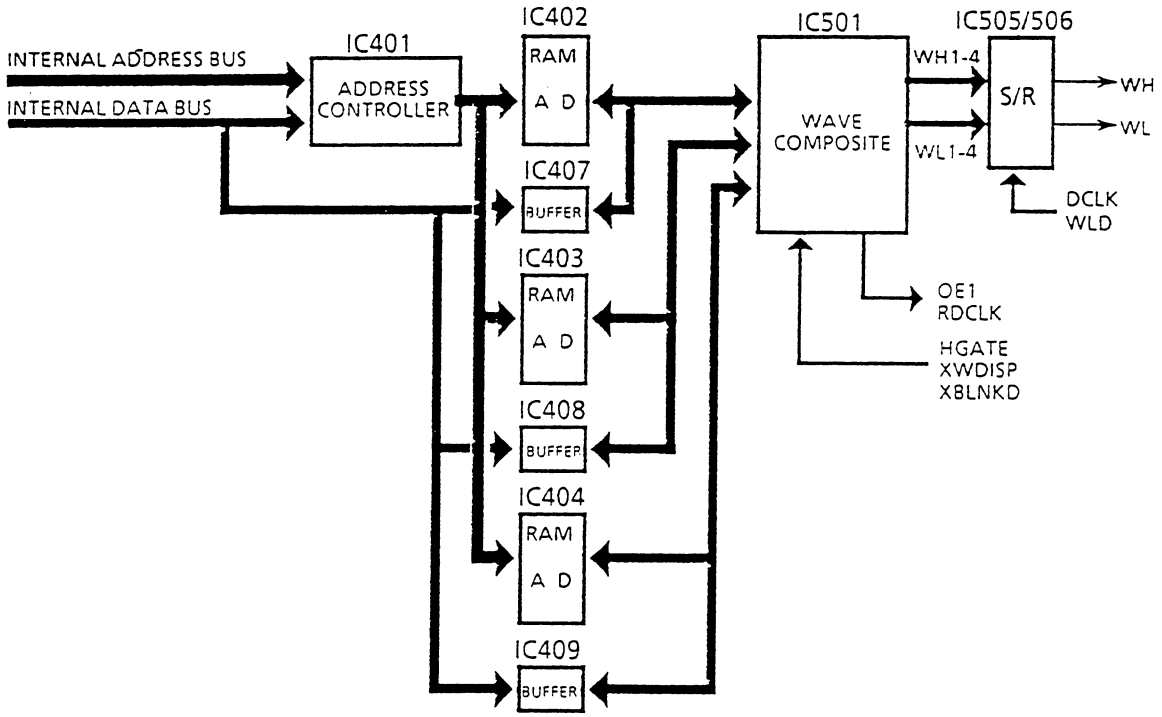
The buffer is desabled to transfer the character code data from the MPU to the Character RAM during the Display cycle.



The Character code--Bit assignment table is shown as follows:

Bit Assignment		Symbol	Function	
CD Bus	CA&CB Bus			
CD15	CB15	HL	ATTRI-BUTE	Half Tone (1: Active, 0: Inactive)
CD14	CB14	BL		Blink (1: Active, 0: Inactive)
CD13	CB13	RV		Reverse (1:Active, 0: Inactive)
CD12	CB12		No use	
CD11	CA14	C11	Character Code for CGROM	
CD10	CA13	C10		
CD09	CA12	C09		
CD08	CA11	C08		
CD07	CA10	C07		
CD06	CA09	C06		
CD05	CA08	C05		
CD04	CA07	C04		
CD03	CA06	C03		
CD02	CA05	C02		
CD01	CA04	C01		
CD00	CA03	C00		

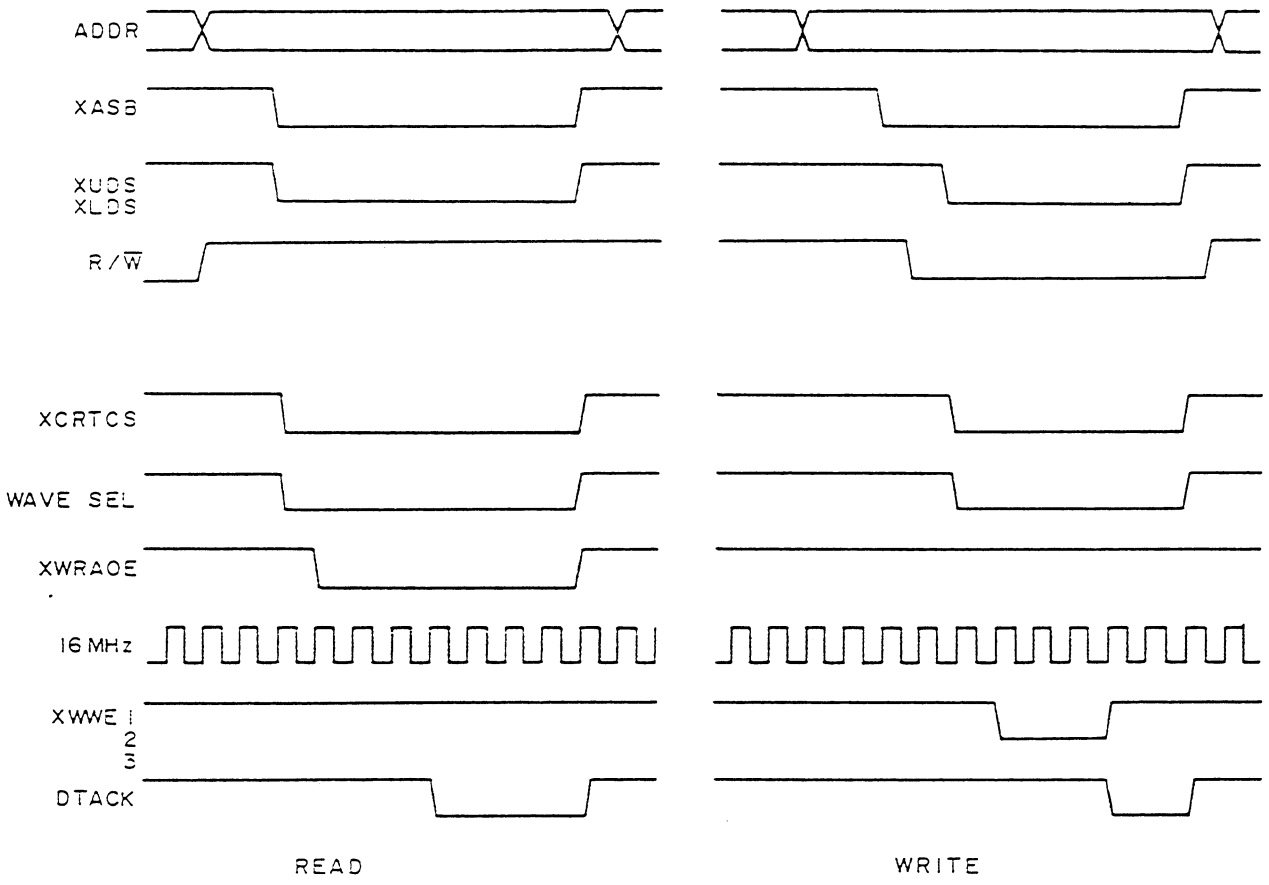
3.2.4 Wave Processing circuit



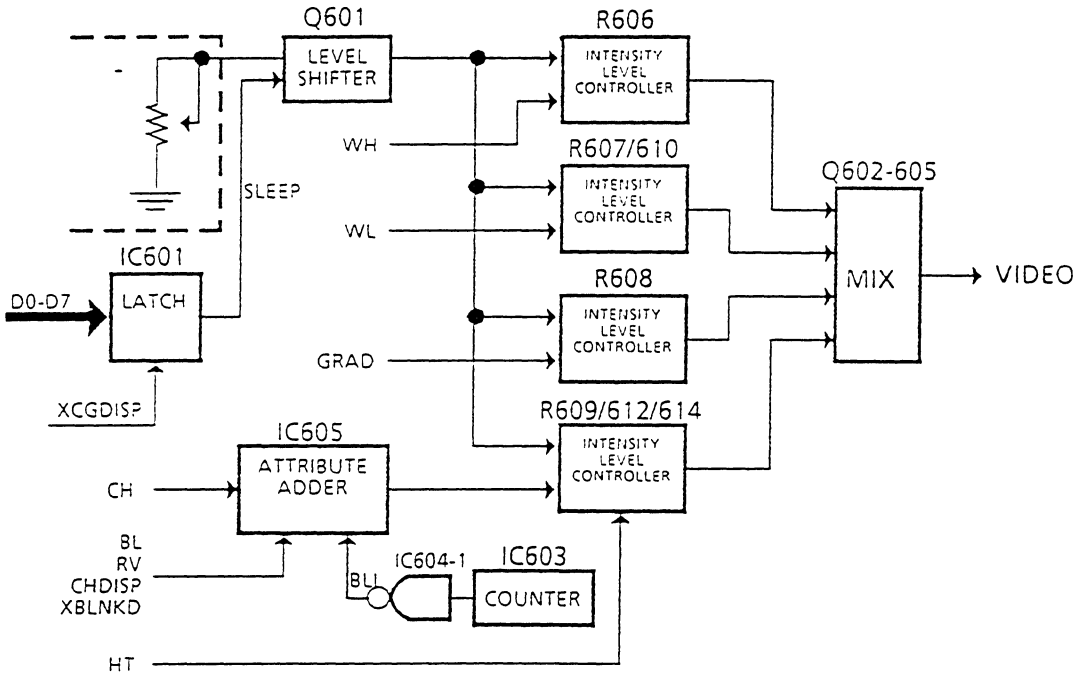
The circuit provides 2 custom ICs an Address Controller (IC401) and Waveform Composite (IC501), to display the waveform on the raster scan CRT.

The IC401 generates display timing and transfers a specified address to the Wave RAMs (IC402-0404). The Wave RAMs IC402, IC403, and IC404 acquire the wave data for Channel-1 & 2, Channel-3 & 4, and Channel-5 & 6 respectively. The wave data are transferred to the IC501 to convert to raster data. The IC501 generates the raster data for Standard intensity (WH1-4) and Low intensity (WL1-4) while receiving Wave ON/OFF data and Intensity Control data. The raster data, WH1-4 and WL1-4, are converted to Serial data, Standard intensity data signal (WH) and Low intensity data signal (WL), by the Shift Register (IC505/506) synchronized with the Load signal (WLD) respectively.

An Address specified by the MPU on the CPU board is transferred to the Wave RAMs through the IC401. A wave data is transferred thorugh the Buffer (IC407-409). When a wave data is read out to the IC501 synchronized with the Horizontal Synchronizing signal (XHS), access from the MPU 68000 to the Wave RAM is negated.



3.2.5 Video Signal Processing circuit



The circuit generates a Video signal from each serial display data. The Intensity Level Controller controls intensity of the signals GRAD, CH, WH, and WL.

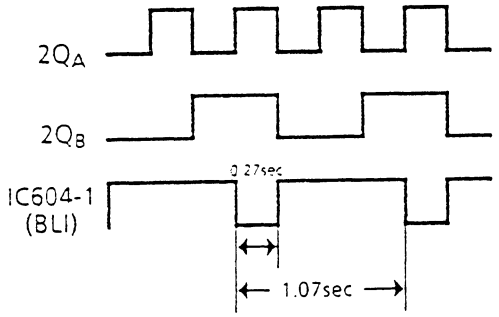
The Level Shifter (Q601) sets the Video signal amplitude with the Screen Brightness Control (from the front panel) signal and Sleep Control signal.

When the VM-003P CRT unit is used in the BSN-8500A/J/K bedside monitors and when the SLEEP ON/OFF key is set to "ON", the intensity level becomes inaccessible to the Screen Brightness Control on th the front panel.

The Mixer (Q602-605) generates a Video signal to the CRT unit (VM-003P) by mixing each intensity controlled display signal.

Concerning Character display data CH, this circuit provides the following circuit:

[Blink Interval circuit]



Blink interval (BL1) is fixed through the counter (IC603) by counting XVS signal.

[Character Attribute Adder circuit]

The following character attritude is set by combination of three attribute signals, RV, BL, and BL1.

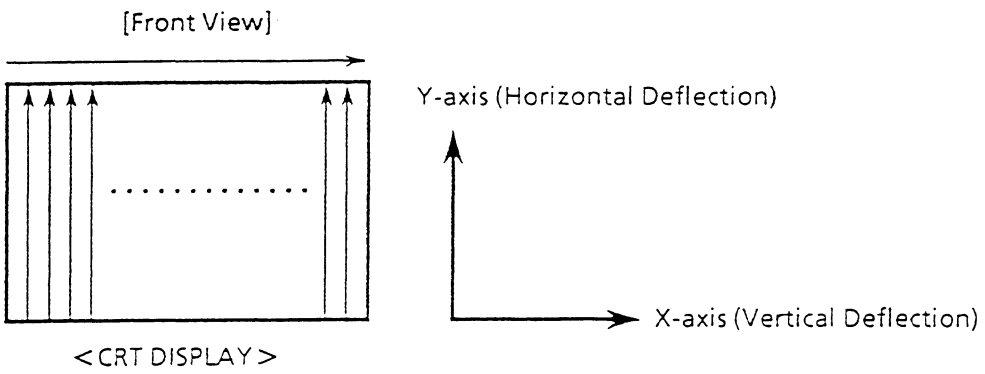
RV	BL	BLI	FUNCTION
0	0	0	Standard Indication
0	0	1	
1	0	0	Reverse Indication
1	0	1	
0	1	0	Standard Blinking Indication
0	1	.1	
1	1	0	Reverse Blinking Indication
1	1	1	

0: Low level
1: High level

The other attribute signal HT is applied to the Intensity Level Controller next to the Attribute Adder.

3.3 VM-003P CRT unit

3.3.1 General



The CRT unit provides Lengthwise (Y-axisward) Raster full scanning method as shown in the above figure. The CRT unit consists of the following circuits:

1) Video Signal Amplifier circuit
The circuit amplifies video signals generated on CRTC board (UP-0262) and energizes the cathod.

2) CRT Signal Processing circuit
The circuit generates signals for the Horizontal and Vertical Deflection circuits.

3) Vertical Deflection circuit
The circuit supplies the vertical deflection coil with sawtooth current synchronized by XVS signal to deflect an electron beam X-axisward.

4) Horizontal Deflection circuit
The circuit supplies the horizontal deflection coil with sawtooth current synchronized by XHS signal to deflect an electron beam Y-axisward.

5) CRT High Voltage circuit
The circuit supplies each electrode with the required voltage.

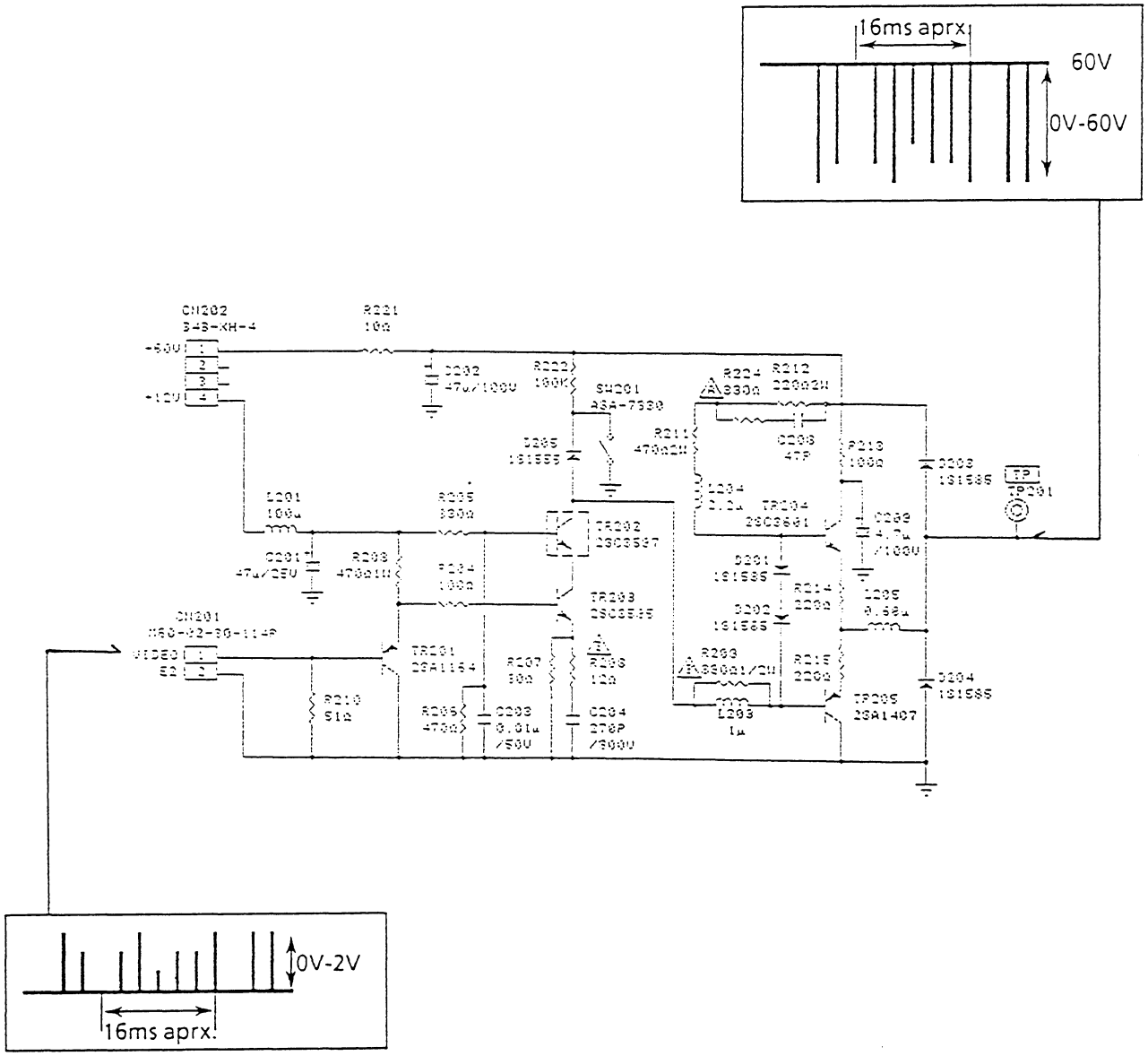
3.3.2 Video Signal Amplifier Circuit

The circuit matches the impedance between CRTC board (UP-0262) and this circuit through the transistor (TR201) with emitter follower.

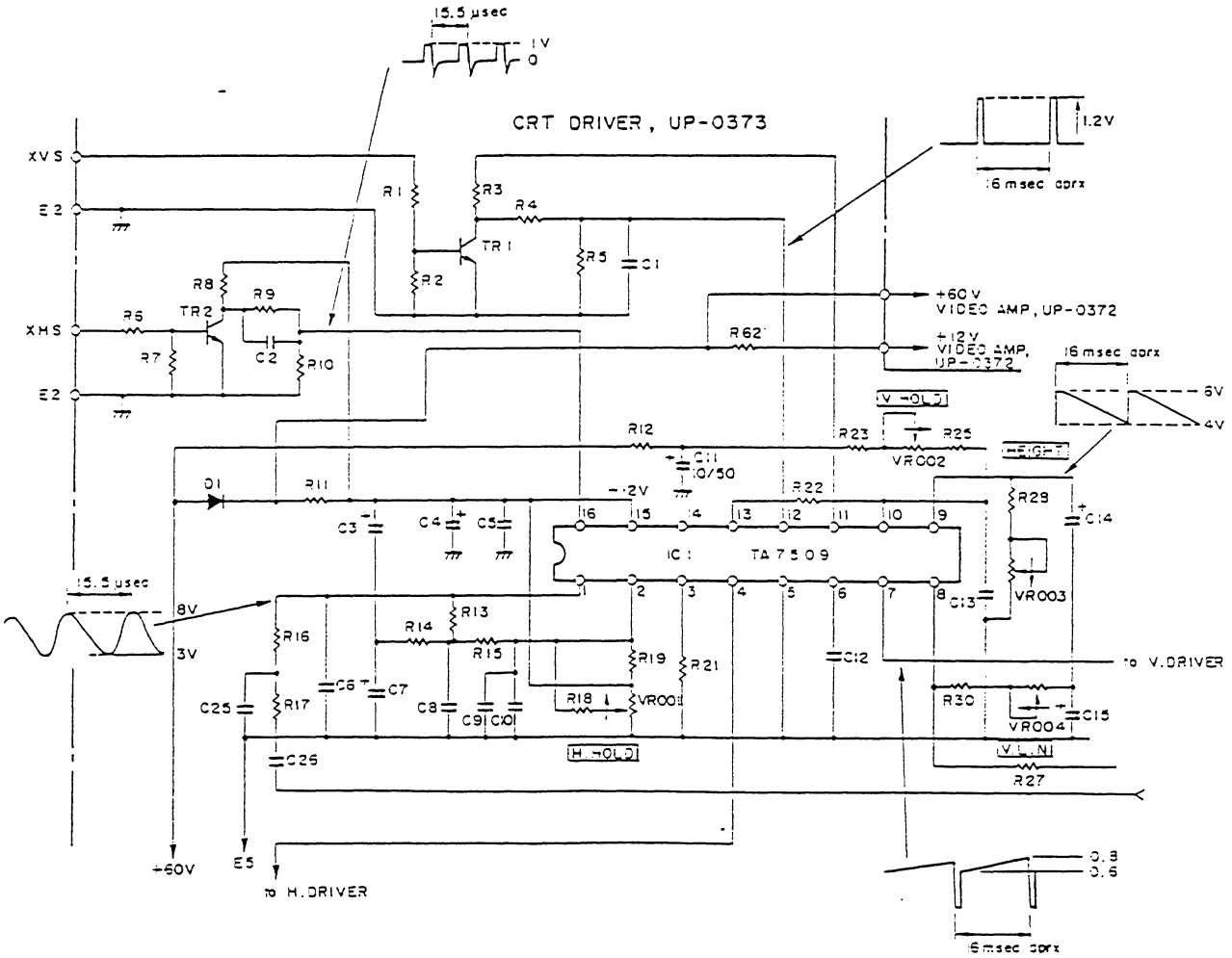
The circuit compensates frequency characteristics (Middle to High Frequency band on Video frequency band) through the cascade connected transistors (TR202/203), C204, L203, and L204.

The circuit amplifies the current to energize the cathode through the cascade connected transistors (TR204/205).

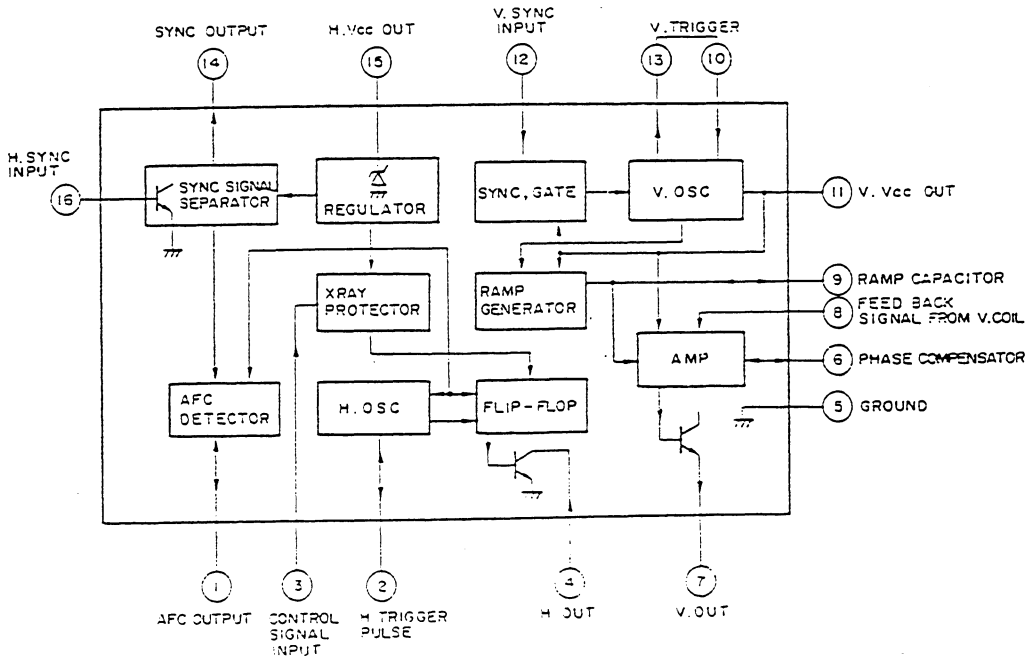
The circuit provides the switch (SW201) "Beam Finder Switch" to check the CRT unit. When the CRT unit is normal, the CRT is wholly lighted by depressing the switch.



3.3.3 CRT Signal Processing circuit



The circuit is controlled by the following IC001, TA7609P.



The IC001 provides vertical oscillator and horizontal oscillator functions.

1) Vertical Oscillating Circuit

The IC001 generates sawtooth waveform at pin-9 synchronized with XVS signal while receiving the XVS signal at pin-12. The IC001 generates the driving signal (sawtooth voltage) for Vertical Deflection Circuit at pin-7 while vertical deflection current is fed back to the pin-8 on the IC001.

VR002 (V.HOLD) holds the display vertically (X-axisward).
VR003 (V.LIN) compensates the display vertical linearity.
VR004 (HEIGHT) adjusts the vertical display size (X-axisward).

2) Horizontal Oscillating Circuit

The IC001 generates the stable driving signal for Horizontal Deflection Circuit synchronized with XHS signal since the IC001 internally provides Automatic Frequency Control (AFC). The IC001 outputs the signal at pin-1 after phase-detecting the XHS signal while receiving the XHS signal at pin-16.

At pin-2, the IC001 feeds back the phase-detected signal and integral signal with C025/026 and R016/017 feeding back from the pin-4 of the flyback transformer (T002).

The IC001 generates horizontal driving signal (Duty cylce:50%) from the above signals at pin-2 through the internal Flip/Flop.

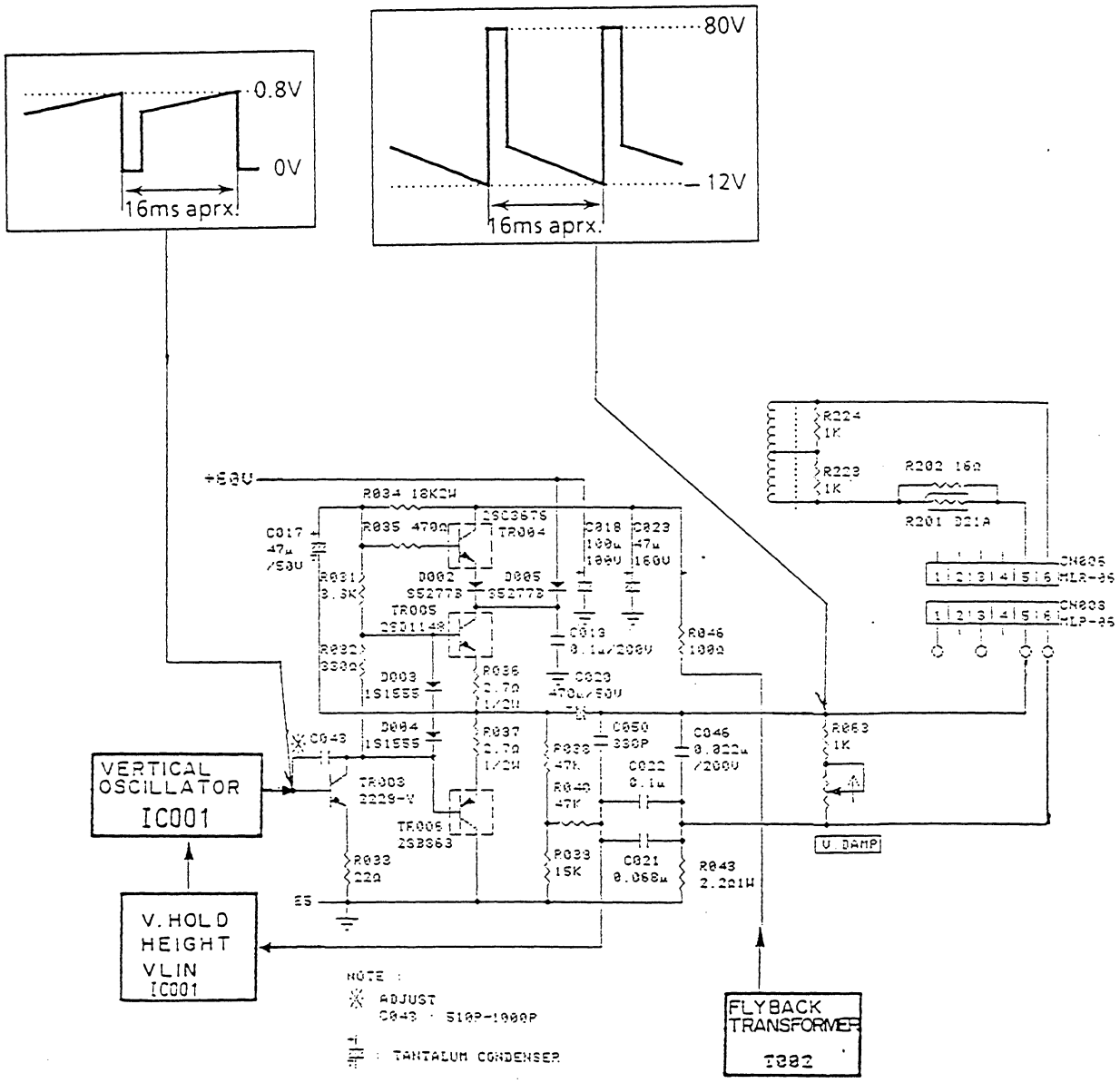
VR001 (H.HOLD) varies synchronous range and holds the display horizontally (Y-axisward).

3.3.4 Vertical Deflection Circuit

The circuit supplies the vertical deflection coil with a 60Hz sawtooth current and scans an electron beam vertically (X-axisward).

The circuit generates a vertical deflection current from the vertical sawtooth voltage at pin-7 on the IC001 through the transistors TR003, TR005, and TR006.

The R202 is the compensating resistor to hold vertical linearity. If the R202 is not mounted on the location, both edges of the vertical raster will be prolonged.

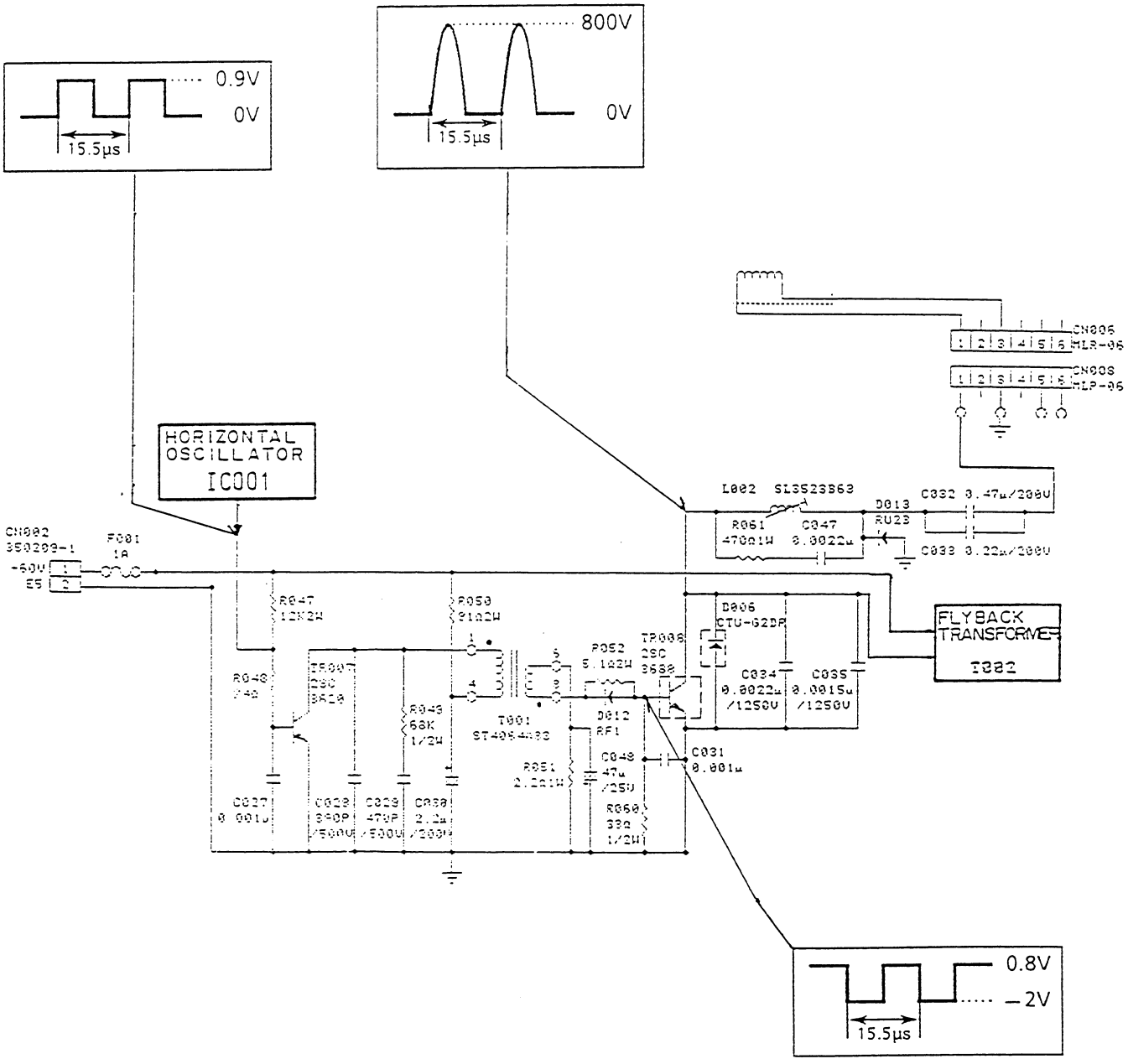


3.3.5 Horizontal Deflection Circuit

The circuit supplies the horizontal deflection coil with a 65.5kHz sawtooth current and scans an electron beam horizontally (Y-axisward).

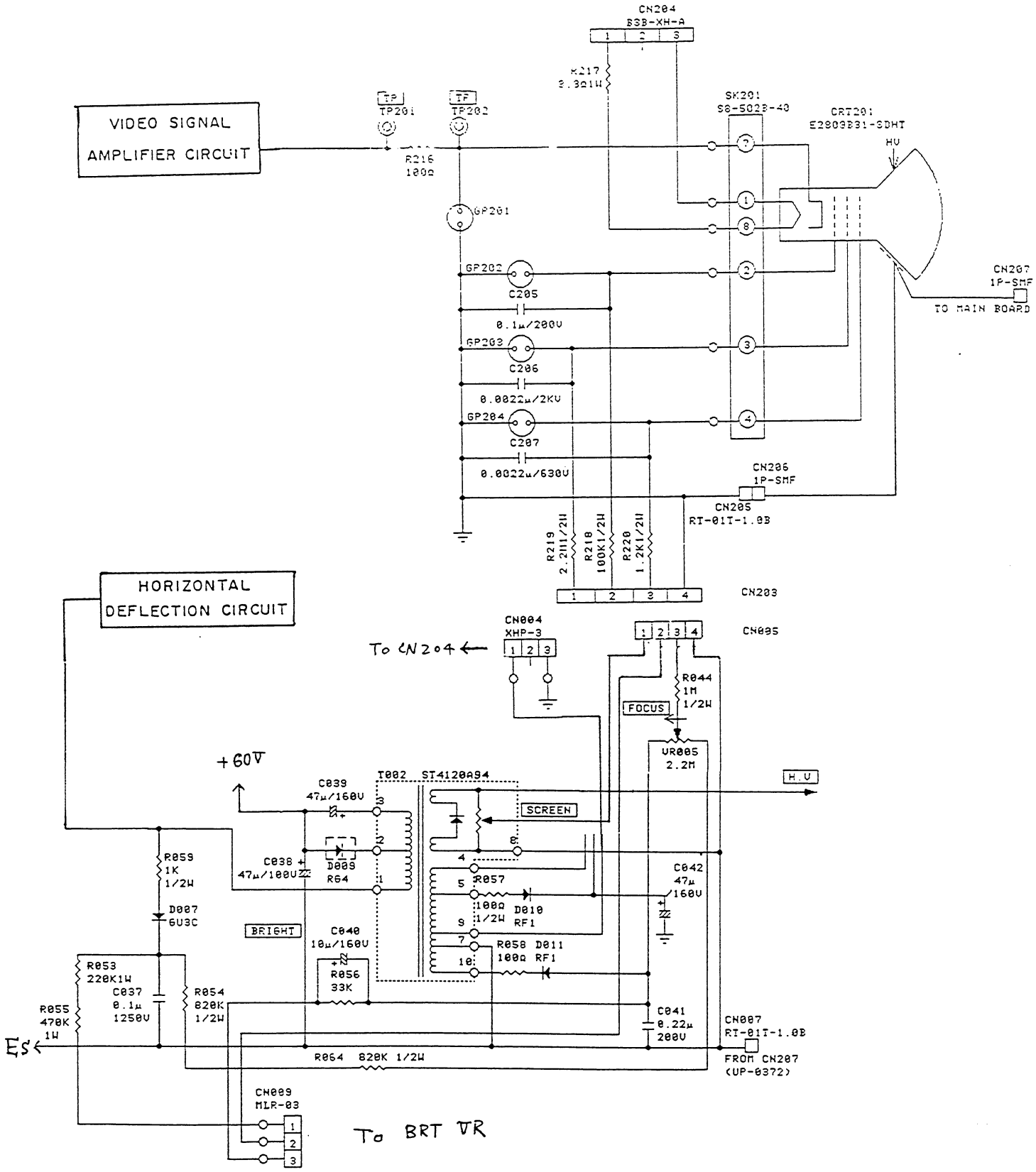
The circuit drives the transistor (TR007) and transformer (T001) with the horizontal driving signal so as to drive the horizontal output transistor (TR008). The circit generates the TR008 as a switching circuit.

The circuit generates the horizontal deflection sawtooth current through the damping diode (D006), the resonance capacitor (C034/035), and horizontal deflection coil including the WIDTH coil (L002). The L002 is a variable coil to adjust the horizontal display size (Y-axisward).



3.3.6 CRT High Voltage Circuit

The circuit supplies the anode with a 12.5kV high voltage and the other electrodes with the required voltage to operate the CRT.



The circuit consists of the Intensity Control Circuit, Focusing Control Circuit, and Spark Protective Circuit.

1) Intensity Control Circuit
The circuit controls the intensity, the number of electrons colliding against the fluorescent screen, with the bias voltage to the Grid number-1 (G1).

The Brightness Control Volume on the front panel adusts the intensity.

2) Focusing Control Circuit
The circuit control the focus by applying Direct Curent through the flyback transformer (Middle high voltage) and rectifier to the Grid number-2 (G2).

The VR005 (FOCUS) adjusts to the best focus condition.

3) Spark Protective Circuit
The circuit prevents damage to the CRT or other components from the sparks with 800V ga arrestors GP210/202/203/204.

3.4 UP-0464 AD board

3.4.1 General

Major functions of the AD board are as follows:

1) A/D conversion
Always A/D converts the data and automatically writes them into the Dual Port RAM. The MPU always reads the data from the Dual Port RAM.

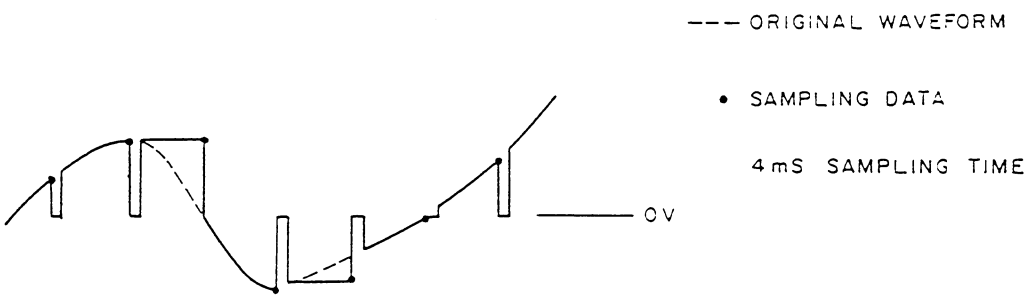
2) Number of A/D conversion bits
A/D conversion is made by 12 bits.

3) Sampling time
Sampling time of the A/D conversion is 4ms after peak hold processing of the analog waveform data.

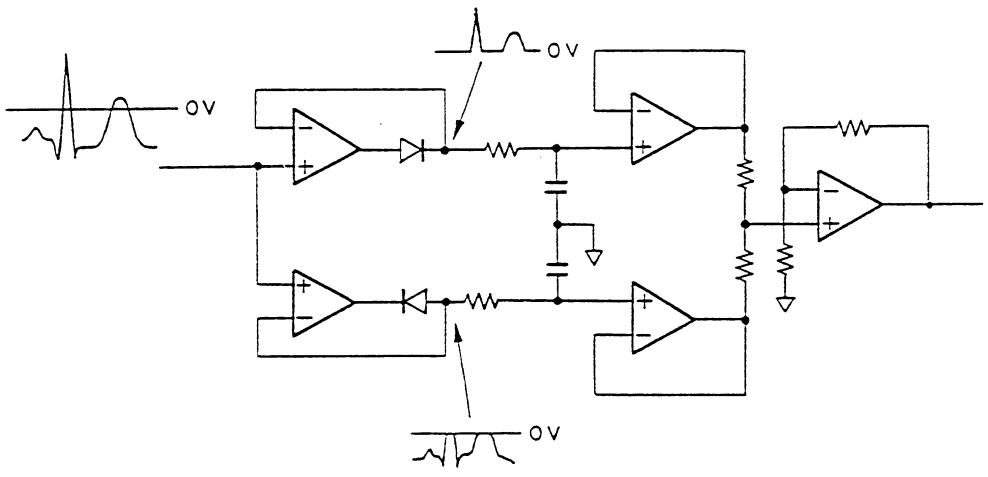
3.4.2 Peak Hold circuit

Peak hold circuit is for the following analog waveforms

- 16 Beds' real time ECG waveforms sent from the signal exchanger
- Selected one of 16 beds' MDW (depalyed ECG) waveforms sent from the REC CNTL board
- Selected one bed's waveforms



Sharp spikes like cardiac pacing pulse cannot be sampled by the 4msec sampling time of the A/D converter and waveforms cannot be reproduced correctly. Peak hold circuit hold the data until next sampling starts so that the peak of the pacing pulse can be displayed on the CRT and recorded with maximum amplitude.



3.4.3 Decoder circuit

A/D board is directly controlled by the MPU of the CPU board and address is decoded by this decoder circuit.

System bus is buffed by IC501 and IC502 and system data by the IC503 and IC504. Address is decoded by ICIC505 and IC506.

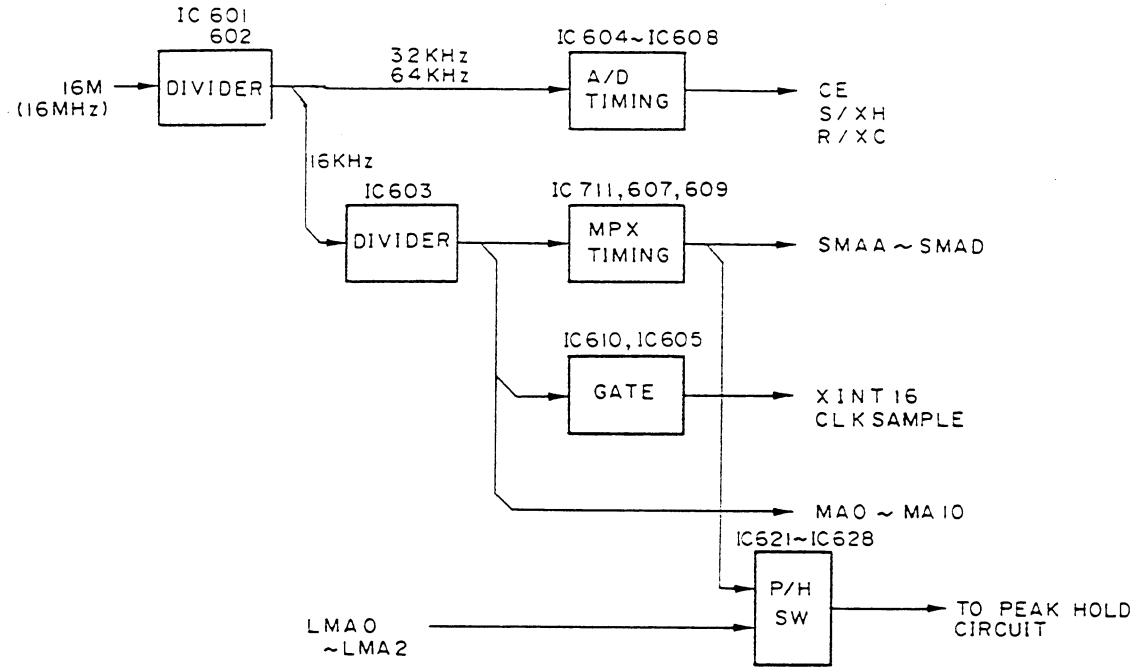
IC507, IC508 and IC510 generate Read/Write and DTACKB (response to the acess) signals.

Address is assigned as follows:

Chip select signal	Address	Device
XDPSEL	D00000-D00FFF	MB8241 (dual port RAM), 2kbyte
XCNRD	D01000-D01FFF	HC244
XIOWR	D03000-D03FFF	HC374

3.4.4 Timing control circuit

This circuit generates timing signals for sample hold, A/D conversion and multiplex.



Timing singals are generated from the 16MHz (signal 16M) clock signal of the CPU board.

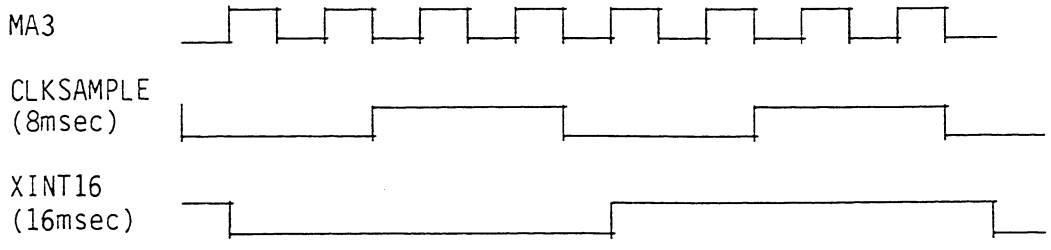
A/D timing signals CE, S/XH, and R/XC signals are generated by IC604- IC608 (refer to A/D conversion timing on page 3-38 for details).

Peak hold switching signals SMAA- SMAD and LMA0-LMA2 aer mixed in IC621-IC628.

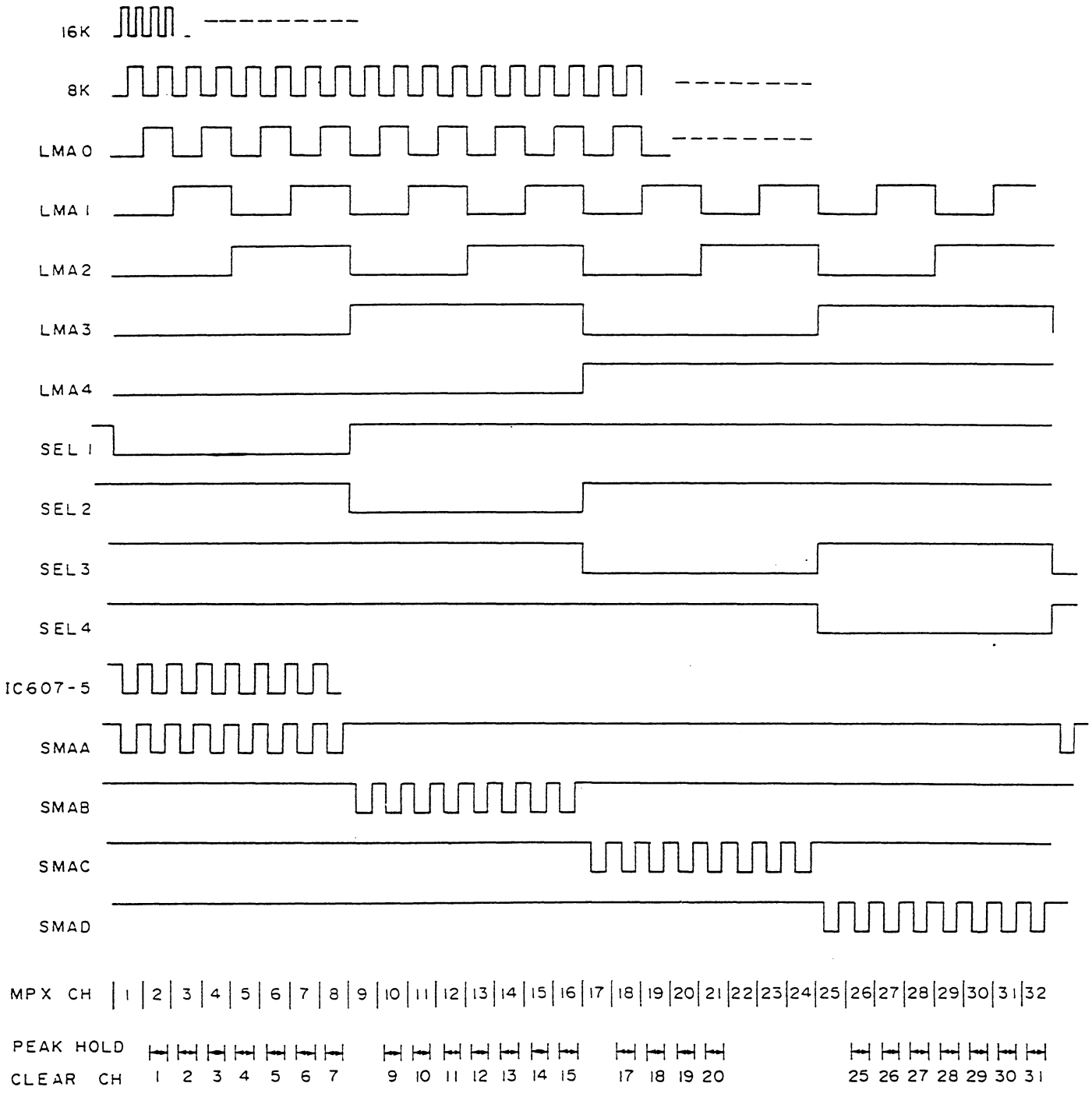
Interrupt signal XINT16 for CPU board and synchronizing signal CLKSAMPLE are generated by IC610 and IC605.

XINT16 ..... 62.5Hz(16ms) for A/D conversion timing

CLKSAMPLE ... 125Hz (8ms) for CPU board counter clock and waveform display synchronization between CPU board and CRTC board.



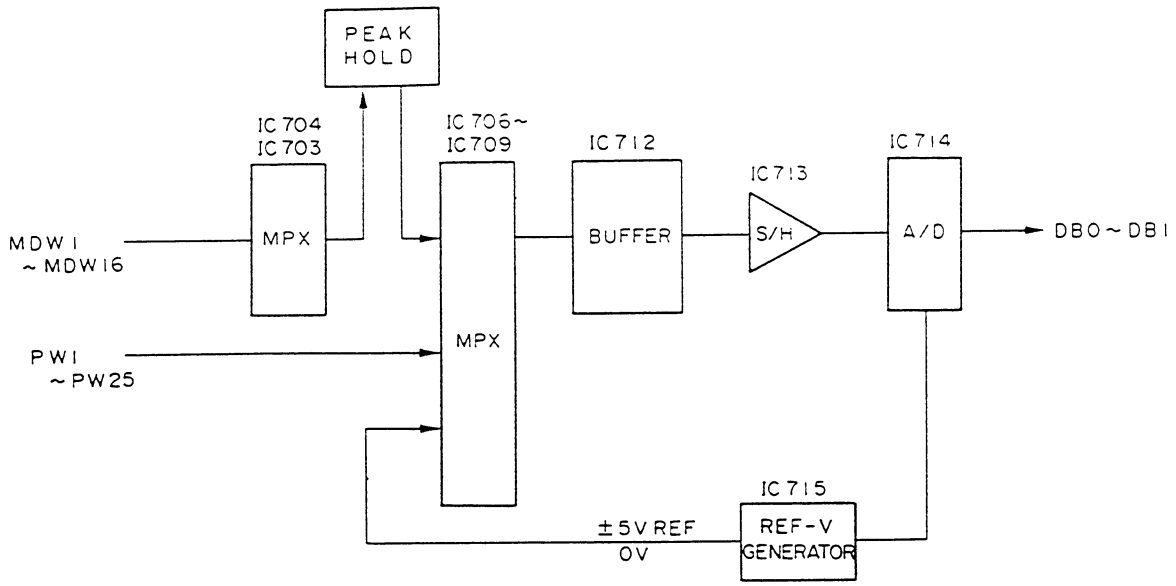
A/D input multiplex timing and peak hold clear timing



3.4.5 AD circuit

One of 16 beds' delayed ECG waveforms is selected by IC703 and IC704 and peak-hold processed to be PW25 signal.

16 beds' real time ECG waveforms are peak-hold processed to be PW1-PW16 signals.



Analog waveforms are multiplexed by IC706- IC709, buffed by IC712, sample-hold processed by IC103, and then A/D converted by IC714.

Referece voltages ±5VREF and 0VREF are generated by IC715 and IC714.

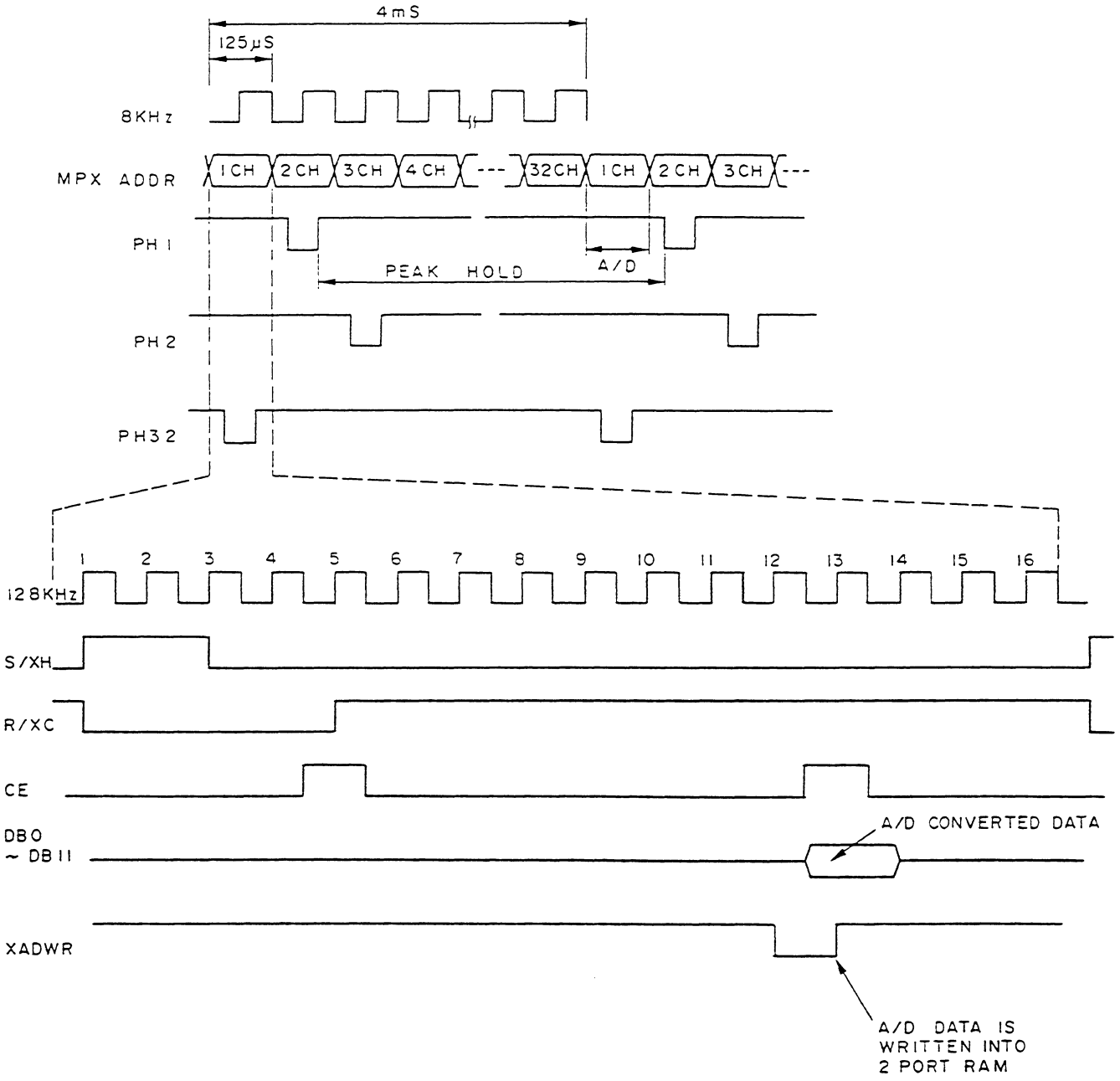
[AD memory]

A/D converted data is automatically written into the IC801 and IC802 dual port RAM.

32CH multiplexer

CH	Signal	Description
1	PW1	B1ECG1W (Bed1 real time ECG1 Waveform)
2	PW2	B2ECG1W
3	PW3	B3ECG1W
4	PW4	B4ECG1W
5	PW5	B5ECG1W
6	PW6	B6ECG1W
7	PW7	B7ECG1W
8	E1	E1 analog ground
9	PW8	B8ECG1W
10	PW9	B9ECG1W
11	PW10	B10ECG1W
12	PW11	B11ECG1W
13	PW12	B12ECG1W
14	PW13	B13ECG1W
15	PW14	B14ECG1W
16	E1	
17	PW15	B15ECG1W
18	PW16	B16ECG1W
19	PW17	Selected bed's ECG1W
20	PW18	Selected bed's ECG2W
21	W26	AUX1
22	W27	AUX2
23	W28	AUX3
24	+5VREF	+5V reference voltage
25	PW19 or W19	Selected bed's CH3W
26	PW20 or W20	Selected bed's CH4W
27	PW21 or W21	Selected bed's CH5W
28	PW22 or W22	Selected bed's CH6W
29	PW23 or W23	Selected bed's CH7W
30	PW24 or W24	Selected bed's CH8W
31	PW25 or W25	Selected bed's MDW (Delayed ECG Waveform)
32	-5VREF	-5V reference voltage

A/D conversioon timing



4.4.6 Power regulator

Supplies the A/D converter with ±15V power voltages.

3.5 UP-0511 REC CNTL board

3.5.1 General

Major functions of the RECL CNTL board are as follows:

1) Control of the built-in thermal array recorder
Sub CPU (8085) is employed in the REC CNTL board to control the built-in recorder and communcation with the Master CPU (68000) on the CPU board is made through the dual port RAM.

2) Control of the keyboard
Optional keyboard is controlled by the communication LSI uPD720G1.

3) Communication
Communication between the JJ signal exchanger and MU central monitor main unit is made by the uPD72001.

4) Hard copy interface
The REC CNTL board provides hard copy interface to generate video signal for hard copy operation by the WS-800RK thermal array recorder.

5) Data transfer
Directly connects the 8 beds' real time ECG waveforms from the JJ signal exchanger to the local bus of the MU main unit.

3.5.2 composition of the REC CNTL board

1) Decoder circcuit
The REC CNTL board is directly controlled by the MPU of the CPU board and address is decoded by this decoder circuit.

2) Communication control circuit
uPD72001 controls communication between the JJ signal exchanger and MU main unit.

3) Keyboard control ciircuit
uPD72001 control an optional keyboard.

4) Built-in recorder control circuit
Generates character print data, waveform data, scale data, and recorder control signals to the built-in recorder.

5) Hard copy interface
Generates video signals for hard copy operation of the WS-800RK thermal array recorder.

3.5.3 Decoder circuit

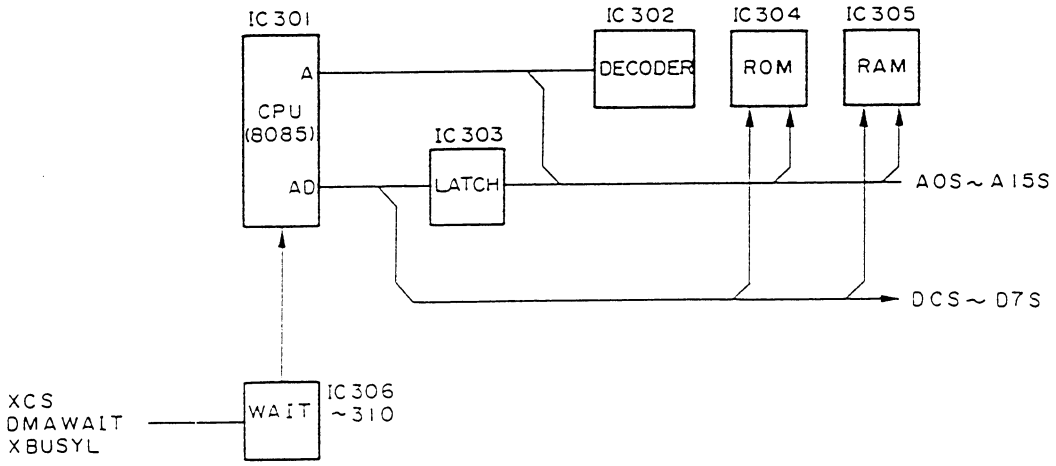
System address is buffed by IC101, IC102 and system data is buffed by IC103. Address is decoded by IC104, IC105 and IC109.

IC106, IC107, IC108 and IC110 generate Read, Write, DTACKB (response to the sccess) signals.

Address is assigned as follows:

Chip selecxt signal	Address	Device
XDPSEL	0E00000-0E0FFF0	MB8241 (dual port RAM), 2kbyte
XCOMRD XCOMWR	0E01000-0E01003	uPD72001
XIOWR	0E030000	HC243

3.5.4 Sub CPU (8085)



Sub CPU (8085) on the REC CNTL board is to control the built-in recorder. Communciaton between the Master CPU (68000) is made through the global memory (dual port RAM). Address is decoded by IC302.

Address is assigned as fllows:

Memory map

Chip select signal	Address	Device
XA15S	0000-7FFF	27C256, 32kbyte
XRAM1, XRAM2	8000-9FFF	62256, 16kbyte
XDPRAM	C000-C7FF	MB8241, 2kbyte
XIRAM	E000-FFFF	6264, 8kbyte

IO map

Chip select signal	Address	Device
XSEL1	80 81	HCT244/HC273 HC374
XSEL2	A0-A7	M58990P(AD)
XTIN1	C0-C3	uPD71054
XTIN2	E0-E3	uPD71054

WAIT signal is generated by IC306- IC310 and inputted to the CPU (8085) READY terminal. CPU (8085) is in WAIT condition during the following conditions:

. DMA cycle of the print RAM

. Dual port RAM access by the Master CPU

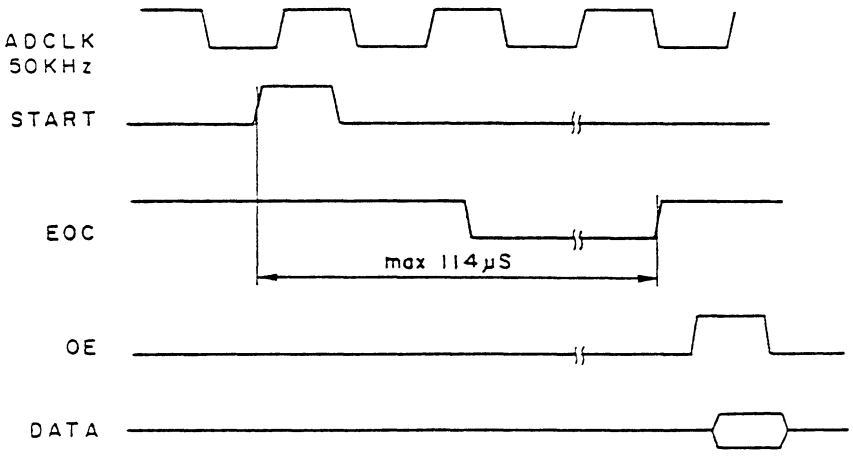
. IO access (250us WAIT; 1 clock)

[Timing circuit]

OUTO singal of the program counter is the trriger of the entire timing system. Refer to the descriptions of DMA pring timing for details.

3.5.5 A/D conversion and dual port RAM

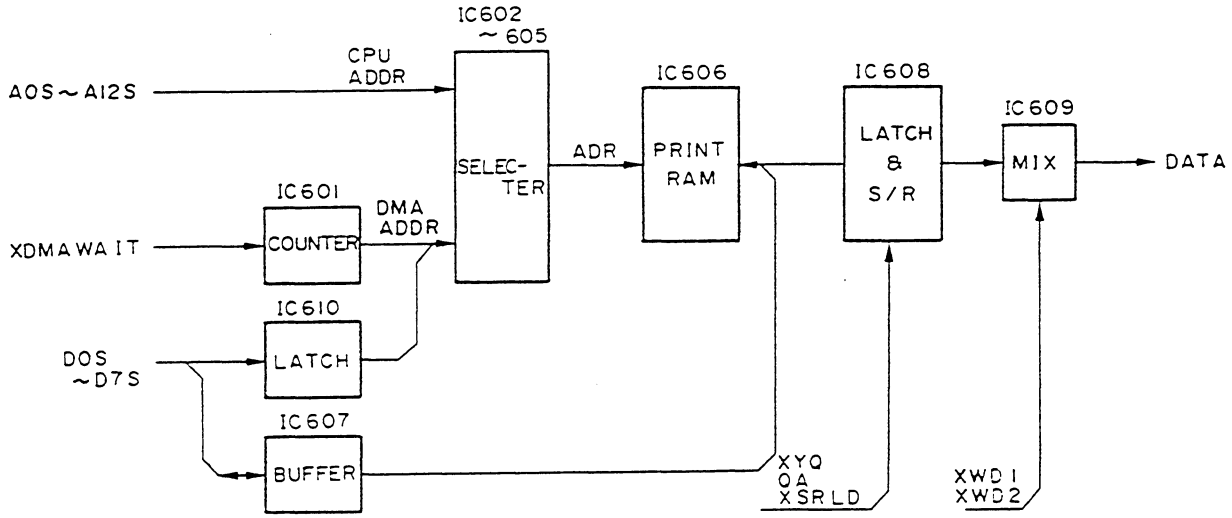
1) A/D conversion
VTH (thermal head temperature signal of the built-in recorder) is A/D converted and transferred to the CPU (8085).



A/D TIMING

2) Dual port RAM
Communciation beteen the Sub CPU (8085) and Master CPU (68000) is made through the dual port RAM (IC707). The RAM provides Left and Right two ports and arrangement of access of each port is done by BUSY and INT signals generated inside the device.

3.5.6 Print RAM

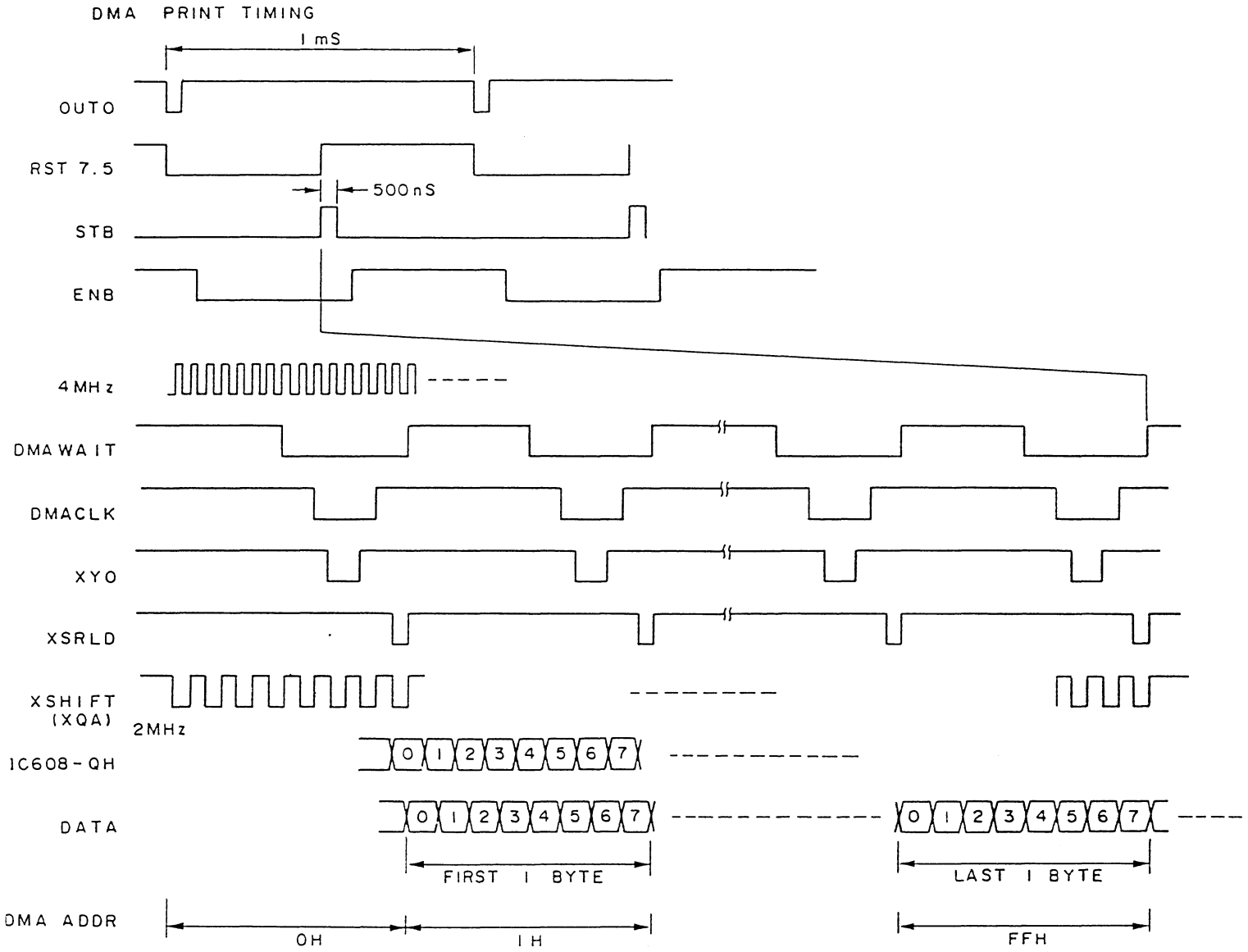


Print data from the character print RAM is directly transferred to the shift register IC608 by DMA (Direct Memory Accrees) operation without intermedication of the CPU (8085).

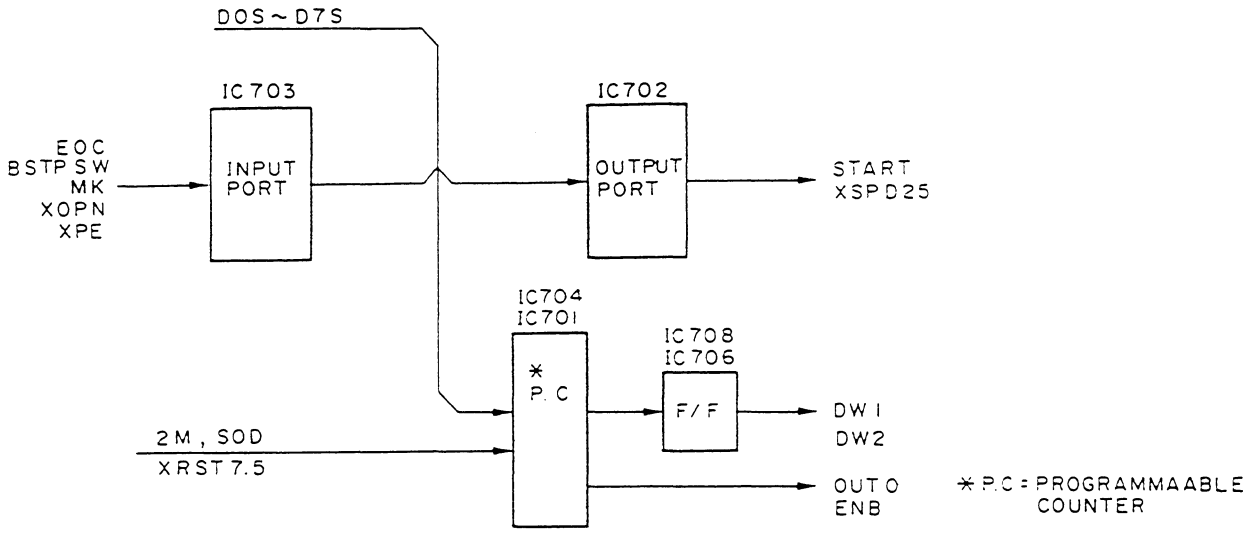
Address during DMA operation is generated by the counter IC601 and latch IC610. Address from the CPU (8085) and address during DMA operation are switched by the selecter IC602-IC605. Data from the CPU (8085) and address during DMA operation are switched by IC607.

Print data includes character and scale data taht are mixed with the waveform data by the IC609.

Print data DMA timing



3.5.7 I/O circuit



Recorder status signal of the built-in recorder (MK: Mark detection, XOPEN: Magazine Open, XPE: Paper Empty, BSTPSW: Switch On/Off) are read by the CPU (8085) through IC703.

Recorder control signals (START: recorder Start On/Off, XSPD25: recorder Speed 25/50 mm) from the CPU (8085) are written into IC702.

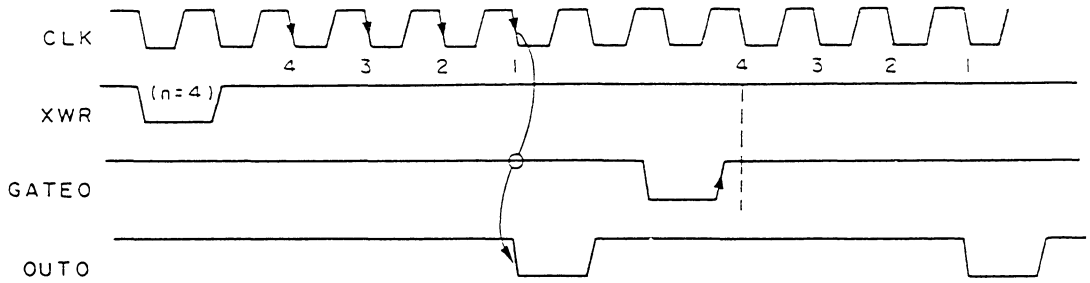
uPD71054 (IC701, IC704) is a programmable counter which generates OUT0 (original timing signal for the recorder) and thermal head enable signal. Waveform data DW1 and DW2 are generated by IC706 and IC708.

[Hard copy interface]

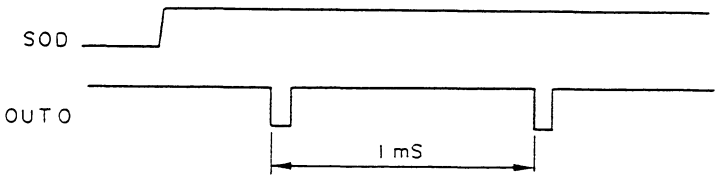
IC801 is a comparator which shapes the waveforms of the video signal for hard copy operation by the WS-800RK thermal array recorder.

3.5.8 Programmable counter

1) Generation of OUT0 signal
Counter-0 is used in Mode-2 (rate generator mode) for OUT0 signal generation. According to the mode setting, the counter output is "H" level. When the gate input is "H", counter restarts to count the clock signal. This counter is a dividing counter that outputs "L" level pulse every time at the end of specified count number. Actually, counter input is a 2.00MHz clock signal and the output is 1kHz, i.e, 1/2000 dividing.

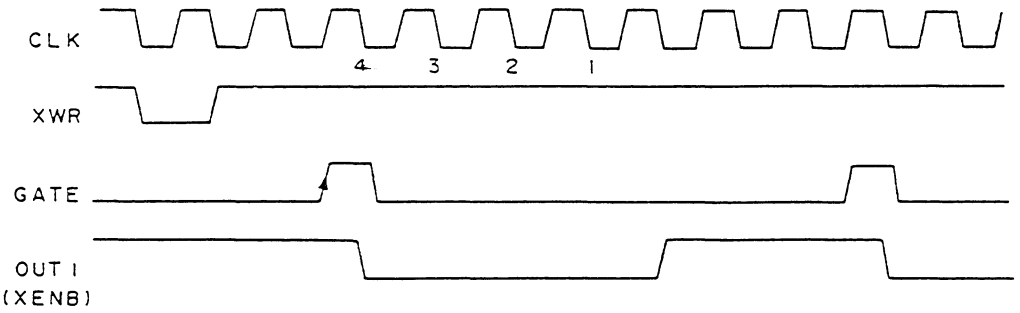


When SOD terminal of the CPU (8085) is "H" level, OUT0 is asserted and OUT0 functions as the original timing of the recorder operation.



3.5.9 Generation of the XENB (enable) signal

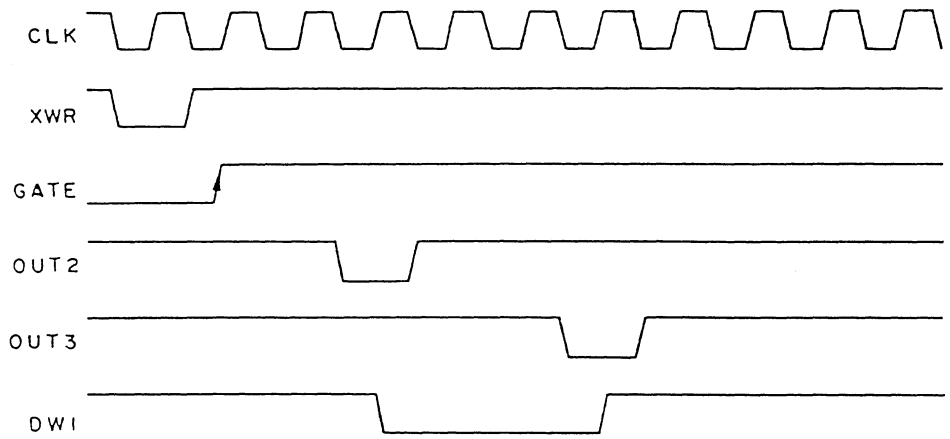
Counter-1 is used in Mode-1 (retriggerable One-shot). Specified width one-shot pulse is outputted from the OUT terminal of the counter in this mode. Retriggering is available by the GATE signal input.



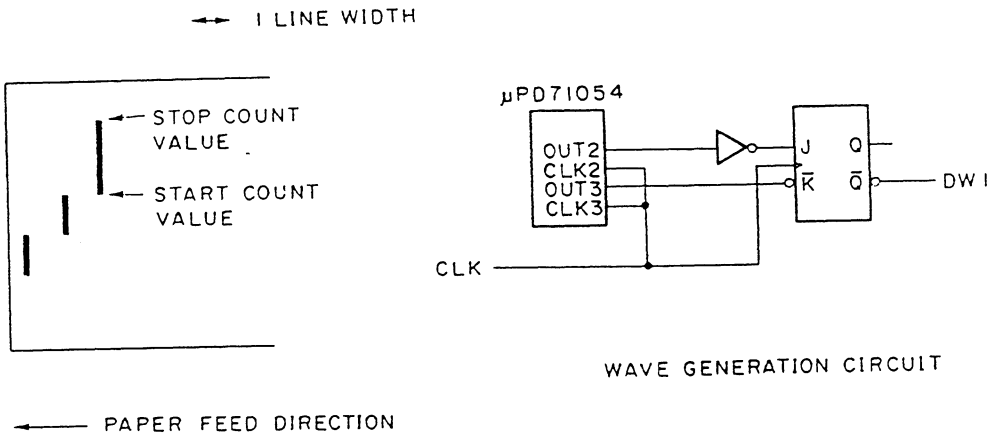
The input is 2.00MHz clock signal for the XENB (OUT1). Pulse width changes according to thermal head temperature.

3.5.10 Generation of WAVE signal

Counter-2 through counter-5 are used in Mode-5 (hardware triggerd strobe mode).



Counter-2 for OUT2 is set to START count number of 1 line for waveform tracing and counter-3 for OUT3 is set to STOP count number of the trace. With these two OUT1 and OUT2 signals, DW1 waveform data is generated by the inverter and J-K Flip-Flop.



WAVE GENERATION CIRCUIT

3.6 UP-0512 REC DRV board

3.6.1 General

Major functions of the REC DRV board are as follows:

1) Direct transfer of the signals from the optional keyboard to the REC CNTL board.

2) Generation of thermal head drive voltage (built-in recorder).
+21V from the mother board is regulated by the switching regulator into the thermal head drive voltage.

3) Motor drive for paper feeding.

4) Transfer of the recorder status signals to the REC CNTL board.

3.6.2 Overall circuit block descriptions

1) Thermal head drive voltage generatior
+21V from the mother board is regulated by the switching regulator into the thermal head drive voltage. The regulator provides over-current protection.

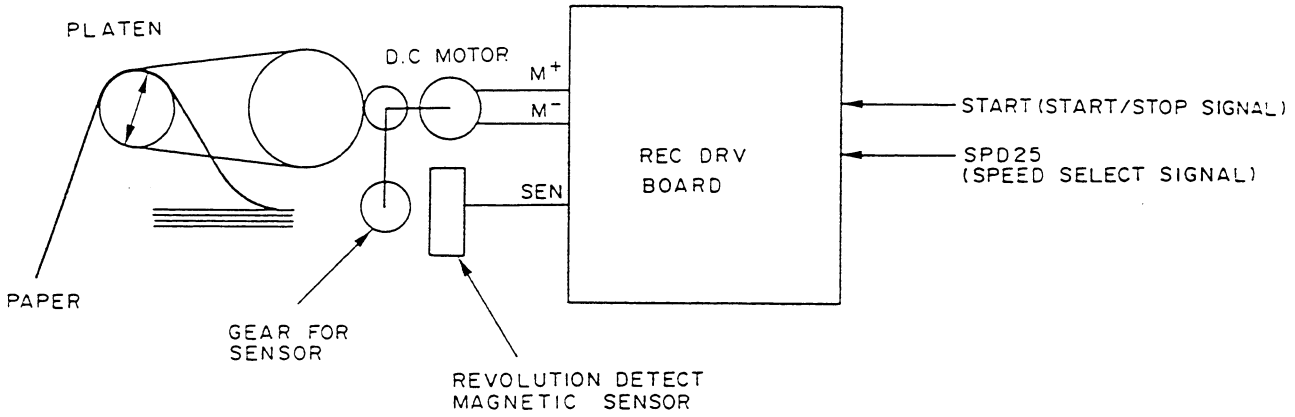
2) Motor drive
Motor revolution for paper feeding is controlled by signal SEN (motor revolution detection Sensor signal), XSTART (Start signal from the REC CNTL board), and SPD25 (Speed select signal).

3) Generation of recorder status signals
Status signals include:
. Mark on paper detection signal
. Magazine open detection signal
. Paper empty detection signal
. Thermal head temperature signal

4) Direct trasnfer of the signals from the optional key board to the REC CNTL board.

5) Recorder operation I/F circuit
Transfers switch operation of the built-in thermal array recorder to the REC CNTL board. Directly drives the LED lamp on the built-in thermal array reocrder by the recorder status signals.

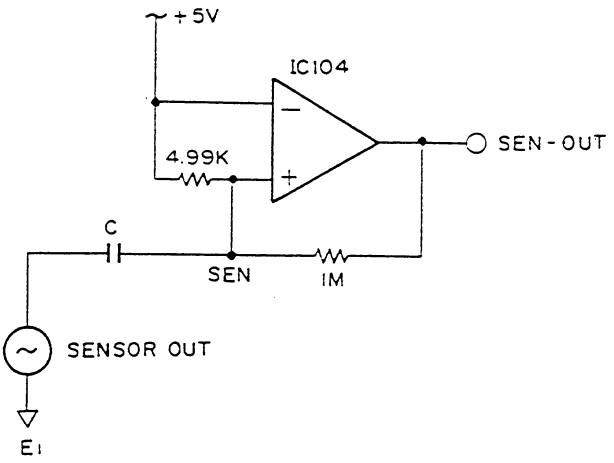
<REC DRV block>

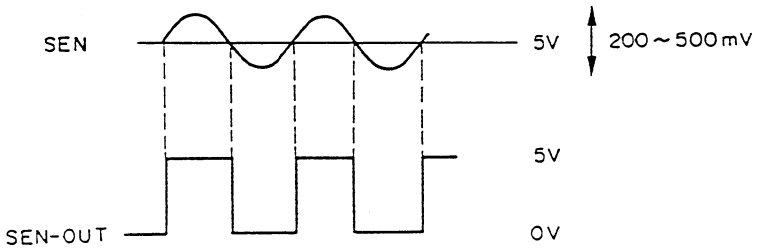


DC motor is controlled by detecting magnetic field strength variation near the gear teech. The revolution sensor signal is fed back to obtain specified stable paper speed.

REC DRV block consists of a comparator for shaping waveform of the sensor output signal, speed selection signal, and motor driver. Motor driver is provided with motor auto stop circuit, over-current protector, magazine open detector, paper empty detector, cueing mark detector, and thermal head temperature sensor.

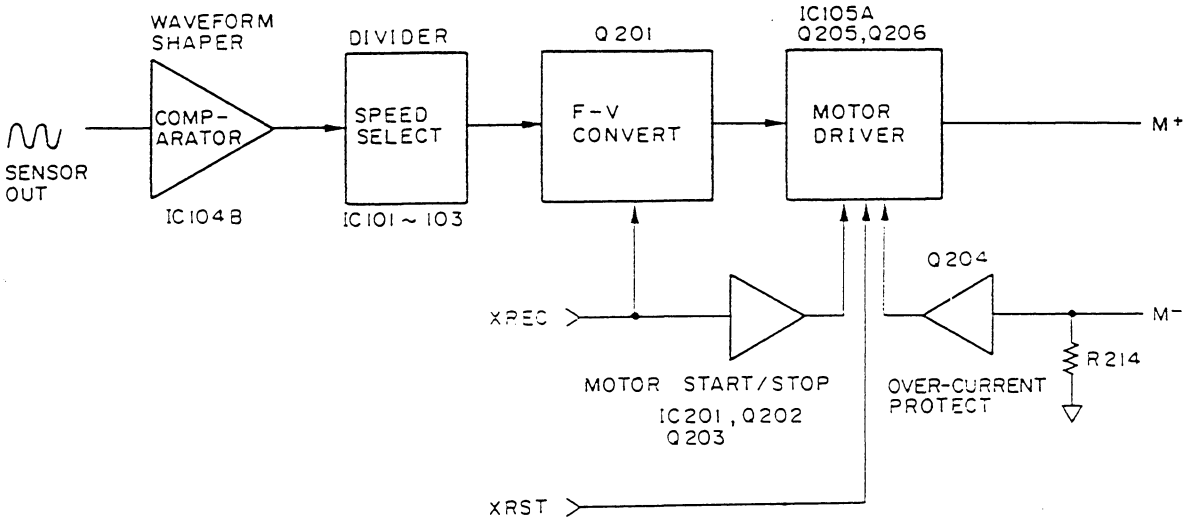
<Waveform shaper>



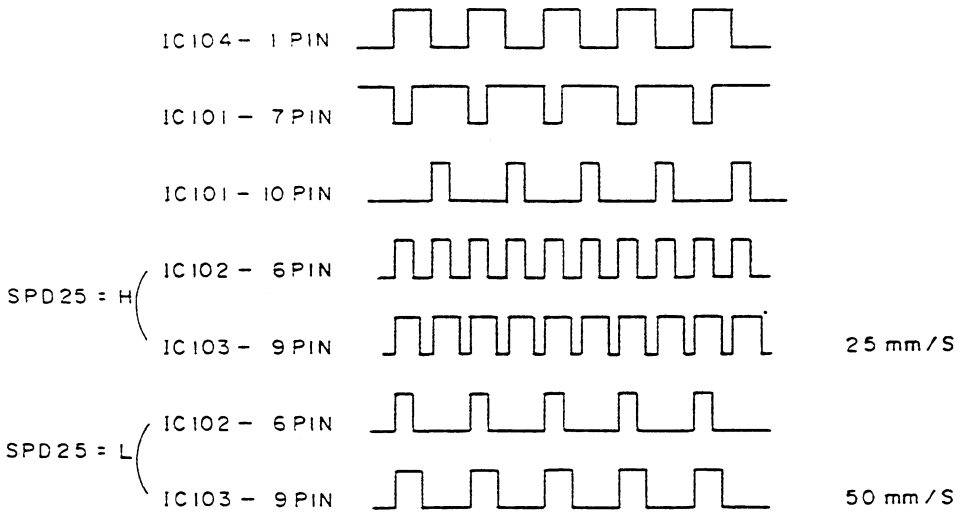


Waveform shaper is composed of a comparator. Revolution sensor output is DC cut by a capacitor and inputted to the IC104B plus terminal which is superimposed with +5V.

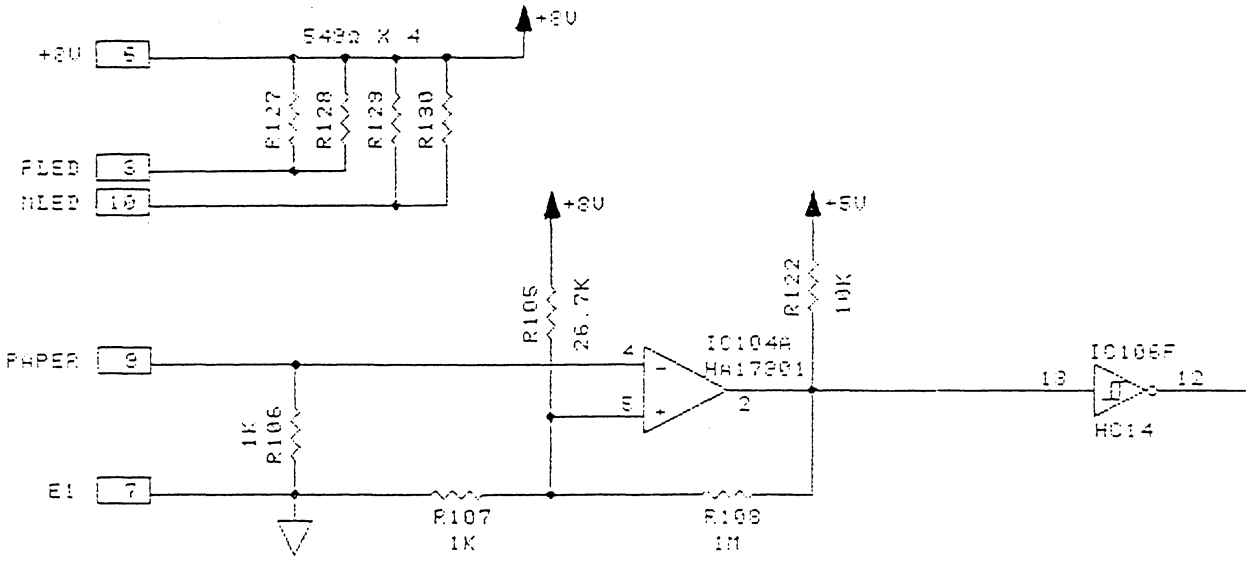
3.6.3 Paper speed selection



DC motor controller controls motor revolution so that the F-V (Frequency-Voltage) converter output voltage becomes equal to the reference voltage. By inserting "1/n" frequency divider between the waveform shaper and the F-V converter so that the frequency is deducted, the F-V converter output voltage drops. The paper speed controller rised the motor drive voltage to the reference voltage when the division ratio is "1/n", the motor revolutes "n" times faster. Paper speed control is done by the IC101 one-shot multivibrator. Paper speed control signal SPD25 changes the frequency of output by the IC102.



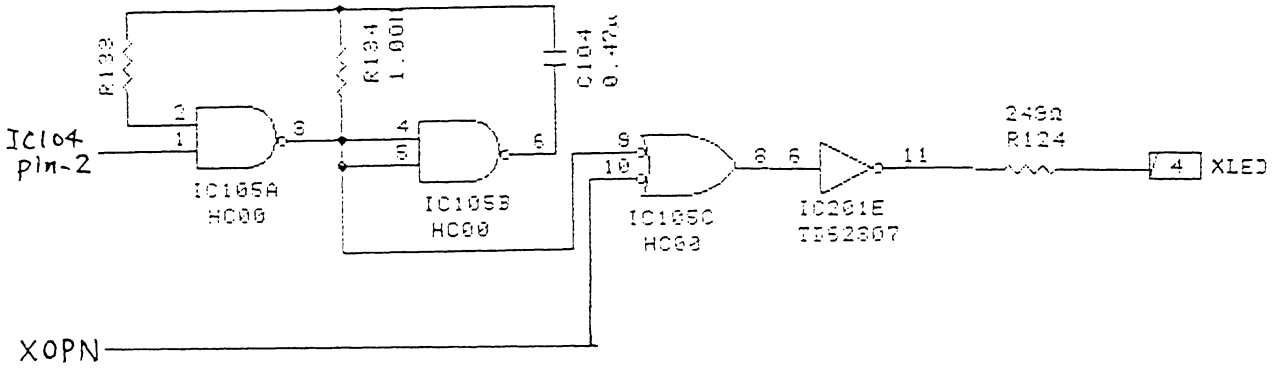
3.6.4 Paper detection



	PAPER output	XPAEMP output level
No paper	0.15V	L
Paper exists	0.8V	H

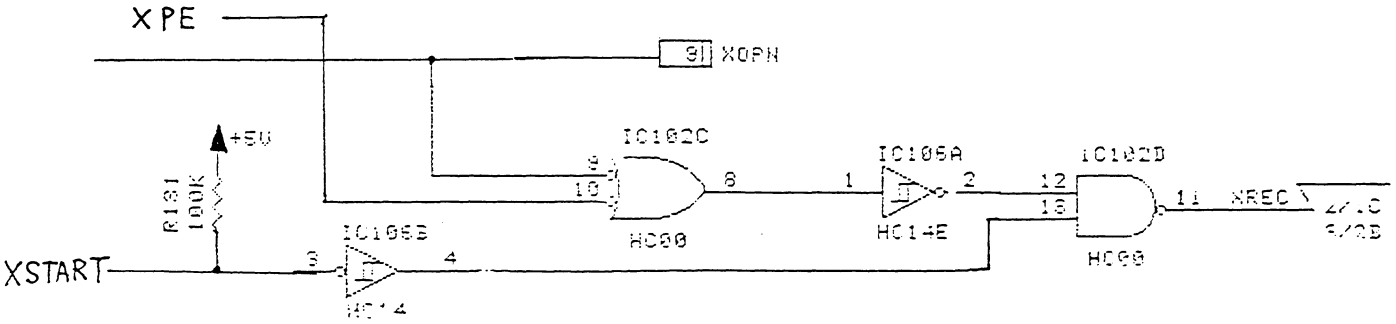
Comparator reference voltage is approximately 0.6V.

3.6.5 Paper empty indication LED lamp

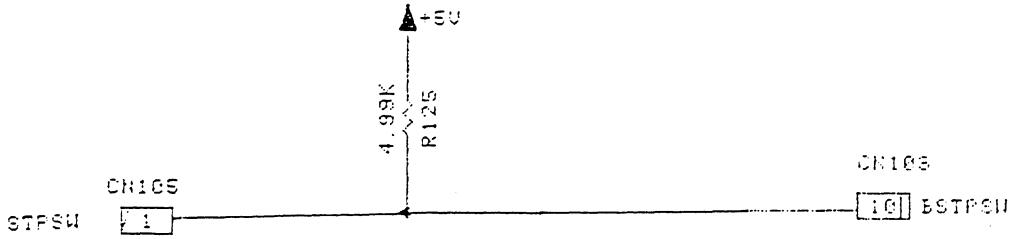


XPE (Paper Empty)	XOPEN (magazine open)	LED lamp
L	L	Lights up
L	H	Goes out
H	L	Lights up
H	H	Blinks

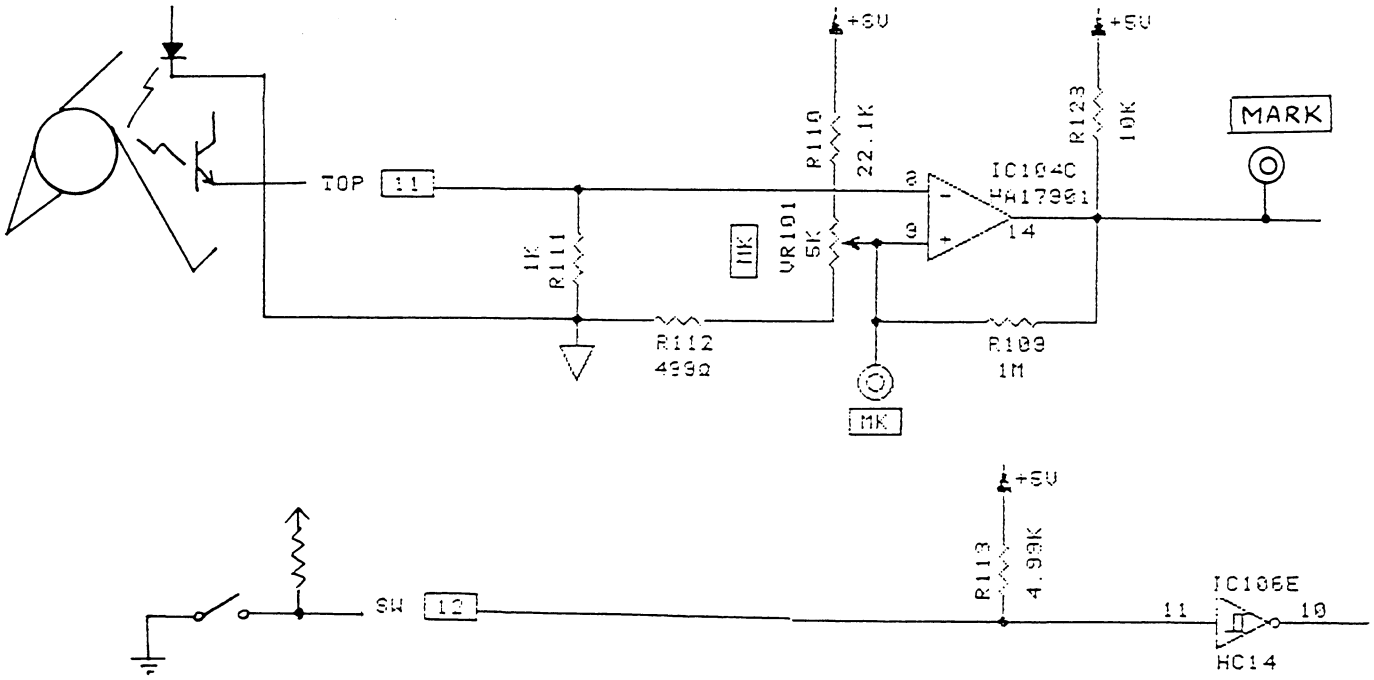
The paper empty LED lamp blinks when paper is empty and lights up when magazine is open.



When paper is empty (XPE: L) or magazine is open (XOPEN: L), XREC signal turns to H to stop the motor.



3.6.6 Mark detection and magazine open detection

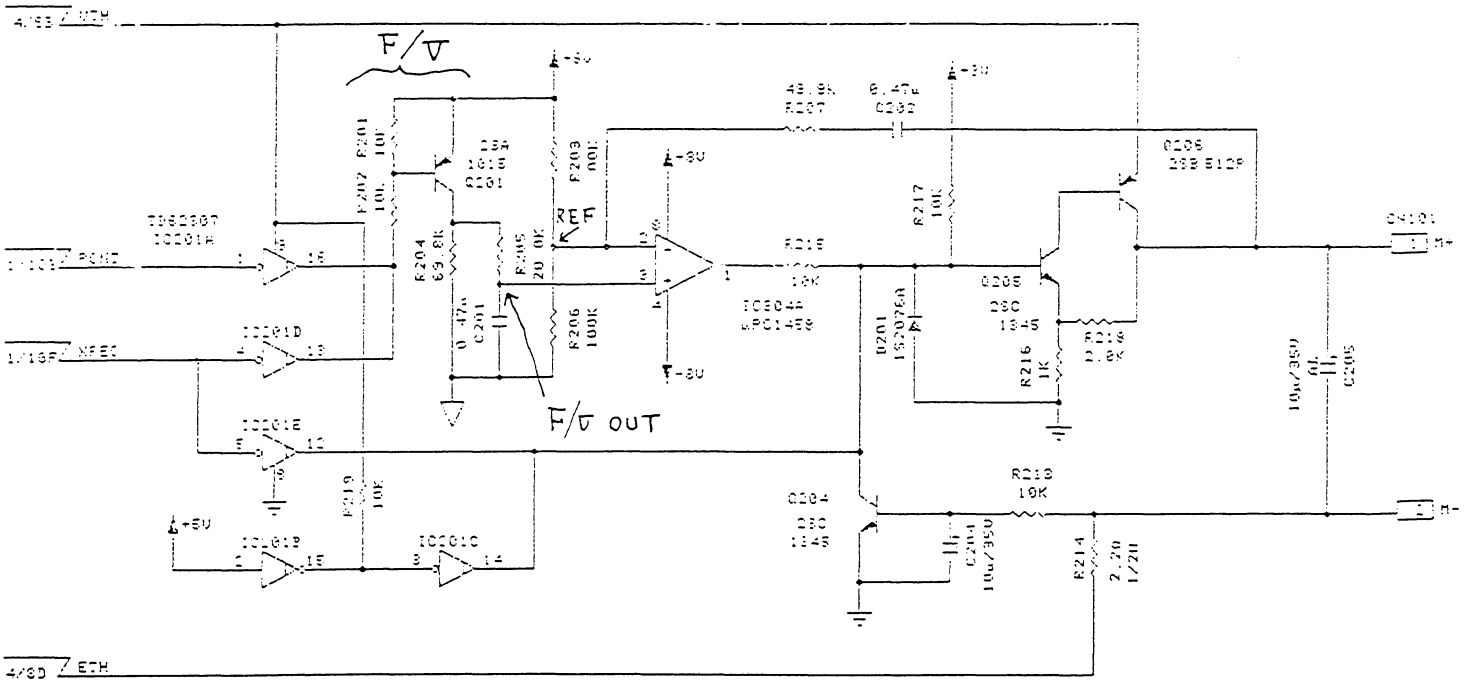


Comparator reference voltage is adjustable by the VR101 (MK). Adjust it to 0.5V. Mark is detected only when the MARK signal is H and XPAEMY signal is L.

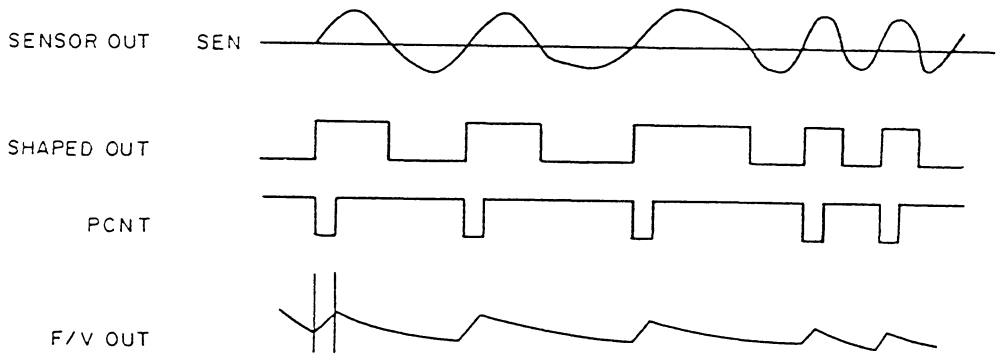
When the magazine is released and the switch turns to off, XOPEN signal becomes L through the inverter (IC106E).

	TOP output (MARK)	MARK output level
No paper	0.15V	H
Paper mark	0.4V	H
Plain paper	0.8V	L

3.6.7 Motor driver

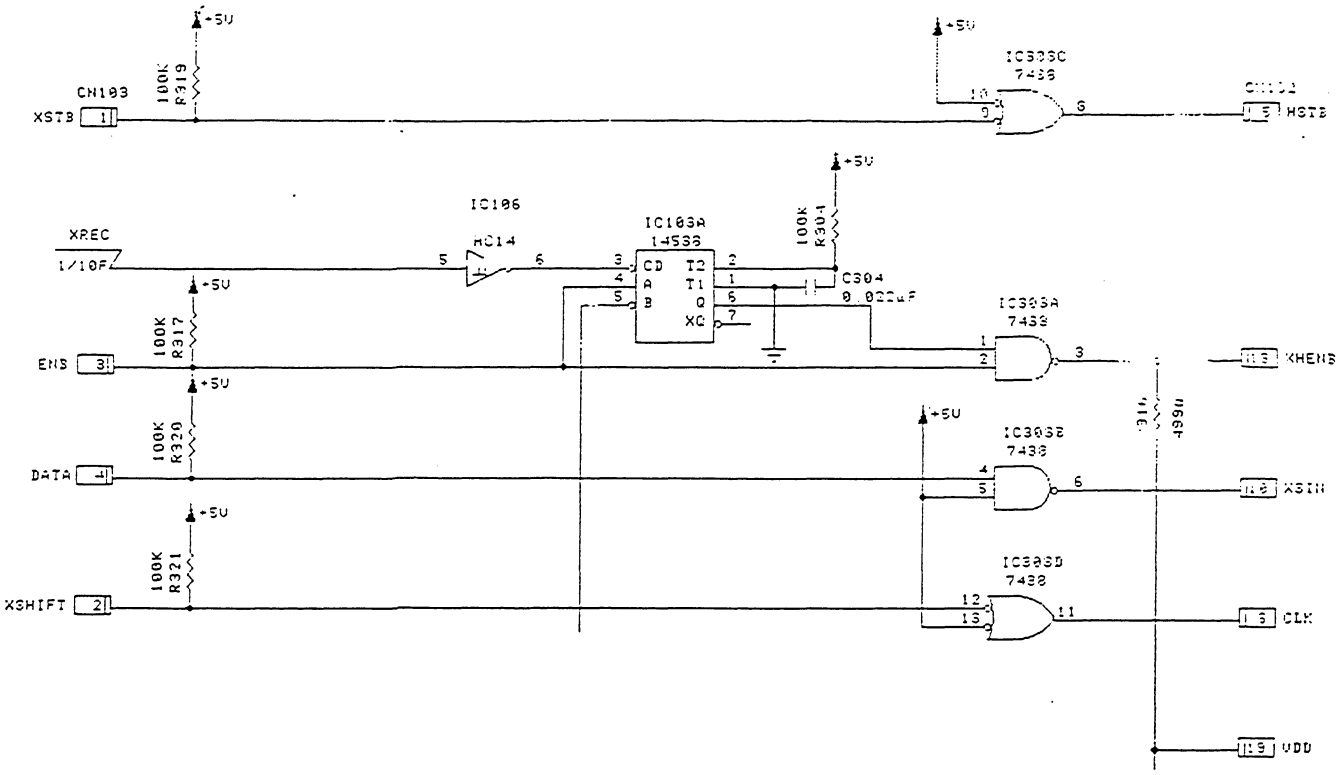


As the above figure, when motor speed decreases, the F-V converter output voltage drops below the reference voltage and then motor terminal voltage inscreases so that the motor speed increases. When F-V output voltage exceeds the reference voltage, motor terminal voltage drops to keep constant motor speed.

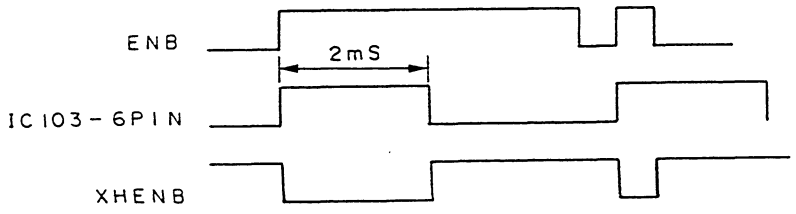


3.6.8 Thermal head driver

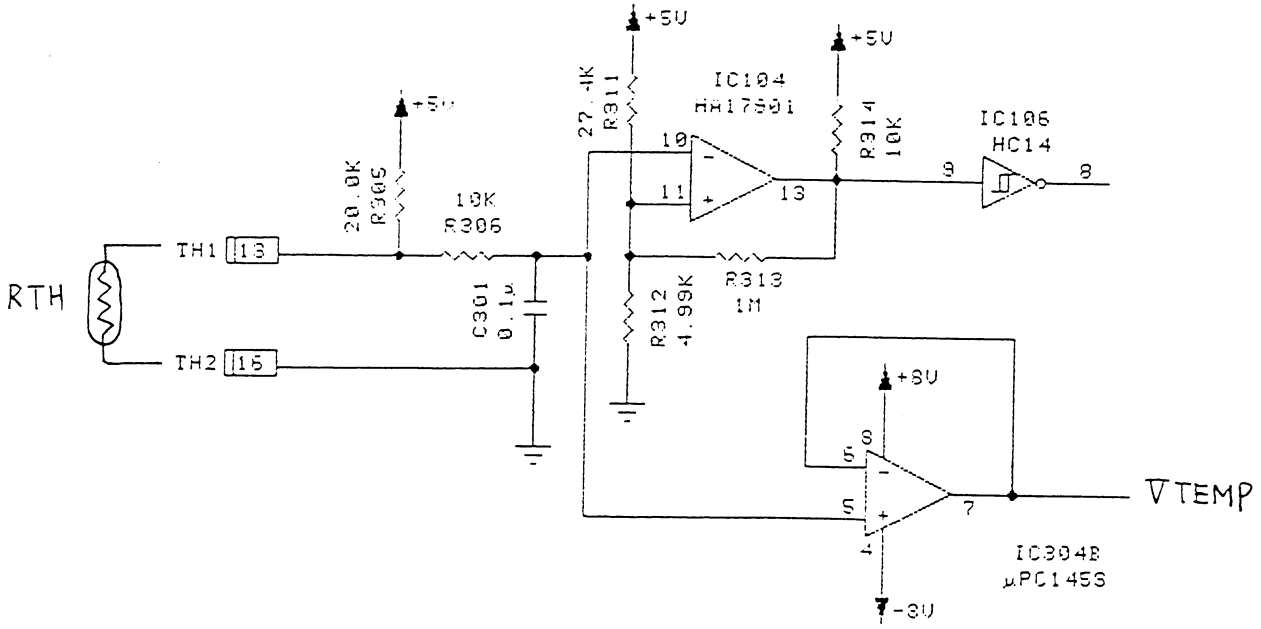
IC303 supplies the thermal head with XSIN, XHEMB, CLK, and HSTB signals.



XHEMB signal pulse width is limitted to maximum 2msec by the one-shot mutivibrator. When XREC is H level (recording is inhibitted) or IC106 pin-8 is L level (thermal head temperature is higher than 70°C), XHEMB becomes H lelvel to stop operation of the thermal head.



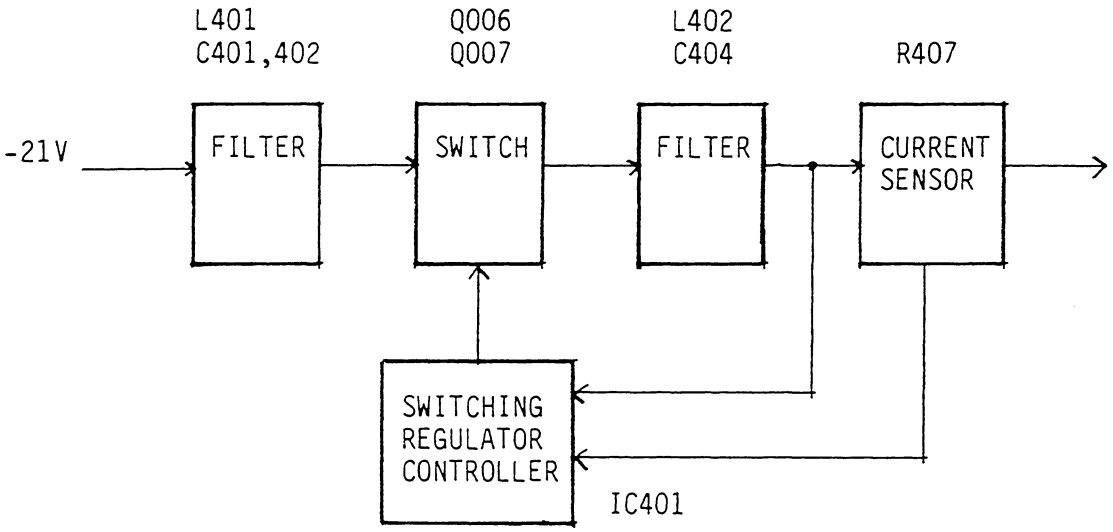
3.6.9 Head temperature detection



Thermistor RTH is provided on the thermal head to detect head temperature. VTEMP voltage corresponding to temperature is obtained by the R305, R306 and IC304. When temperature rises near 70°C, the IC104 comparator turns to L to set ENB (enable) signal of the IC103 to H to protect the thermal head.

Head temperature T (°C)	Thermistor resistance RTH (kohm)	Temperature voltage VTEMP (V)
-10	120.8	4.29
0	69.7	3.89
10	41.8	3.38
20	26.0	2.38
30	16.7	2.28
40	11.0	1.77
50	7.49	1.36
60	5.15	1.02
70	3.65	0.77

3.6.10 DC/DC converter



<VTH regulator>

VTH regulation is controlled by a hybrid IC (SWC-01). the SWC-01 changes the pulse width of its output to control the duration time of Q006 and Q007 on/off control signal so that VTH output voltage becomes stable.

<SWC-01>

SWC-01 has three control input terminals, for output voltage adjustment, for over-current protection and dead time control which cuts off output.

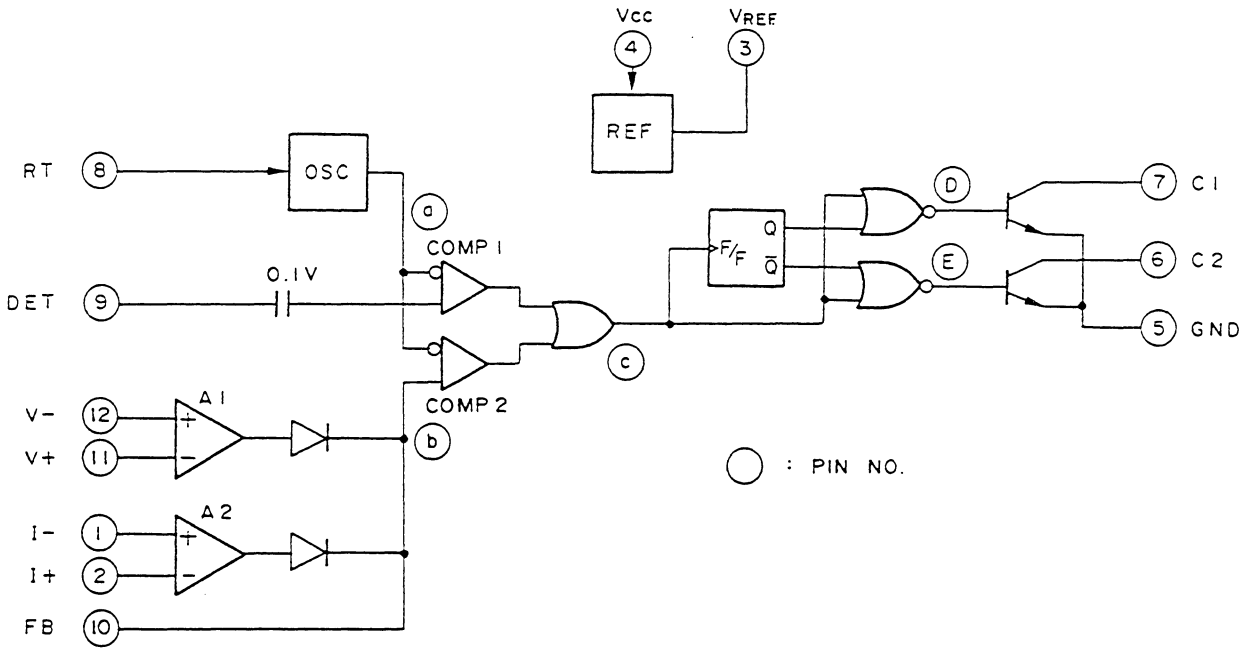
<Output voltage adjustment>

SWC-01 terminals 11 and 12 are diferential amplifier inputs and terminal 11 is internally connected to reference voltage. VTH voltage applied to terminal 12 adjustable by VR402 changes PWM (Pulse Width Modulation) comparator output pulse duration to control output voltage. This voltage is output from terminals 6 and 7 to Q006 and Q007 output control transistors.

<Over-current protection>

When current flow becomes large, voltage across R407 and Q001 base voltage become high. As the divided base voltage of Q001 is applied to the base of Q004, Q004 turns on when Q001 base voltage increases. When Q004 turns on, Q003 is pulled up to +5V and becomes off condition and then Q002 and Q001 turn off to decrease output voltage.

SWC-01 equivalent circuit

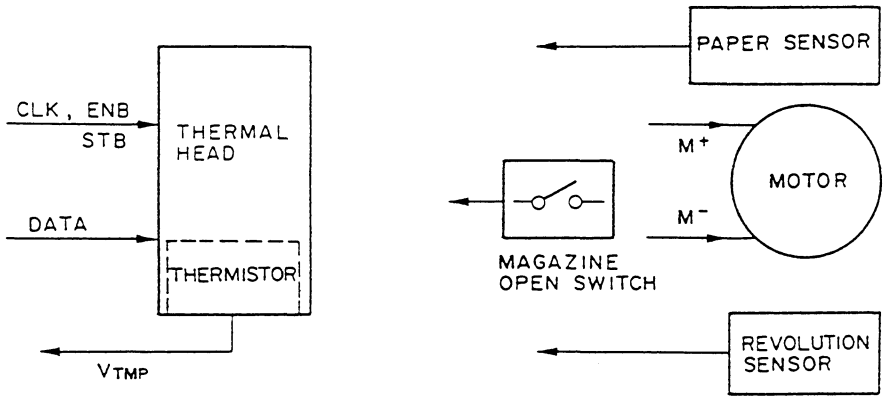


SWC-01 EQUIVALENT CIRCUIT

3.6.11 RG-712P recorder unit

1) General

RG-712P recorder unit consists of DC motor, sensors and thermal head. Details of the DC motor and sensors are described in the motor control for paper feed control circuit block.



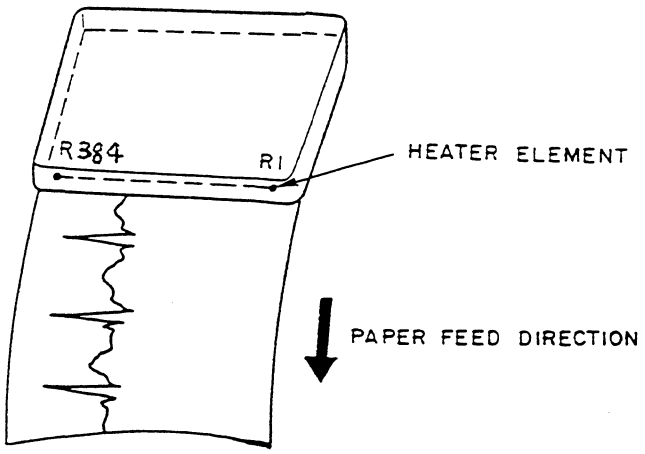
RECORDER UNIT RG-712P

2) Thermal head

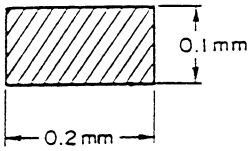
The thermal head consists of hearter elements, heater drive circuits and thermistor mounted on the heatsink.

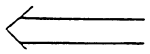
HEATER ELEMENT

There are 384 heater elements in the head in 8pcs./mm density.



Contact of the paper and each element is a square of 0.1mm hight and x 0.2mm width.





PAPER FEED DIRECTION

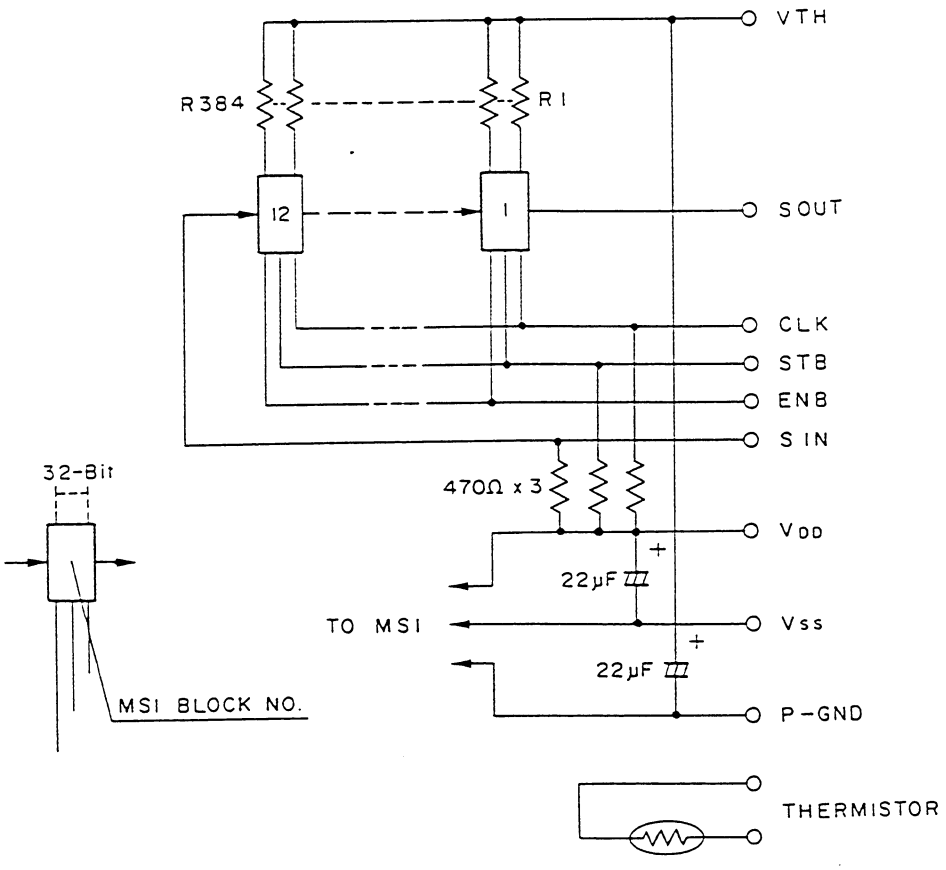
Heeter element resitance of the head is scattering in range of 183 ohm to 352 ohm and resistance of each dot in the head varies in ±15%.

Thermal head : 183 ohm - 352 ohm

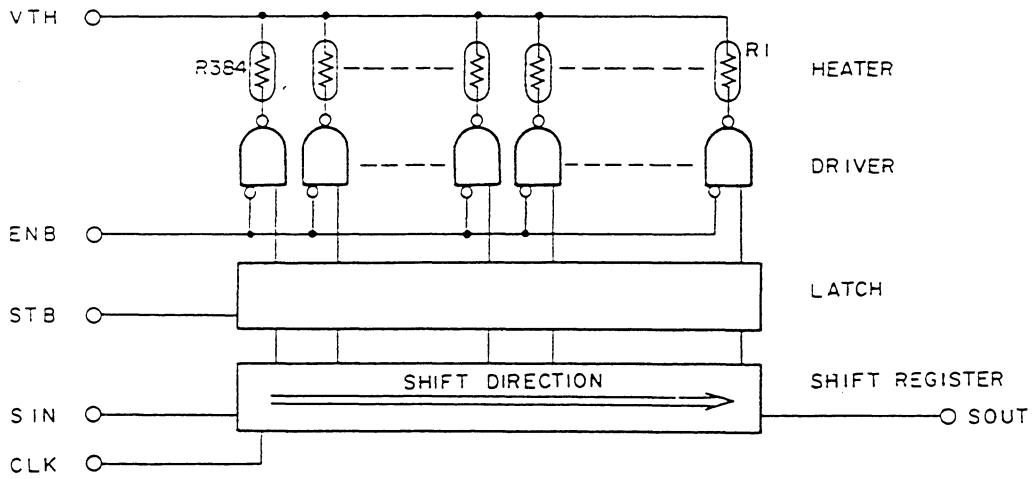
Element : ±15%

+5V VTH and +5V VDD are applied to the circuits. VSS is connected to digital ground E2 and P-GND is connected to ETH.

Serial data input (SIN), clock signal (CLK) and strobe signal (STB) are pulled up to +5V by 470 ohm resistors. In the thermal head there are 12 pieces of MSI blocks and each block contains shift resistor, latch, heater drivers and heater elements.



MSI blocks and thermal head



<MSI blocks>

12 MSI blocks compose of the thermal head and each block incluses shift registers, latches and heater drivers.

<Shift registor>

384 serial data are read every CLK timing and stored in parallel data format in the registor.

<Latch>

When ST (strobe) signal is input, 384 bit parallel data stored in the shift registor are latched at one time.

<Heater driver>

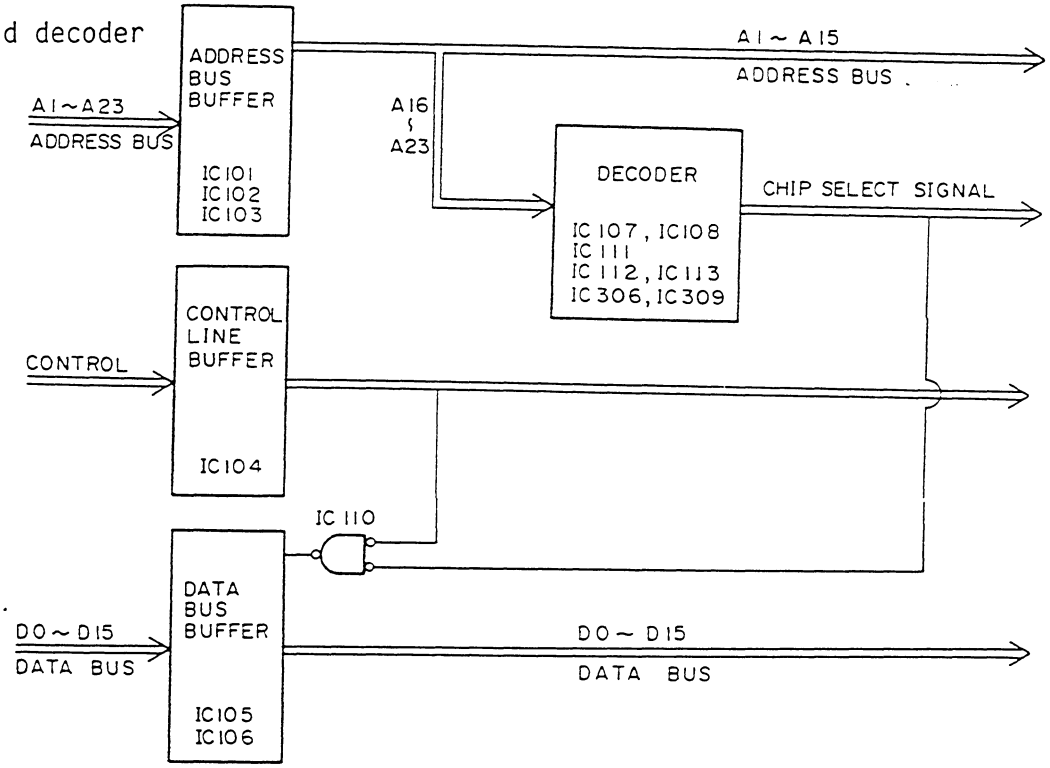
Driver drives the heater element. The driver is a gate which is activated only when ENB is input.

3.7 QI-809P (UP-0507) WS/IO board

3.7.1 General

WS/IO board is an interface provided with RAM (128kbyte), RAM (128kbyte), parallel data port by uPD71055C, serial data port bu uPD72001C, dual port RAM by MB8421, and single port RAM by MB8421.

3.7.2 Bus buffer and decoder



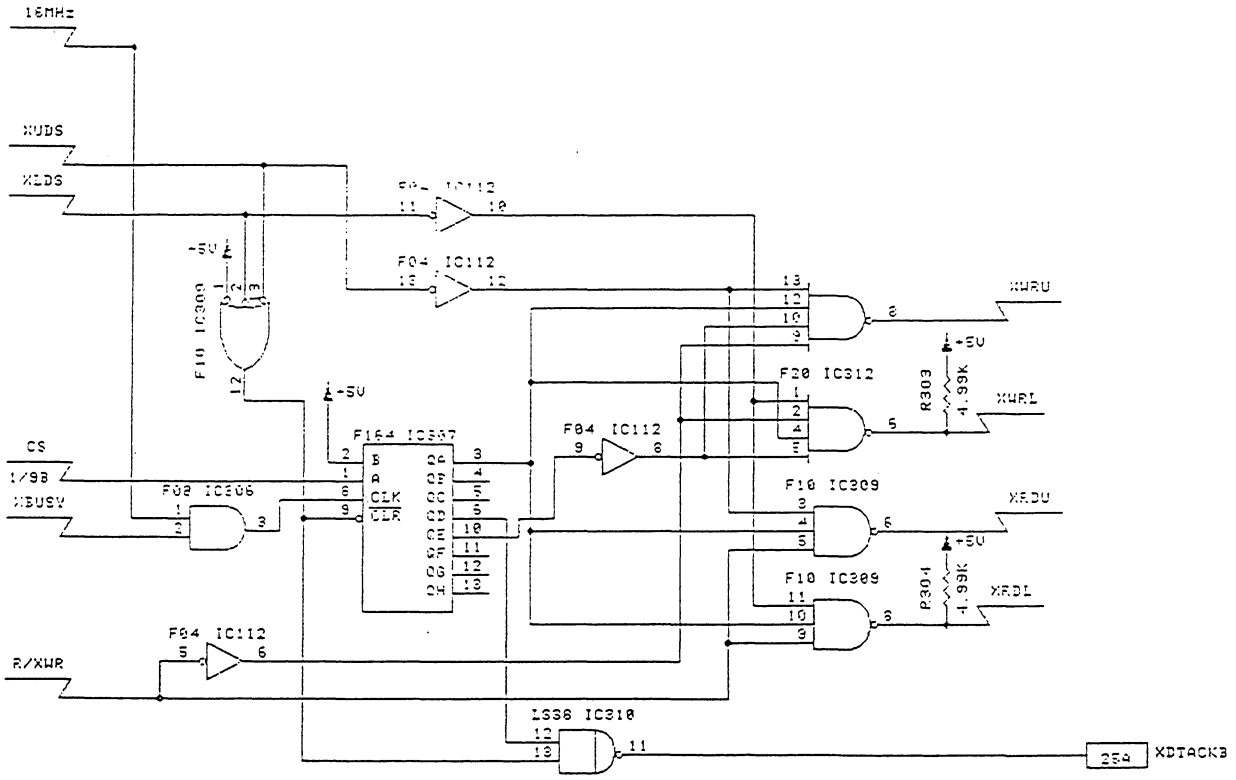
IC101, IC102, and IC103 (HCT240) are for address bus buffer, IC104 (HCT244) is for control line buffer, and IC105 and IC106 are for data bus buffer. IC107, IC108 and IC113 (HC138), IC111 (LS30), IC112 (F04), IC306 (F08) and IC109 (F20) are for address decoder.

IC110 (HC12) is for gate open/close control of the data bus buffer.

Decoder asserts each CS (Chip Select) signal in the following address spaces:

CS	Address	Device
XCS2	D40001H- D40007H	uPD72001C
XCS1	D80000H- D80FFFH	MB8421 (dual port RAM, lower byte only is used)
XCS0	DC0001H- DC0007H	uPD71055C
XCS3	F00000H- F1FFFFH	ROM 128kbyte
XCS4	F80000H- F8FFFFH	SRAM 64kbyte
XCS5	F90000H- F9FFFFH	SRAM 64kbyte

3.7.3 XWR, XRD and XDTACK signals



When an address inside the WS/IO board is accessed, decoder operates and CS signal connected to the pin-1 of IC307 (F164) is asserted to H. If XBUSY signal is negated, 16MHz clock is inputted to the pin-8 of IC307 (XBUSY is asserted when same address is accessed from both Left and Right ports of the IC401 (MB8421 dual port RAM)). Reset of IC307 is released when Data Strobe Signal (XUDS or XLDS) is asserted. After this, 16MHz clock rising edge sets the QA output pin-3 to H.

<Rwite cycle>
When R/XWR line is L (Write cycle), R/XWR line is inverted by IC112 (F04) and inputted to pin-2 and pin-9 of IC312 (F20). QA output (H) of IC307 is inputted to pin-4 and pin-12 of IC312. At this condition, QE output of IC307 is L, and the QA output is inverted by IC112 and inputted to pin-5 and pin-10 of IC312.

NOTE: IC312 output pin-8 becomes XWRU (U: Upper) signal and pin-6 becomes XWRL (L: Lower). This indicates that upper byte and lower byte Write signals are independently provided. Write signal is asserted according to the Data Strobe Signal assertion (XUDS or XLDS). When XLDS is asserted (L), the inverted XLDS by IC112 is inputted to pin-1 of IC312, and XWRL is asserted. In the same manner, XUDS is inverted by IC112 and inutted to pin-13 of IC312 to assert XWRU.

After IC307 is reset, 4th rising edge sets the QD output to H which is inputted to pin-12 of IC310 (LS38).

As the IC307 Reset signal is connected to pin-13 of IC310, this line is H and output of pin-11 (XDTACK) signal becomes L when IC307 QD terminal becomes H to inform the CPU that the Write cycle has completed. At the 5th rising edge of the clock inputted to the clock input of IC307, QE output becomes H, XWRU and XWRL are negated, and Write cycle ends.

<Read cycle>
Basically, Read cycle is same as Write cycle and XRDU and XRDL signals exist. Accessing process is same as Write cycle till the XDTACK signal returns to the CPU.

In Read cycle, the cycle ends by negating XUDS or XLDS signal after retuning XDTACK singal to the CPU while in Write cycle the cycle ends by negating the Write signal at QE output of IC307 from assertion.

NOTE: Output pin-6 of IC312 is pulled up by R303 (4.99k) so that output level is shifted to match input pin of a C-MOS device. Output pin-8 of IC309 is also pulled up.

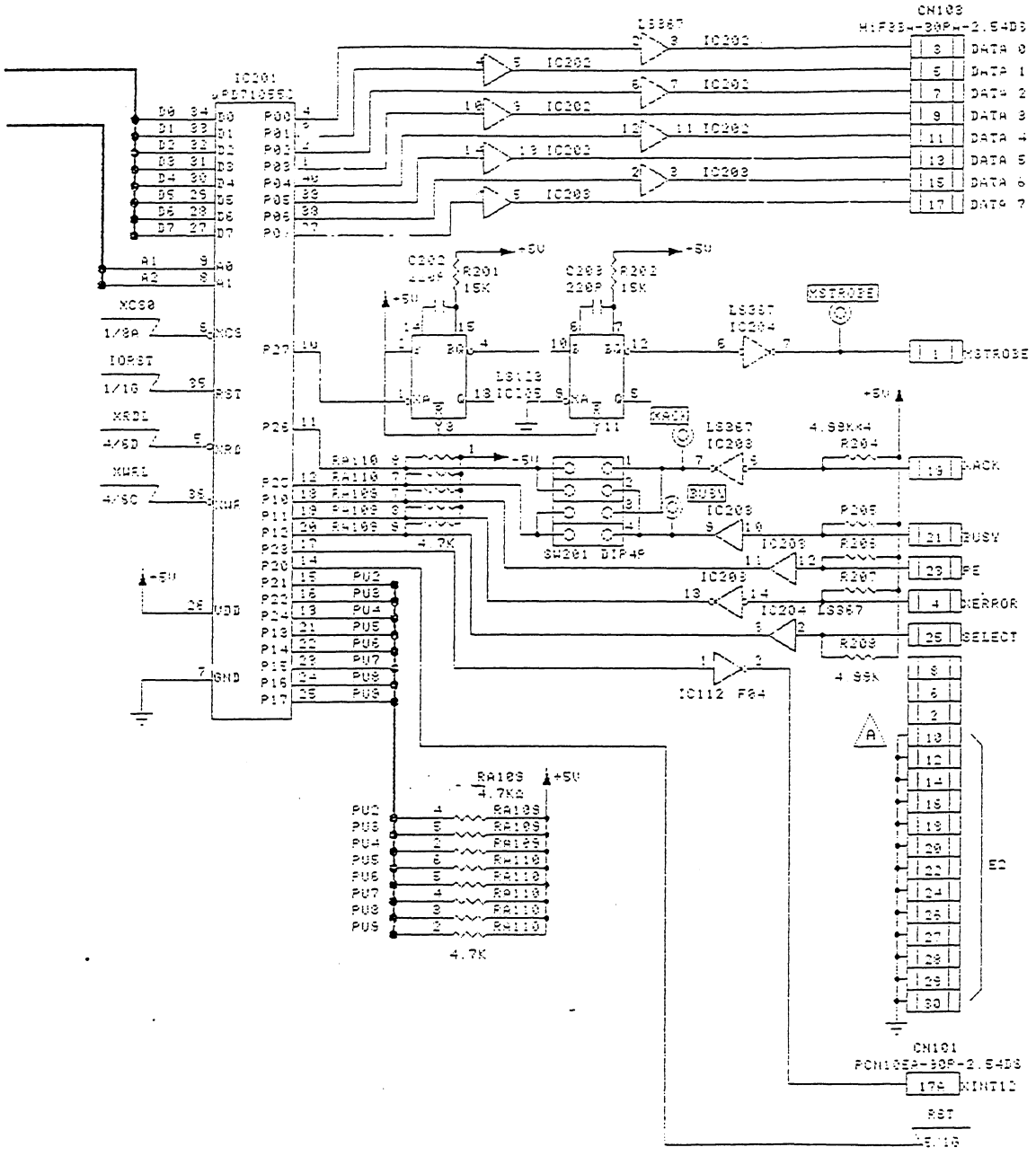
3.7.4 ROM

ROM is composed of 64kbyte IC210 and IC211. 128kbyte address space from F00000H is occupied and XCS3 chip select signal asserts this space.

3.7.5 RAM

RAM is composed of 32kbyte SRAM IC212 through IC215 and 128kbyte address space from F80000H is occupied and XCS4 chip select singal asserts from F80000H to F8FFFFH, and XCS5 asserts from F90000H to F9FFFFH.

3.7.6 Parallel data port



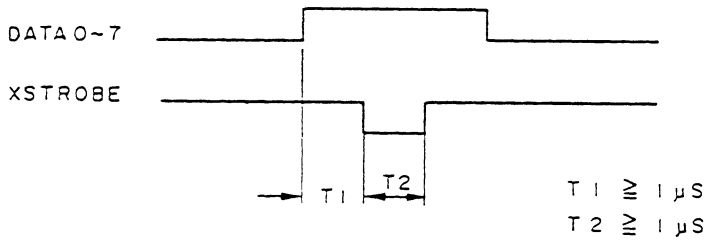
3.7.6.1 Device

uPD71055C is used for parallel data output port (for parallel format printer). 8 bit data outputted from IC201 P0- P7 is buffed by IC202 and IC203 (LS367) to enforth drive capability and connected to the CN103 connector (PARALLEL) on the rear of the central monitor main unit.

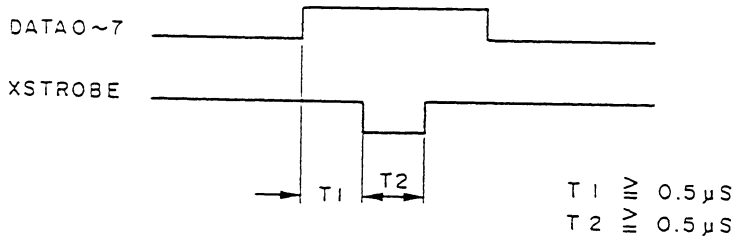
<XSTROBE signal>
XSTROBE signal, an output of IC201 P27, is outputted by synchronizing its timing by IC205 (LS123) to match various printers.

XSTROBE signal for Sentronics communication

Ex. NEC printer

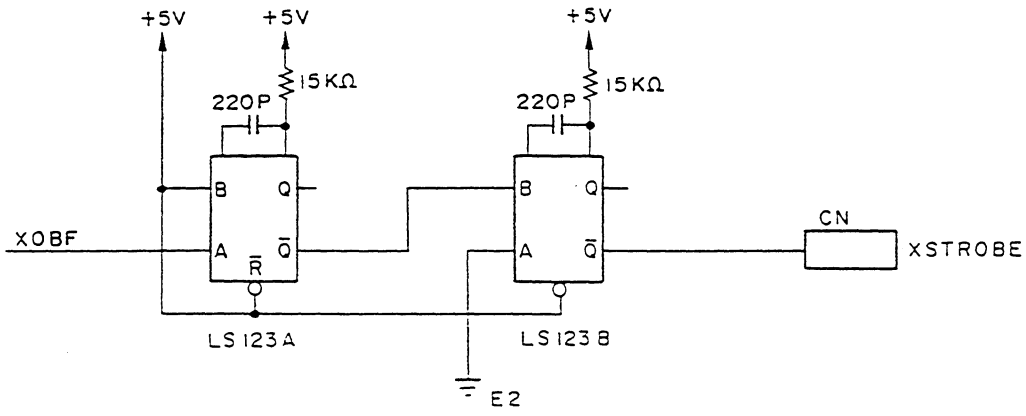


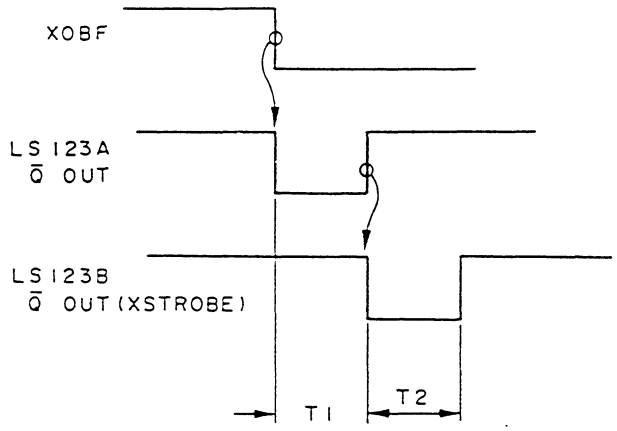
Ex. HP printer



In this unit, wider pulse timing signal for NEC printer is employed.

As the original signal cannot be used as the XSTROBE signal, circuit below is used to match the timing to the printer.

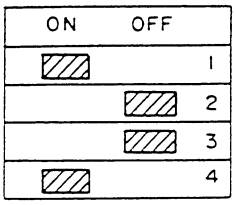




T1, T2 = 0.45 x 220p x 15kohm = 1.188us

3.7.6.2 XACK, BUSY signals and SW201 (4 bit DIP switch)

Printers available in the market sometimes have XSTROBE and BUSY lines only. SW201 is to select the XACK line and BUSY line. For the printers provided with XACK and BUSY lines, the SW201 is set as below.



Both XACK and BUSY signals are buffed by IC203.

3.7.6.3 PE, XERROR, and SELECT signals

These lines are buffed by IC203 and IC204 (LS367) and inputted to IC201.

PE: H when paper is empty

XERROR: L when the printer is reporting an error

SELECT: H when the printer is connected

3.7.6.4 XINT12 signal

IC201 P23 sets the XINT12 line to H during Output Buffer Empty. This line is inverted by IC112 (F04) and used for interrupt request to the CPU.

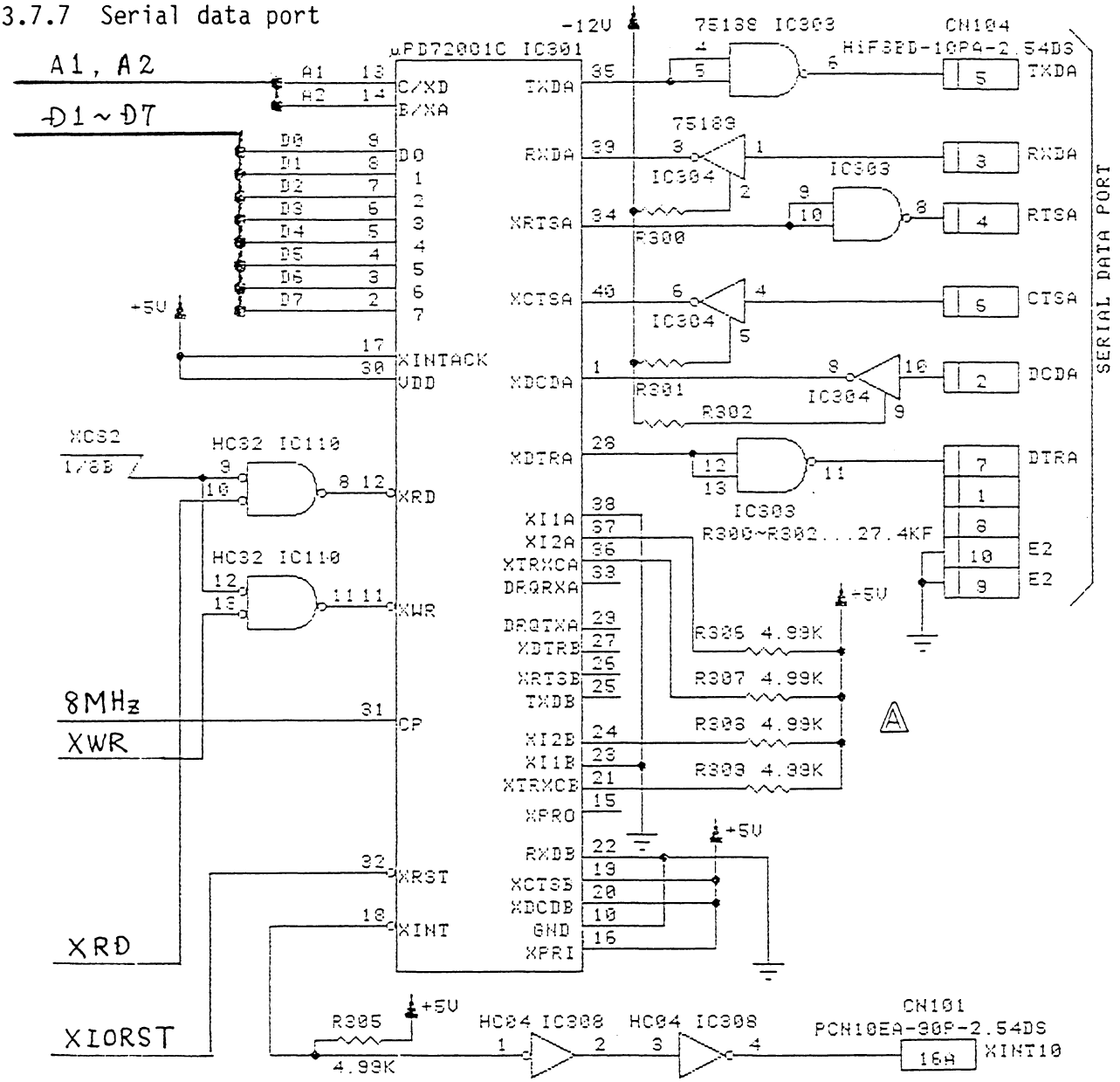
3.6.7.5 RST signal

RST signal resets the WS-841R thermal array recorder by software. This bit is H while resetting.

3.6.7.6 Pulling up the unused input pins

IC201 P21, P22, P24, P13 through P17 are unused and pulled up to +5V by RA109 and RA110 resistor arrays.

3.7.7 Serial data port



IC301 (uPD72001C) is employed for serial data I/O port. uPD72001C provides A and B ports, however, port A only is used in this circuit.

Baud rate clock is not externally inputted and 8MHz system clock inputted to pin-31 is used for baud rate clock by the command at system initialize. Command and data are determined by A1 input to pin-13.

Data bus D0- D7 are for Transmit Data access when A1 = 0 and XWR = 0. Data bus D0- D7 are for Receive Data access when A1 = 0 and XRD = 0. Data bus D0- D7 are for Command access when A1 = 1 and XWR = 0. Data bus D0- D7 are for Status Register Data access when A1 = 1 and XRD = 0.

A2 input to pin-14 selects the I/O port A or B.

A2 = 0: Port A selection
A2 = 1: Port B selection

Pin-32 (XRST) is connected to XINRST and when CPU outputs Reset Command, IC 301 is reset.

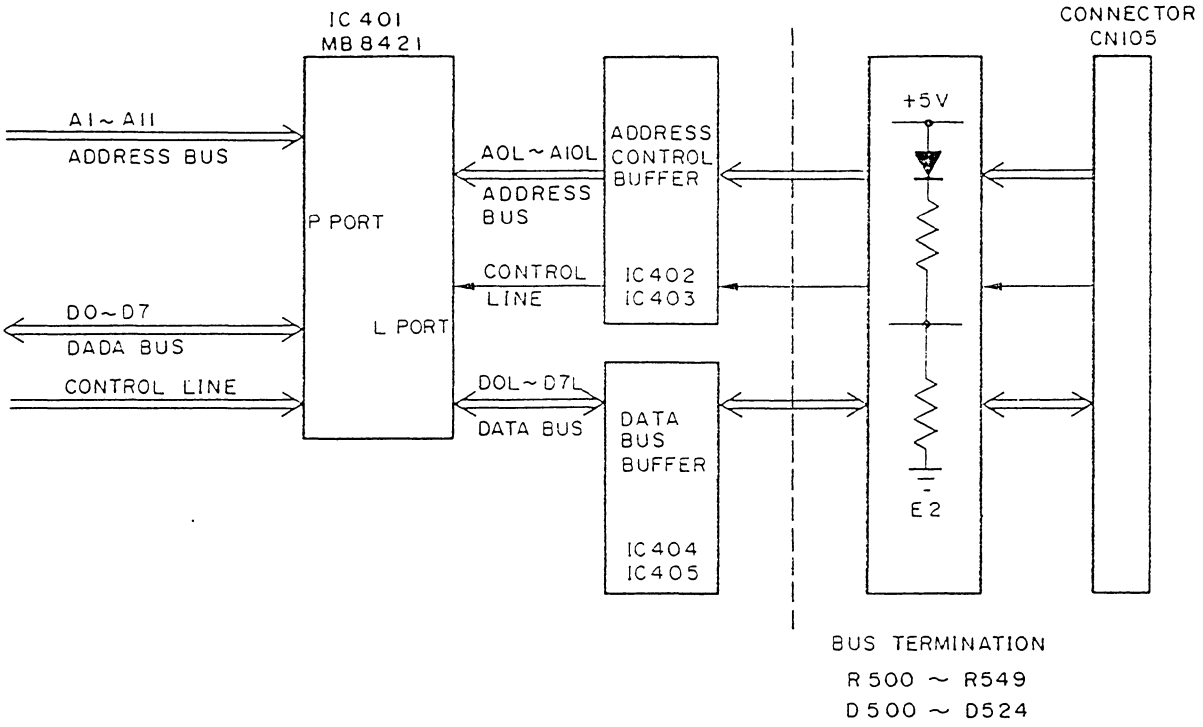
Pin-18 (XINT) is connected to CPU board XINT10 line which is asserted when IC301 requests interrupt (Transmit Buffer Empty, Receive Data Available, External Interrupt condition, etc.) to the CPU.

In the TxD (Transmit Data), XRTS (Request To Send), and XDTR (Data Terminal Ready) lines, line driver device IC303 (75188) is inserted. After IC303, signal level of 0V to 5V is changed to -12V to 12V.

In the RxD (Receive Data), XDCD (Data Carrier Detect), and XCTS (Clear To Send) lines, line receiver device IC304 (75189) is inserted. After IC304, signal level of -12V to 12V is changed to 0V to 5V.

IC304 pin-2, pin-5 and pin-9 are pulled down to -12V by R300, R301 and R302 (27.4kohm) to make hysteresis in received data.

3.7.8 Dual port RAM (for WS-841R thermal array recorder)



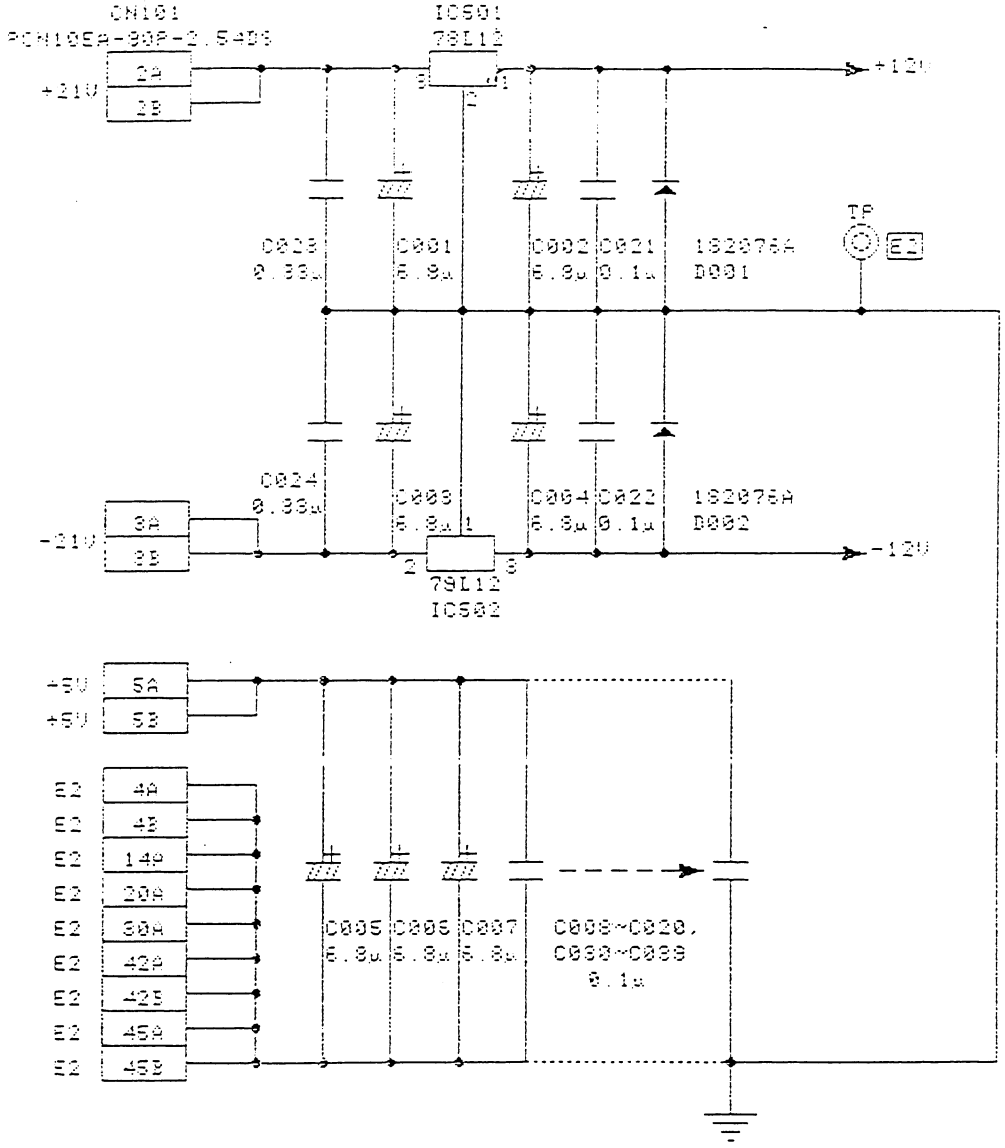
Dual port RAM IC401 (MB8421) is for Receive/Transmit data and command between the WS/IO board and the externally connected WS-841RA/J/K thermal arrray recorder.

Address bus, data bus and control lines from the CPU that control the WS/IO are inputted to the IC401 R (Right) port while address bus from the WS-841R is inputted to the IC401 L (Left) port. This address bus is inputted from the CN105 connector (WS) on the rear panel of the central monitor main unit and connected to the IC401 L port through the terminator composed of resistors and diodes, and address bus buffer composed of IC402 and IC402 (LS244). In the same manner as the address bus lines, control lines are connected to the IC401 L port thorugh the bus terminator and buffer.
Data bus lines from the WS-841R are inputted from the CN105 and after bus terminator, the lines are buffed by differenct buffers during Read cycle and Write cycle.

a) Write cycle
Data is connected to the IC401 data bus through the data bus buffer IC404 (LS244).

b) Read cycle
Data is outputted from the IC401 and connected to the WS-841R through the data bus buffer IC405 (LS641). XINT and XBUSY signal from the IC4301 L port are inverted by IC406 (LS04) to change the format to open collector output and inverted again by IC310 (LS38). These reinverted lines are also of open collector output format.
XINT signal from the IC401 R port is buffed twice by IC308 (HC04) and inputted to the INT11 terminal.
XINT and XBUSY lines on both R and L ports are pulled up by 4.99kohm resistors to match the signals to the open drain format XBUSY and XINT terminals of the device.

3.7.9 Voltage regulators



3.7.9.1 +12V power

Three-terminal voltage regulator IC501 (78L12) regurates +21V power from the mother board into +12V power. C001, C002, C021 and C023 are for noise reduction.

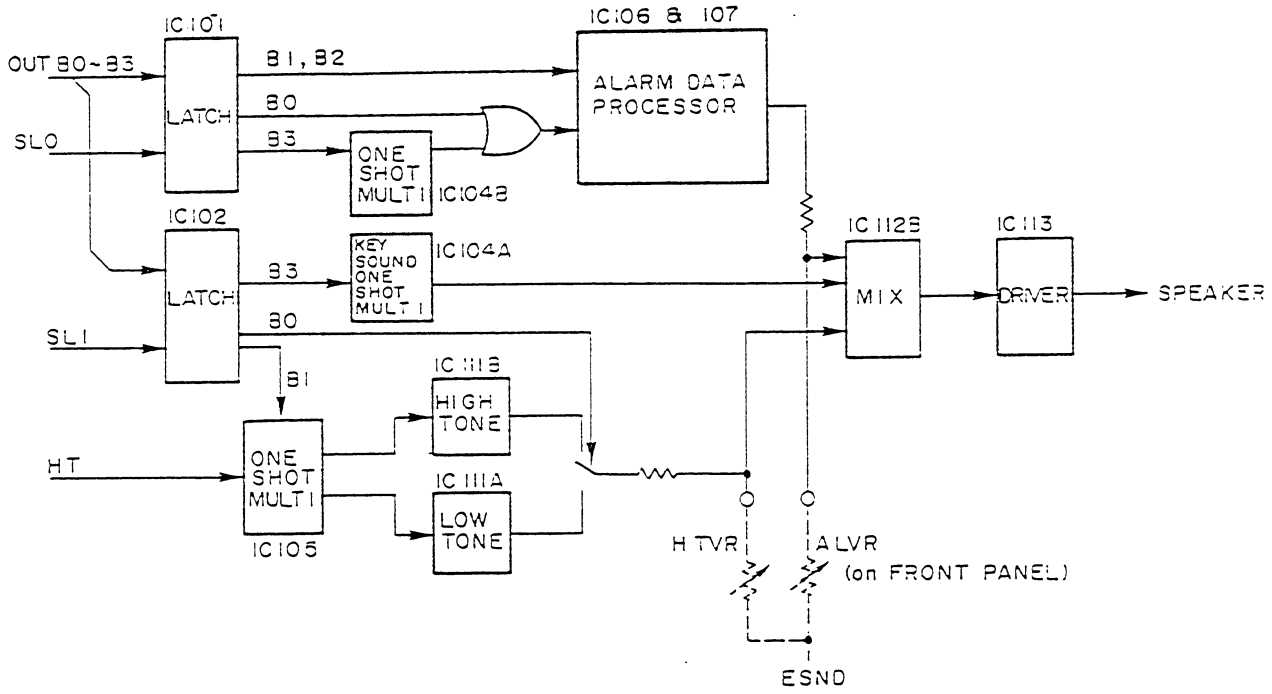
3.7.9.2 -12V power

Three-terminal voltage regulator IC502 (79L12) regurates -21V power from the mother board into -12V power. C003, C004, C022 and C024 are for noise reduction.

3.7.9.3 +5V power

+5V power is directly inputted from the mother board. C005 to C007, C008 to C020, C030 to C039 are for noise reduction.

3.8 UP-0265 Sound control board



The board is controlled by the keyboard/display controlller IC176 (8279) on the CPU board.

The tone setting is executed by latching the output signals (OUTB0- OUTB3) from the IC176 with the scan lines (SL0- SL1) as shown in the following table.

SL	OUTB	Tone
SL0	B0	Continuous alarm tone 0: Off 1: On
	B1	Alarm tone-1 (B1,B2) = (0, 0): Ding Dung
	B2	Alarm tone-2 (0, 1): Ping Pong
		(1, 1): Poung
	B3	Single alarm tone on/off 0: Off 1: On
SL1	B0	QRS synch. tone HI/LO 0: Low 1: High
	B1	QRS synch.tone on/off 0: Off 1: On
	B2	No function
	B3	Key click tone of/off 0: Off 1: On

3.9 UP-0481, 0482, 0483, 0456 MU operation boards

3.9.1 General

Operation boards are controlled by 8279 keyboard/display controller device on the CPU board. Major functions of the 8279 are as follows:

1) LED display control
   . Recorder incdication lamp-1 to lamp-8 can be freely lit
   . Alarm indication lamp-1 to lamp-8 can be freely lit
   . Only one of bed indication lamp-1 to lamp-8 can be lit
   . SYSTEM ALARM, ALARM, and CALL lamps can be lit

2) Volumes

   . CRT brightness volume on the front panel
   . Alarm tone volume on the front panel

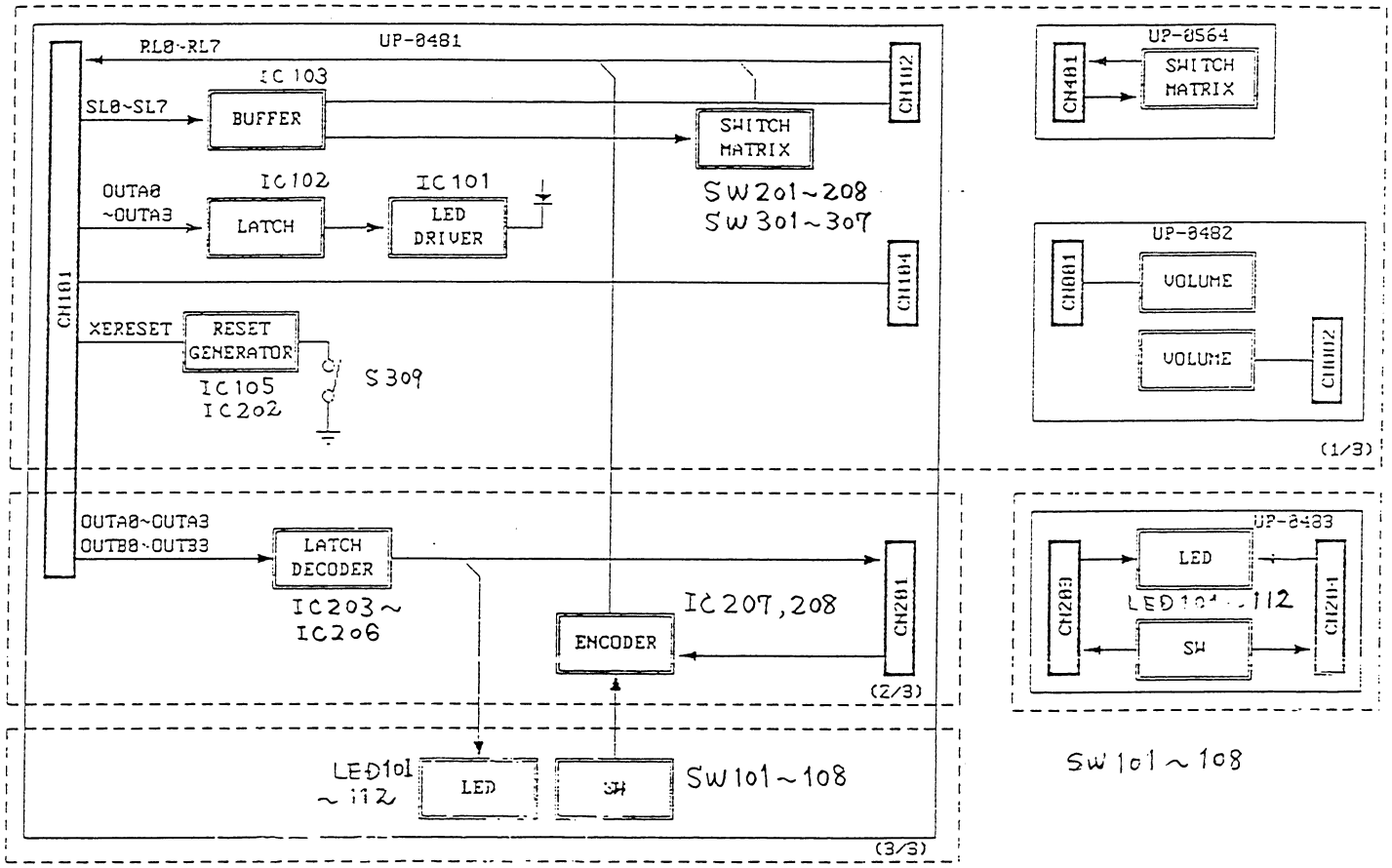
3.9.2 Circuit block descriptions

1) Latch
Data OUTA0- OUTA3 and OUTB0- OUTB3 from the 8279 controller are latched by scan lines (SL) to generate a recording indication lamp signal and alarm indication lamps.

2) LED driver
Drives the LED lamps accroding to the above latched signals.

3) Reset circuit
Counter starts counting while the RESET switch is pressed to reset the CPU.

3.9.3 Operation boards



SL0- SL3 (Scan Lines) from the 8279 are connected to the switches through the buffer IC103 and when switches are pressed, switch condition is sent to the 8279 through the RL0- RL7 (return lines). Only when the SW309 SELF CHECK is pressed, counter IC105 starts counting and if the switch is pressed for longer than three seconds, XERESET turns to L from H and the main CPU is reset and SELF CHECK PROGRAM screen is called up on the CRT.

3.9.4 8279 Key input terminal (individual bed's keys)

Bed select key by Scan Line SL0

Bed ID	RL0	RL1	RL2	RL3
1	H	H	H	L
2	L	H	H	L
3	H	L	H	L
4	L	L	H	L
5	H	H	L	L
6	L	H	L	L
7	H	L	L	L
8	L	L	L	L

Record select key by Scan Line SL1

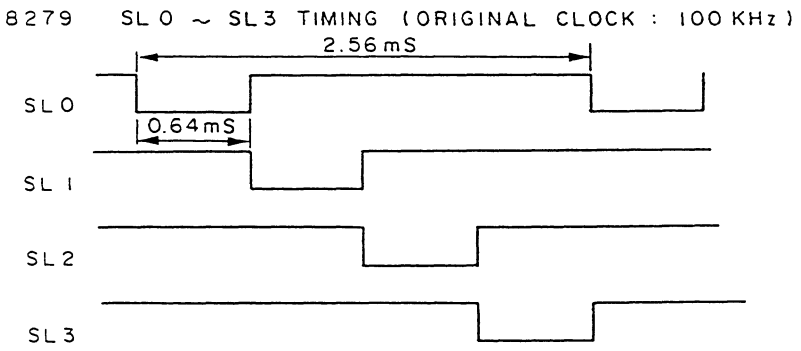
Bed ID	RL0	RL1	RL2	RL3
1	H	H	H	L
2	L	H	H	L
3	H	L	H	L
4	L	L	H	L
5	H	H	L	L
6	L	H	L	L
7	H	L	L	L
8	L	L	L	L

3.9.5 8279 Key input terminals (other keys)

SL / RL	SL3	SL2	SL1
RL0	MF0 SW401	SETUP SW301	ARRHY SW201
RL1	MF1 SW402	SYSTEM SETUP SW302	TREND SW202
RL2	MF2 SW403	ALARM LIMITS SW303	ETC SW203
RL3	MF3 SW404	VPC LEARN SW304	OTHER BEDS SW204
RL4	MF4 SW405	EXT REC SW305	SUSPEND SW205
RL5	MF5 SW406	REC PATT SW306	FREEZE SW206
RL6	None	REPORT SW307	INDIV BED SW207
RL7	None	Spare SW308	ALL BEDS SW208

MF: Multi-Function key

8279 SL0- SL3 timing (basic clock: 100kHz)



3.9.6 8279 output terminals (LED display and tone generation control)

Scan line	Output	Remarks
SL0	OUTA3	CALL lamp
	OUTA2	ALARM lamp 1: On 0: OFF
	OUTA1	REPORT lamp
	OUTA0	EXT REC lamp
	OUTB3	Single alarm tone 1: On 0: Off
	OUTB2	Alarm tone-2
	OUTB1	Alarm tone-1 * NOTE
	OUTB0	Continuous alarm tone mode 1: On 0: Off
SL1	OUTA3	Display on/off bit 1: On 0: Off
	OUTA2	Select LED lamp of the selected bed by decoding
	OUTA1	OUTA0- OUTA2 Ex. Bed 1: (OUTA2,1,0) = (0,0,0)
	OUTA0	
	OUTB3	Key click tone 1: On 0: Off
	OUTB2	SYSTEM ALARM lamp 1: On 0: Off
	OUTB1	QRS synch. tone On/Off 1: On 0: Off
	OUTB0	QRS synch. tone HI/LO 1: High 0: Low
SL2	OUTA3	Record lamp bed8
	OUTA2	Record lamp bed7
	OUTA1	Record lamp bed6
	OUTA0	Record lamp bed5 1: On 0: Off
	OUTB3	Record lamp bed4
	OUTB2	Record lamp bed3
	OUTB1	Record lamp bed2
	OUTB0	Record lamp bed1
SL3	OUTA3	Alarm lamp bed 8
	OUTA2	Alarm lamp bed 7
	OUTA1	Alarm lamp bed 6
	OUTA0	Alarm lamp bed 5 1: On 0: Off
	OUTB3	Alarm lamp bed 4
	OUTB2	Alarm lamp bed 3
	OUTB1	Alarm lamp bed 2
	OUTB0	Alarm lamp bed 1

* NOTE: (Alarm tone-2,1) = (0, 0): Ding Dong
(Alarm tone-2,1) = (1, 0): Ping Pong
(Alarm tone-2,1) = (1, 1): Poung

3.10 Power supply unit

The power supply unit is composed of the power transformer unit (SC-001RA/J/K) and the following power regulator unit (UP-0315).

3.10.1 General

The power regulator unit, UP-0315, consisits of the following circuits:

1) +60V regulating circuit
2) Overheat protectors (for 5V and 60V) and power down detector (for 5V)
3) +5V regulating circuit
4) ±21, ±8, ±12V power generating circuit

Each power is used as follows:

Output voltage (V)	Processing method	Use
+60	Dropper	for CRT unit
+5	Chopper (switching)	for digital circuit
+21	Rectifier (unregulated)	for +12V, +15V three terminal regulators
-21	Rectifier (unregulated)	for -12V, -15V three terminal regulators
+8	Regulator	for analog circuit
-8	Regulator	for analog circuit
-12	Rectifier (unregulated)	for fan motor

3.10.2 +60V regulating circuit

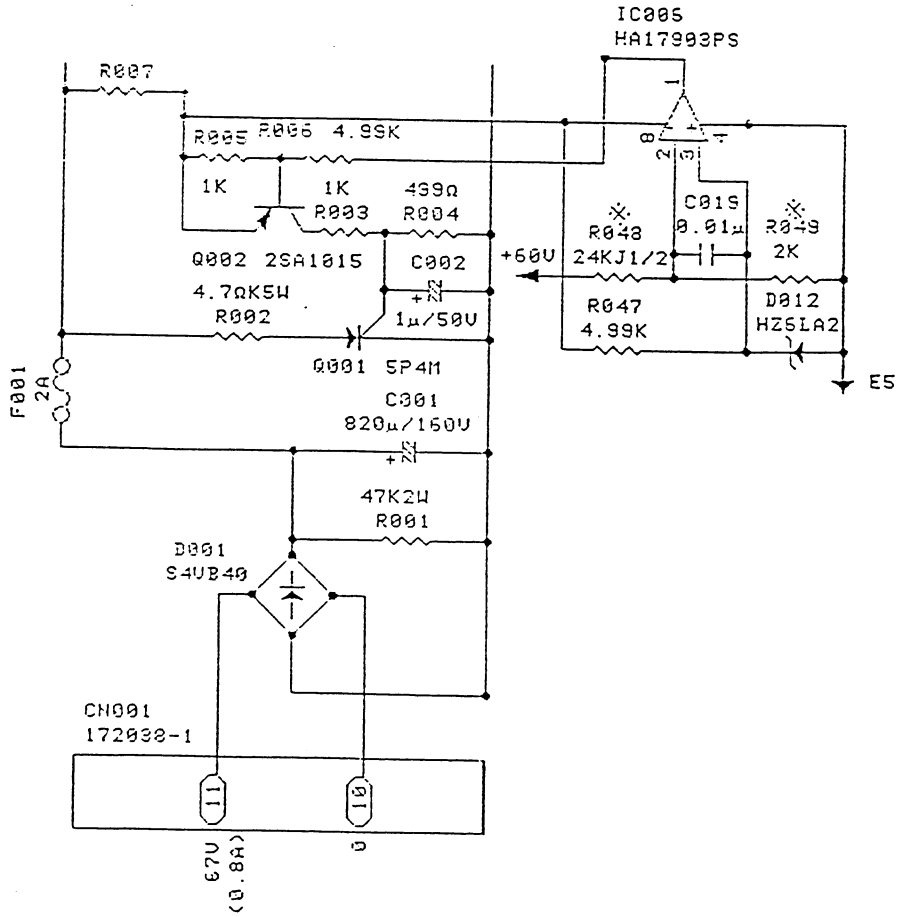
The circuit consists of the rectifier, overvoltage protector, +60V regulator with overcurrent protection and LED output indicator.

3.10.2.1 Overvoltage protector

The circuit is located after the rectifier (D001) and mainly composed of the Zener diode (D012), comparator ((IC006), thyristor (Q001) and transistor (Q002).

The circuit protects all the parts against overvoltage as follows:

When the +60V power exceeds +60V, the comparator (IC006) outputs 0V by comparing the voltage divided by the resistors (R048/049) with the constant voltage (+6V) on the zener diode (D012). The transistor (Q002) and thyristor (Q001) are set to "ON" by the comparator output, 0V. the 2A fuse (F001) opens up since a heavy current is pulled in the thyristor.



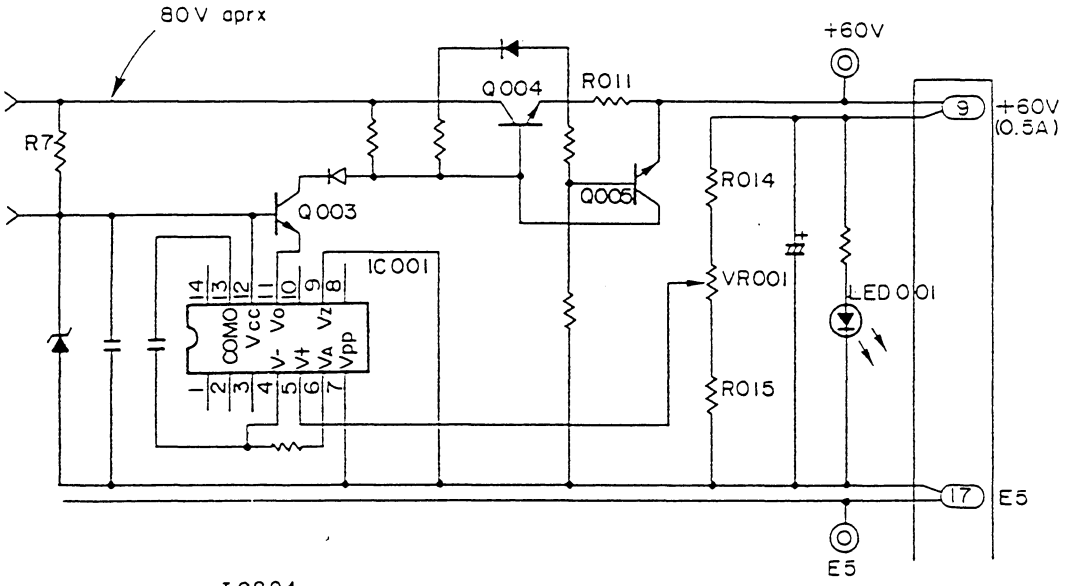
3.10.2.2 +60V regulator with overcurrent protection

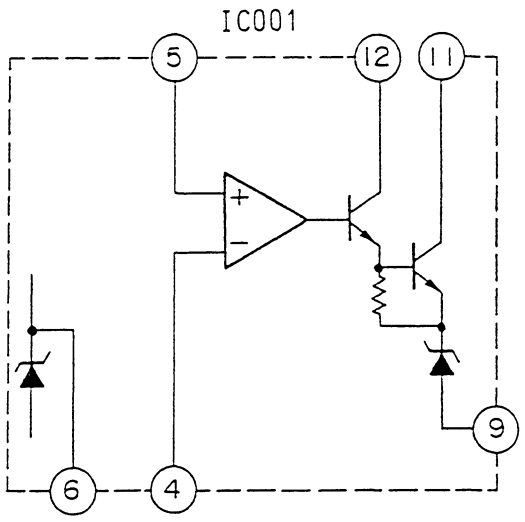
The circuit mainly consists of the regulator (IC001), transistors (Q003-005), variable resistor (VR001) and resistors (R014/015).

The transistor (Q005) protects all the parts against an overcurrent as follows:

When the output current from the +60V power exceeds 0.5A, the resistor (Q005) starts to operate since the current results in a voltage drop across trhe resistor (R011). The transistor (Q005) operates to decrease the bias voltage between the base and emitter of the transistor (Q004) so as to decrease the current.

The combination of R014, VR001 and R015 functions as a voltage feedback control loop to the regulator (IC001). The VR001 is an output voltage control for the +60V power.

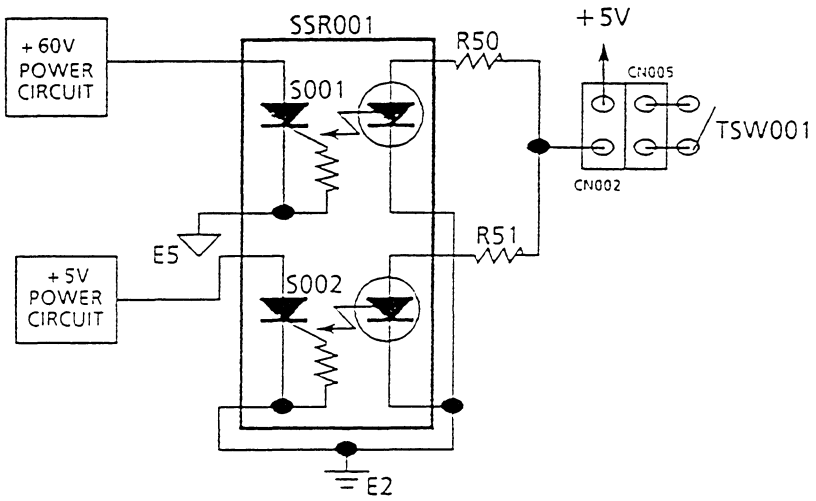




HA17723G
(Equivalent circuit)

3.10.3 Overheat protector and power down detector

3.10.3.1 Overheat protector (90°C or more)

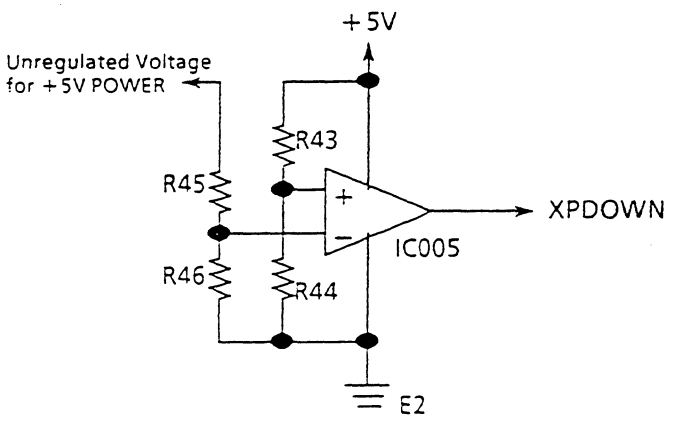


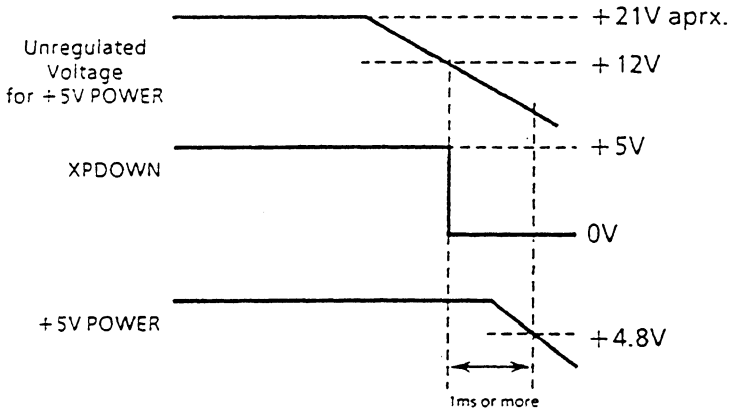
If the main unit (MU-820RA/J/K) warms up to 90°C or more due to a fan motor malfunction, the circuit stops the main thermal source, +5V and +60V power, to protect all the parts against overheating, as follows:

The thermal switch (TSW001) is turned on by overheating (90°C or more) though the normal condition of the TSW001 is off. In the thyristor switch (SSR001), the internal photo-thyristors (S001, S002) are turned on. The fuse (F001) opens up due to the S001 operation to stop the +60V power while the S001 is connected to the overvoltage protector in parallel. The transistor (Q009) is set to "OFF" due to the S002 operation to stop the +5V power while the S002 is connected to the base of the Q009 on the +5V regulating circuit. After the TSW001 is turned off from the "ON" condition because the temperature has lowered (less than 90°C), the +60V power circuit needs fuse replacement due to a blown fuse, though the +5V power regulating circuit recovers.

[Note]
Before fuse replacement, check the cause of the overheat.

3.10.3.2 Power down detector

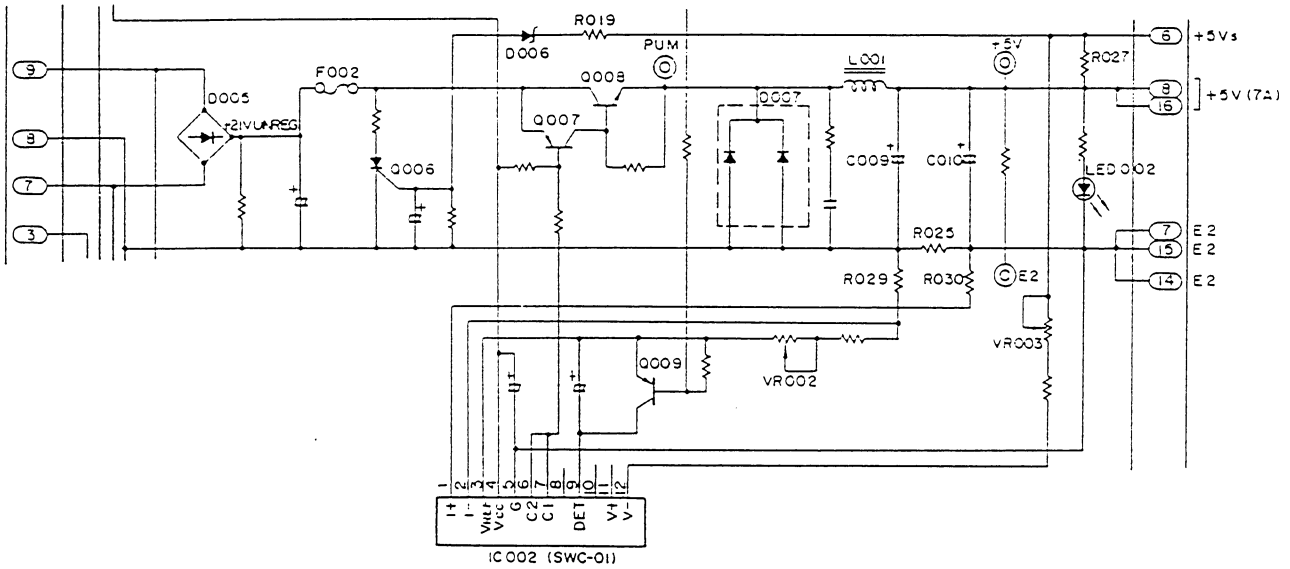




When the power source fails, the circuit detects the power down condition prior to 1msec. or more to the +5V power down and simultaneously generates XPDOWN signal to indicate the condition to the MPU 68000 on the CPU board. The circuit enables the MPU to protect memorized data against such power failure.

3.10.4 +5V regulating circuit

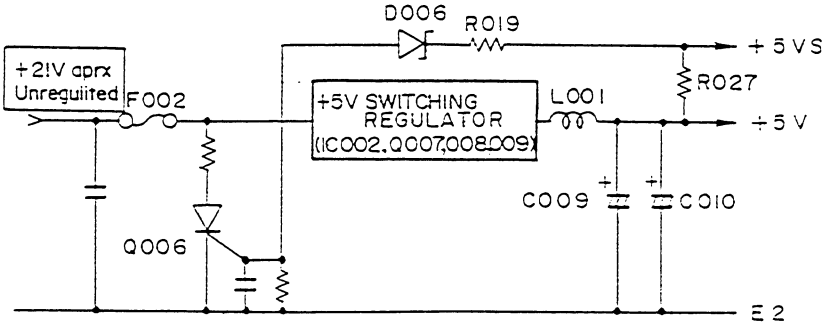
The circuit consists of the rectifier, overvoltage protector, +5V switching regulator with overcurrent protection and LED output indicator.



3.10.4.1 Overcurrent protector

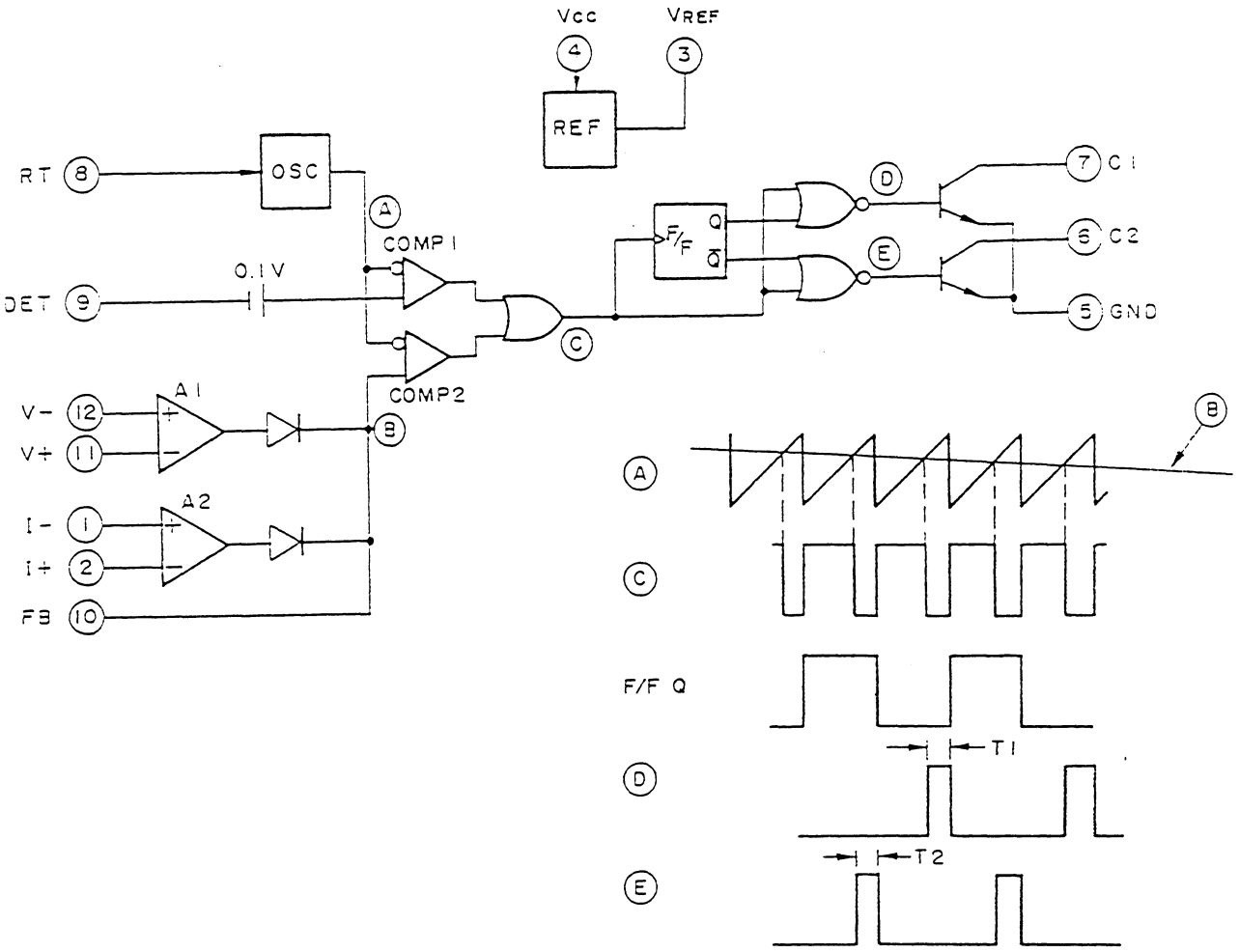
The circuit protects all the parts against overvoltage as follows:

When the +5V power exceeds +6V, the thyristor (Q006) is turned on since a voltage across the zener diolde (D006) is more than +6V of zener voltage. The fuse (F002) opens up since a heavy current is pulled into the Q006 to stop the +5V power supply.



3.10.4.2 +5V switching regulator with overcurrent protection

The circuit generates +5V switching regulated power for the digital circuit with pulse width control. The pulse width control is executed by the controller (IC002), SWC-01. The controller (IC002) is a custom hybrid IC composed of a sawtooth oscillator (OSC), two comparators (COMP1 and COMP2), two amplifiers (A1 and A2), and a +5V reference voltage generator.



The COMP1 controls the maximum pulse width in low level to obtain the dead time. The COMP2 controls the pulse width by comparing the output signal from the A1 and A2 with the sawtooth signal from the OSC.

The A1 functions as a feedback amplifier by feeding back +5V Remote Sense Line (5Vs). The A2 functions as an amplifier with overcurrent protection by feeding back the voltage drop across the resistor (R25).

The switching signal from the SWC-01, C1 and C2 , drives transistors (Q007 and Q008). The output from the emitter of Q008 is converted to +5V regulated power through the L-C filter (L001, C009/010). VR002 is an adjustor to set a current value (threshold level) to start the overcurrent protection. VR003 is an adjustor for the +5V regulated power output.

Section 4

4. Self check program Page

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4.1 General

The following self check programs are provided in this unit.

1) Power-on initial self check

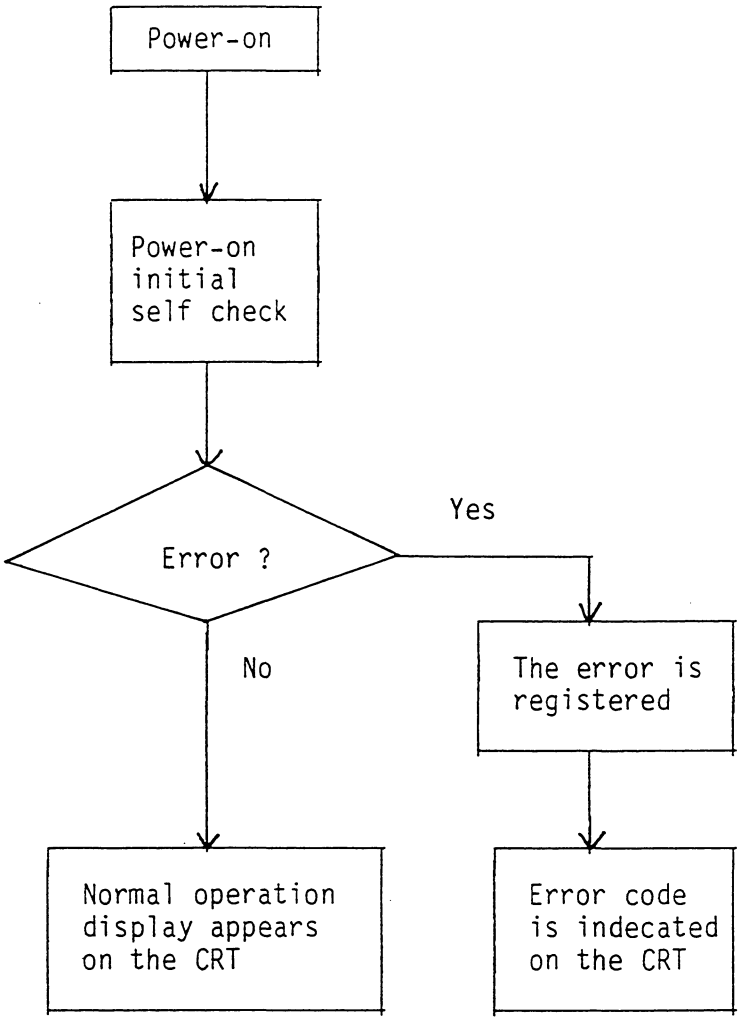
2) Manual self check

Self check program

PCB	Inital self check	Manual self check
CPU board	ROM RAM 8279 71051 EEPROM	ROM RAM 8279 71051 (RS232C) Sound DIP switch/LED/Status Others
CRTC board		Wave RAM Character RAM Graph RAM Wave display Character display Graph display WCG display
AD board	Global memory A/D converter	Global memory A/D converter
REC CNTL board Built-in recorder	72001 (local test) Keyboard	Communication Keyboard Built-in recorder Busy line
WS/IO board	ROM RAM 72001 (local test)	ROM RAM Global memory RS232C Centronix External recorder

4.2 Power-on initial check

This check program is automatically executed whenever the power switch is turned on. If there is a problem, the display changes to DIAGNOSITC CHECK AND SYSTEM SETUP display with the error indication while the error code is registored on ERROR HISTORY.



4.2.1 CPU board

1) ROM check
The ROM check is executed by comparing the value of the acquired sum of data except the value at the last adress with the prestored check sum at the last address. If the values do not coincide, the error code is indicated on the CRT. Refer to ERROR CODE explanation.

2) RAM check
The RAM check is executed by comparing each word after being written the memory area of the RAM with "5555"H to be written as a test pattern. If a word is not "5555"H, the errorr code is indicated on the CRT.

3) 8279 (Programmable keybord/display controller) check
The check is executed by comparing each byte after being written into the memory area of the internal RAM (LED DISPLAY RAM) with "FF"H or "55"H ti be written as a test pattern.

4) 71051 (Programmable communication controller interface) check
Two bits of the status register of 71051, "Tx" and "Rx" are checked.

5) EEPROM, 2816 check
Teh check is executed by means of Cycle Redendancy Check (C.R.C.).

4.5 AD board check

1) Global memory check
The gloal memory check is executed by comparing each word aftr being written into the memory are with "5555"H to be written as a test pattern. In this memory check register inside the MPU on the CPU board is used as the program working area not in the global memory.

2) AD check
A/D conveter output of the reference voltages (±5VREF and OVREF) is checked whether the output data is in the specified ranges or not.

. +5VREF ..... FD0 ± 0AH

. -5VREF ..... 30 ± 0AH

. OVREF ..... 800 ± 0AH

[Descriptions of the check]

a) ROM check
ROM check at power-on is executed by comparing the value of the aquired sum of the data with the prestored check sum. If the values do not coincide, an error code is displayed on the CRT.

b) RAM check

b-1) Checker flag test
"5555"H data is written into all words and read out from the lowerst word to upwards one by one to be compared with the original data. Then "AA55"H data is written into all words and read out from the lowerst word to upwards one by one to be compared with the original data.

b-2) Sequential test
Number 0 through number 255 are writtern into the lower 256 bytes of the RAM area and number 1 through number 254 and number 0 are written into the next 256 bytes. In the same manner, all memory area is written wi the numbers by increasing the numbers one by one. After writing the data into all area, all bytes are read out from the lowest bytes to upwards one by one to be compared witht he original data.

c) Print RAM check
Print RAM area is checked in the same manner as the above b) RAM check.

d) 71054 check
A count number is set to the 71054 count register and count operation is started. By reading the current count number by the count latch command, 71054 is checked whether the counter is counting down correctly.

4.2.3 REC CNTL board

1) uPD72001 check
Inside the uPD72001 at local self test mode, data "55"H, "AA"H, "FF"H and "00"H are transmitted and received between the two ports to compare the data before transmitting and after receiving.

2) Global memory check
Test pattern "5555"H is written into tthe memory area and then read out to be compared with the original data. In this memory check, register inside the MPU of the CPU board is used as the program working area not in the global memory.

3) Communication check
Communication beteen the Master CPU (68000) on the Sub CPU (8085) on the REC CNTL board is made through the global memory. Communication errors include Response Time Out Error and Line Test Error.

4) Recorder check
Built-in recorder is controlled by the MPU (8085) on the REC CNTL board. Check result is sent to the MPU on the CPU board through the global memory.

Check items are as follows:

a) ROM check
b) RAM check
c) Print RAM check
d) 71054 (programmable timer counter) check

5) A/D check
A/D conveter output of the reference voltages (+5VREF and 0VREF) is checked whether it is in the specified range.

+5VREF ..... OFF -3H

0VREF ..... 0 +3H

4.2.4 WS/IO board check

1) RAM check
Test pattern "5555"H is written into the memory area and then read out to be compared with the original data. In this memory check, register inside the MPU of the CPU board is used as the program working area not in the RAM.

2) uPD72001 check
Inside the uPD72001 at local self test mode, data "55"H, "AA"H, "FF"H and "00"H are transmitted and received between the two ports to compare the data before transmitting and after receiving.

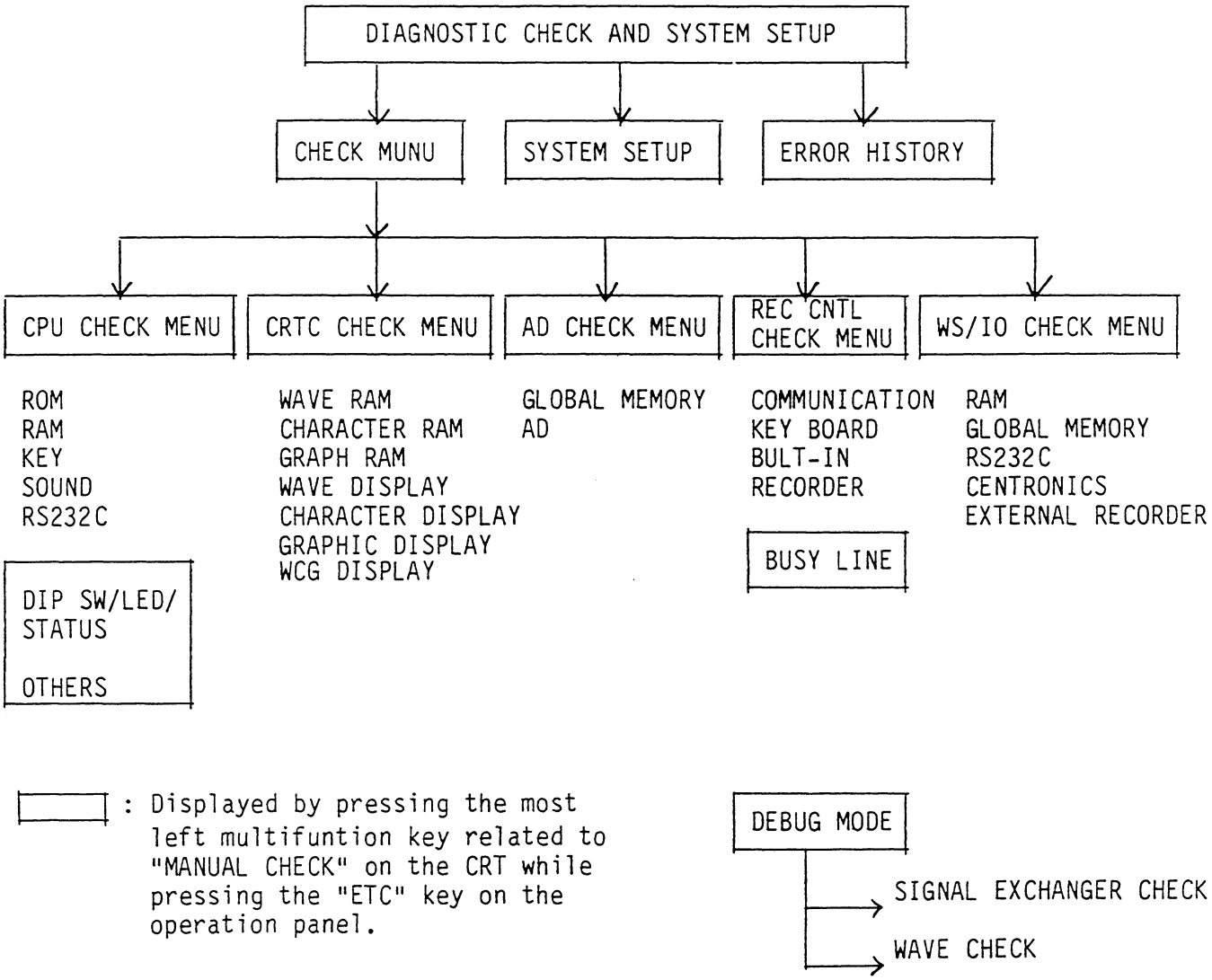
4.3 Manual check

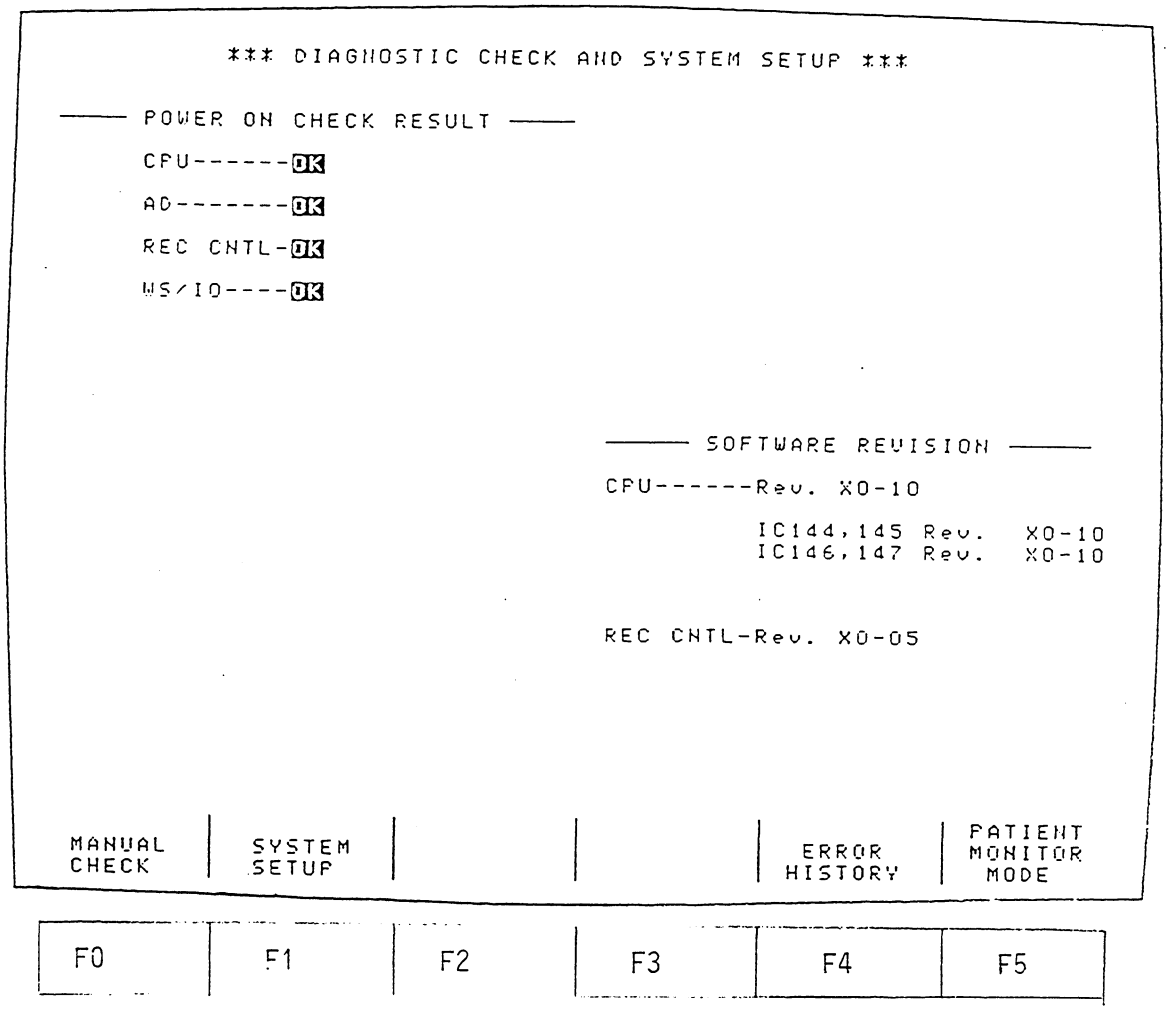
There are two methods in manual check.

. Manual check ..... Called up by pressing the SELF CHECK key on the front panel for longer than three seconds.

. Debug mode ..... Called up by pressing the ALARM LMITS key and ALL BEDS key simultaneously.

Program hierarchy structure

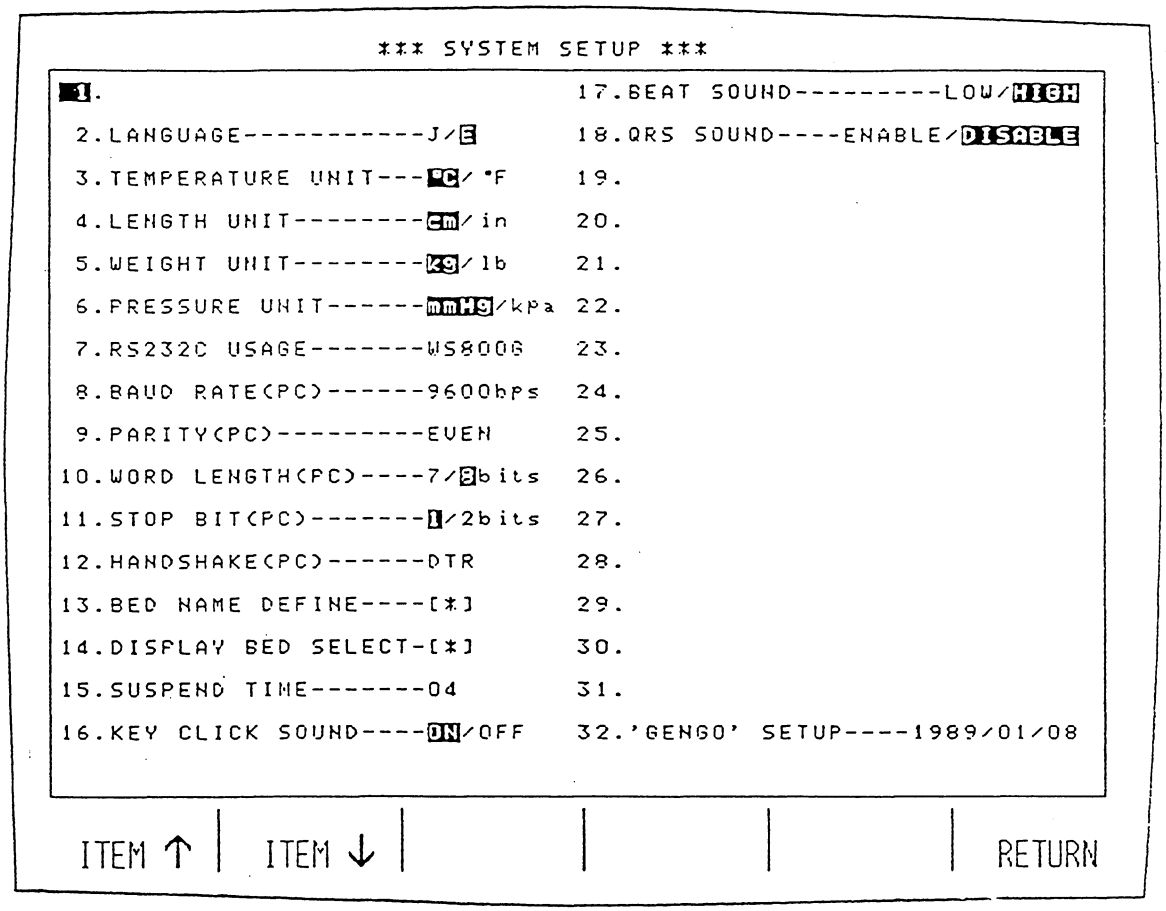




Above screen is called up by pressing the SELF CHECK key on the front panel for longer than three seconds.

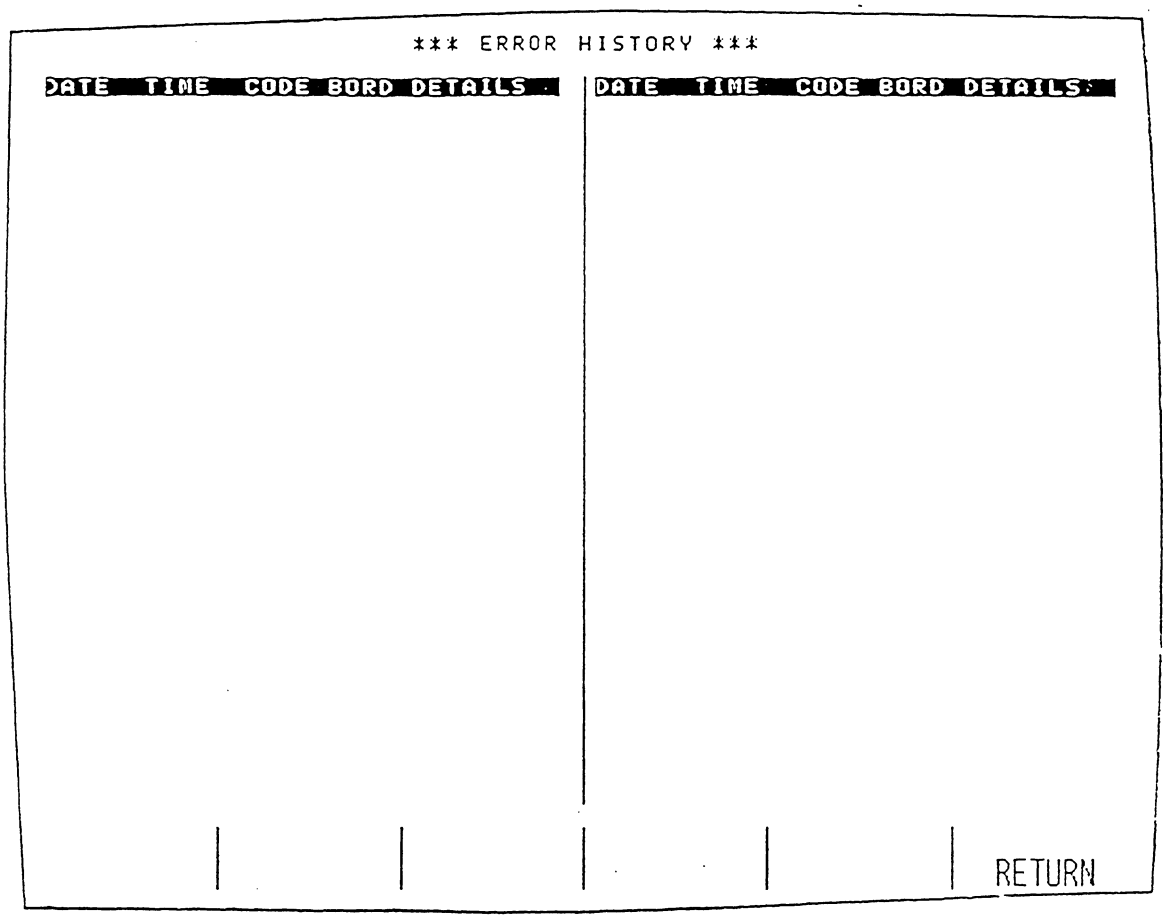
Power-on check results and sofrware version numbers are dipalyed.
Multifunction keys (F0- F5) are used to call up each menu for the test.

4.3.1 System setup



Called up by pressing the F1 key (SYSTEM SETUP) on the DIAGNOSTIC AND SYSTEM SETUP screen. ITEM UP/DOWN keys select the items.

4.3.2 Error history



Called up by pressing the F4 key (ERROR HISTORY) on the DIAGNOSTIC AND SYSTEM SETUP screen.

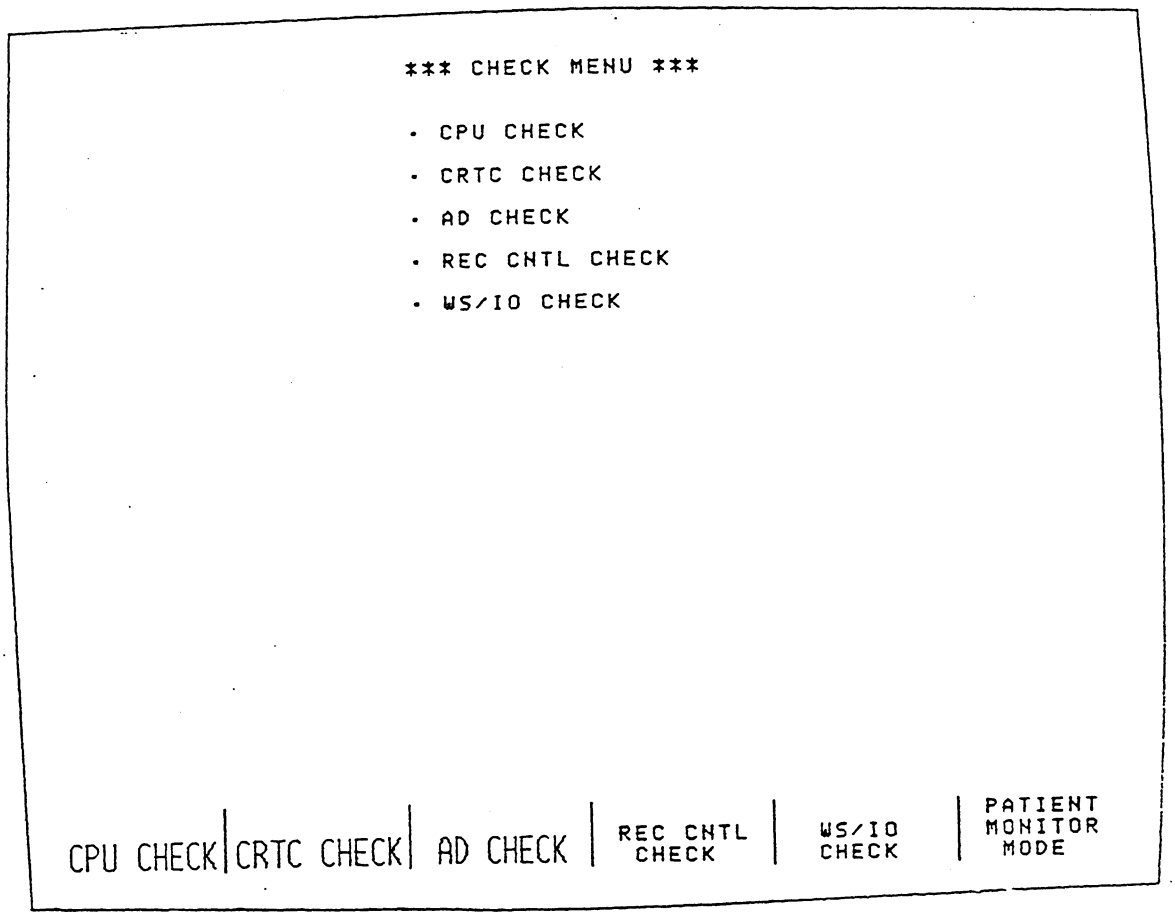
Error history includes

TIME: Time of error detection
CODE: Error code
BOARD: PC board related to the error
DETAILS: details of the error

4.3.3 Patinet monitoring mode

The DIAGNOSTIC AND SYSTEM SETUP screen returns to the normal patinet monitoring mode by pressing the F5 key (PATIENT MONITORING MODE).

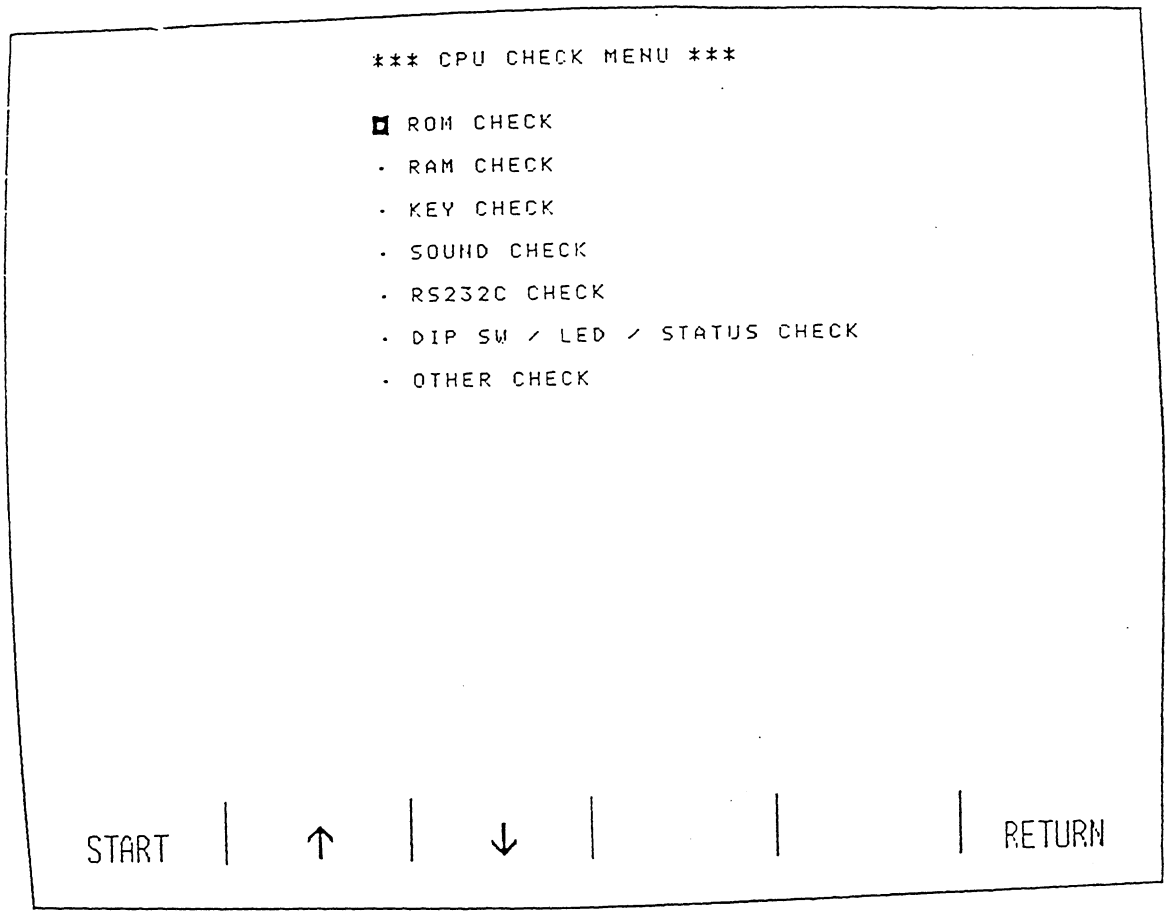
4.3.4 Check menu



Called up by pressing the F0 key (MANUAL CHECK) on the DISGNOSTIC AND SYSTEM SETUP screen.

Multifunction keys call up the check screens of each board.

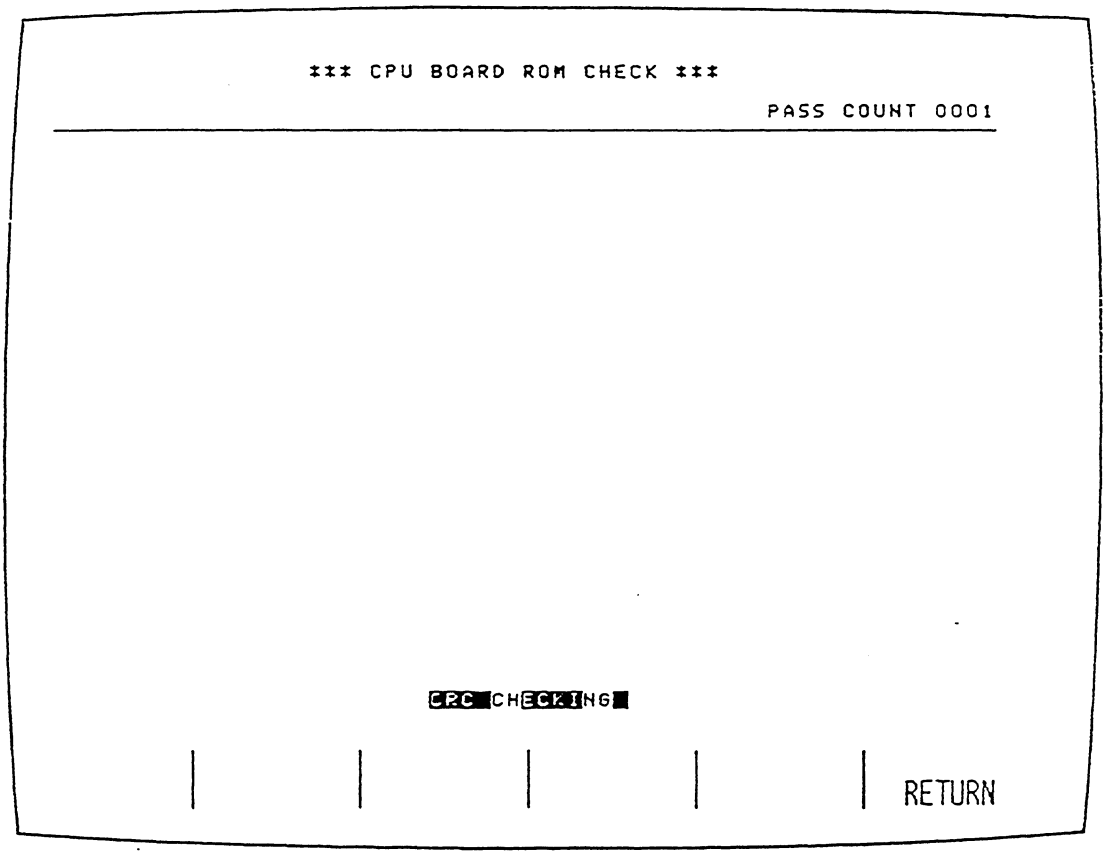
4.3.4.1 CPU check



UP/DOWN keys select the items, START key exucutes the check program, and RETURN key returns the screen to the previously displayed screen mode.

4.3.4.1.1 ROM check

When ROM CHECK is selected, the display changes to the following display.



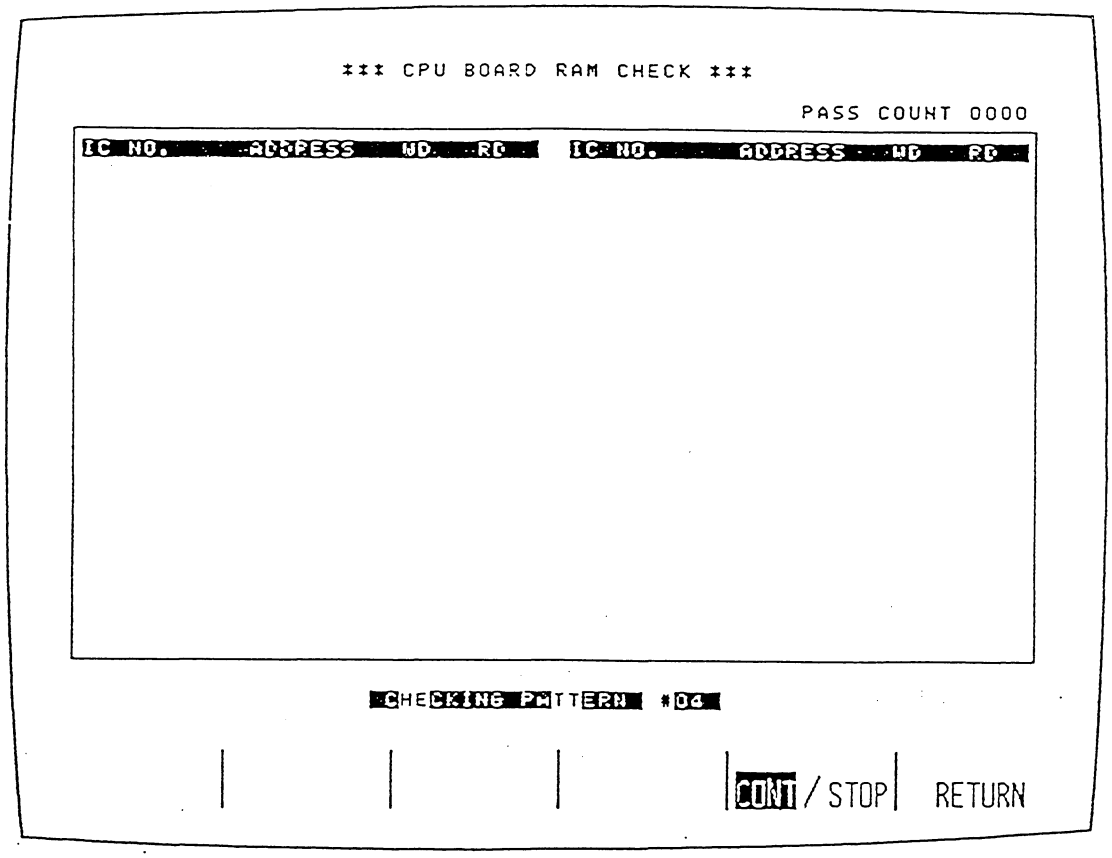
"CRC CHECKING" message is blinking while the check is executred with Cyclic Redundancy Check (C.R.C.). Whenever one cycle of the check is completed without an error, "PASS COUNT" increases by one. If there is an eror, the error message appears on the display, as in the following example.

ERROR !! (IC No. 144, 146, 148)

The check is stopped by pressing the RETURN key (F5) and the display returns to the CPU CHECK MENU.

4.3.4.1.2 RAM check

When RAM CHECK is selected, the display changes to the following display.



The check is executed by comparing each data after writing one of the following check patterns (No.1 to No.15)

No.	Pattern
1	Decrement (byte)
2	55H (byte)
3	0FH (byte)
4	Alternating 00H and FFH
5	Upper byte: 00H, Lower byte: FFH
6	AAH (byte)
7	F0H (byte)
8	Alternating FFH and ooH

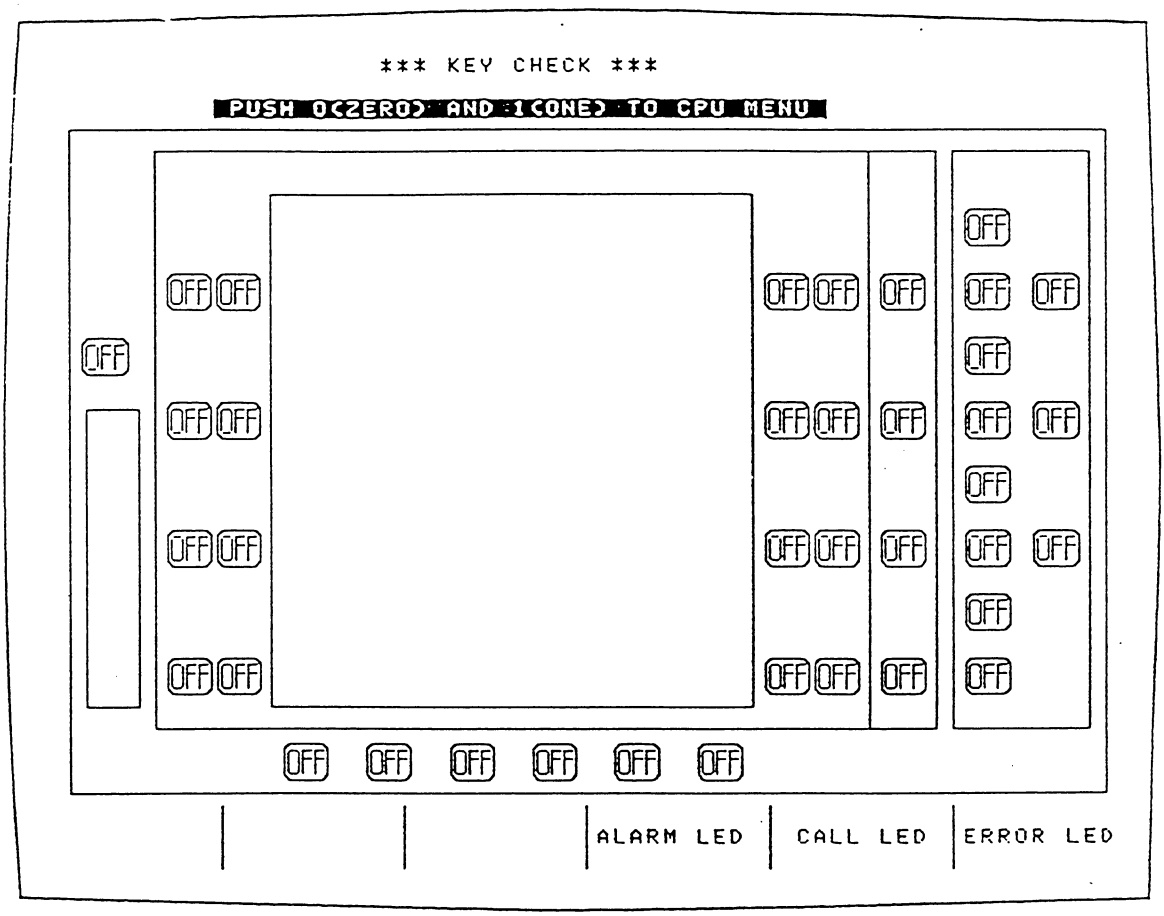
No.	Pattern
9	Upper byte: FFH, Lower byte: 00H
10	00H (byte)
11	Bit shift (word)
12	5555H (word)
13	AAAAH (word)
14	FFFFH (word)
15	0000H (word)

Whenever one cycle of the check patterns (No.1- No.15) is completed without an error, "PASS COUNT" increses by one. If there is an error, the error massage appears on the dispaly as on the following example.

IC NO.	ADDRESS	WD	RD	(WD: Data to be written)
IC152, 153	08A00	5555	FFFF	(RD: Data to be read)

The check is continued until the CONT/STOP modfe on the display is set to STOP by pressing the F4 key (CONT/STOP).

4.3.4.1.3 Key check

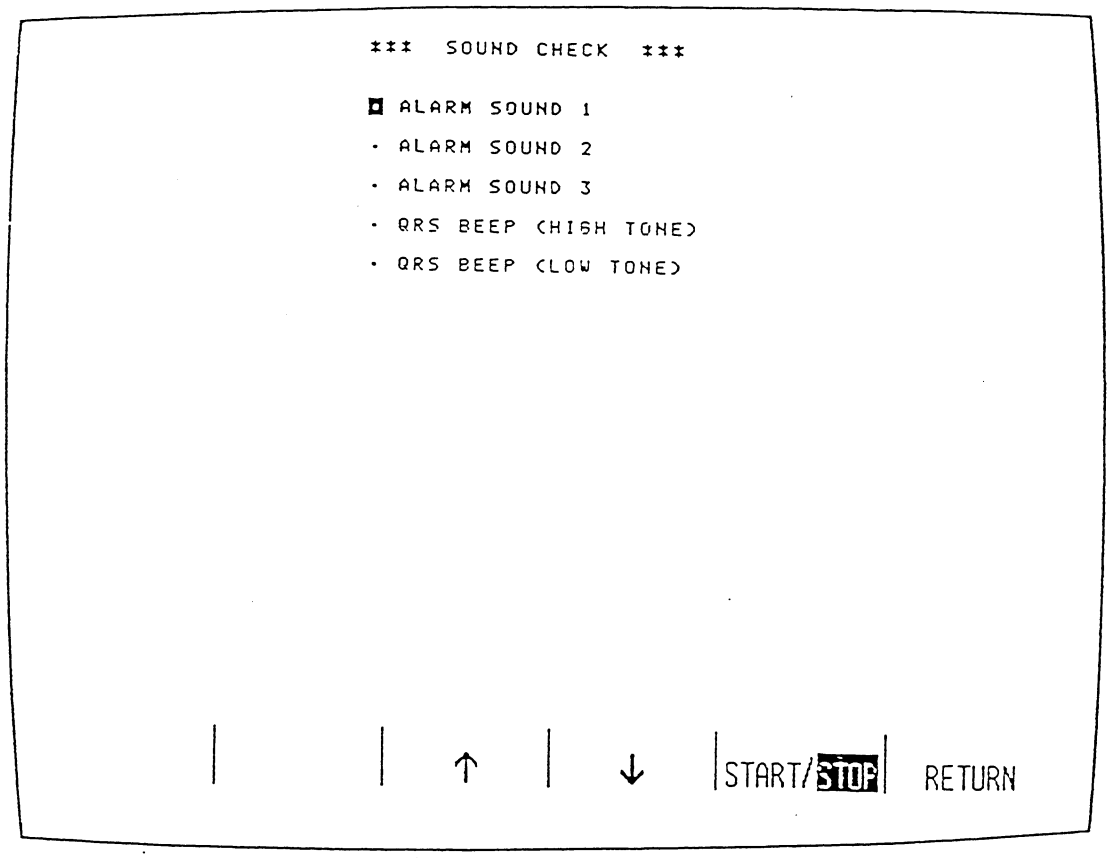


Displays the keys of the central montior main unit on the corresponding positions on the front panel.

When a key is pressed, its corresponding key OFF incdication changes to ON and LED lamp lights up if the key provides a lamp. Individual bed's alarm LED lamp lights up by pressing its patient select key and record key simultaneously.

Pressing the F0 and F2 key simultaneously returns the screen to the CPU CHECK MENU mode screen.

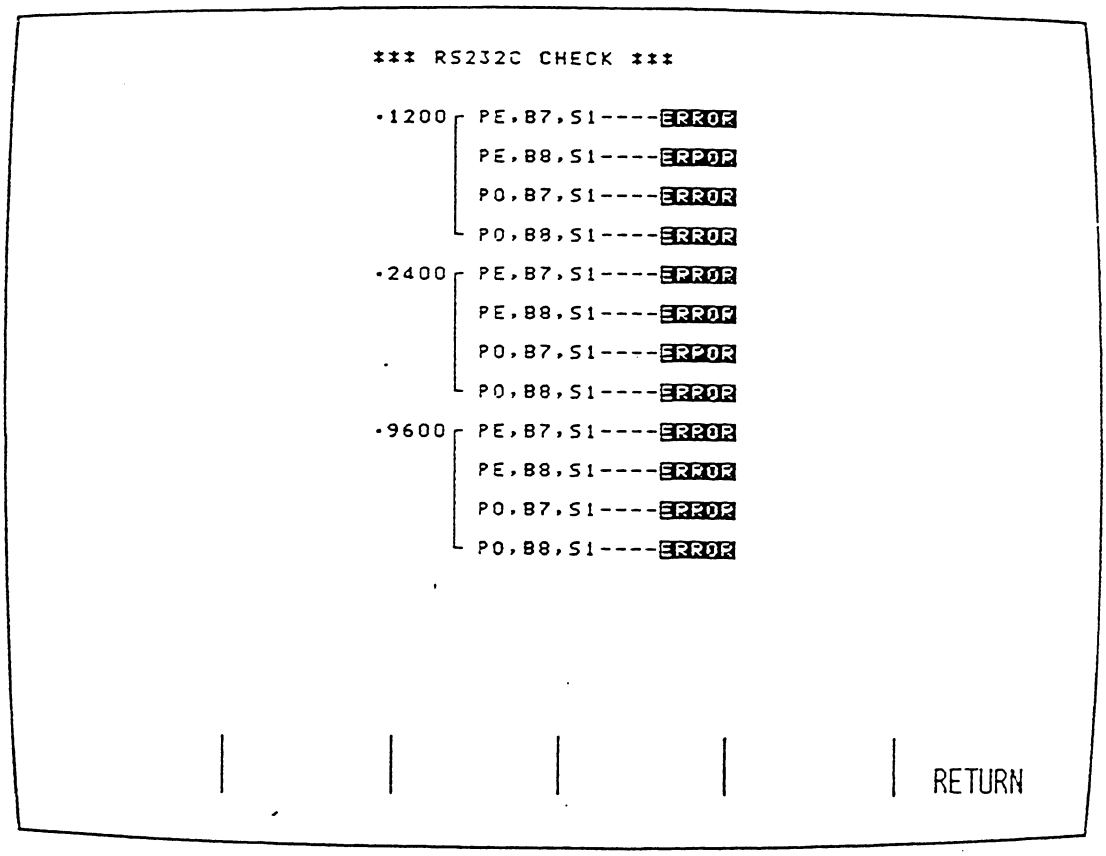
4.3.4.1.4 Sound check



Each sound is generated by setting the START/STOP key (F0) mode to START after selecting one of five check sounds ont eh display by pressing the | (F2) or | (F3) key.

Sound menu	Tone
Alarm sound 1	Ring (patient alarm)
Alarm sound 2	Ding dong (system alarm)
Alarm sound 3	Ding
QRS beep (high tone)	High toned beep
QRS beep (low tone)	Low toned beep

4.3.4.1.5 RS232C check



When the MU-820R is not connected with an external equipment which provides RS232C communication or when the following modification is not done to the receptacle of RS232C, the RS232C CHECK display appears with all the error indications on the CRT as in the above display.

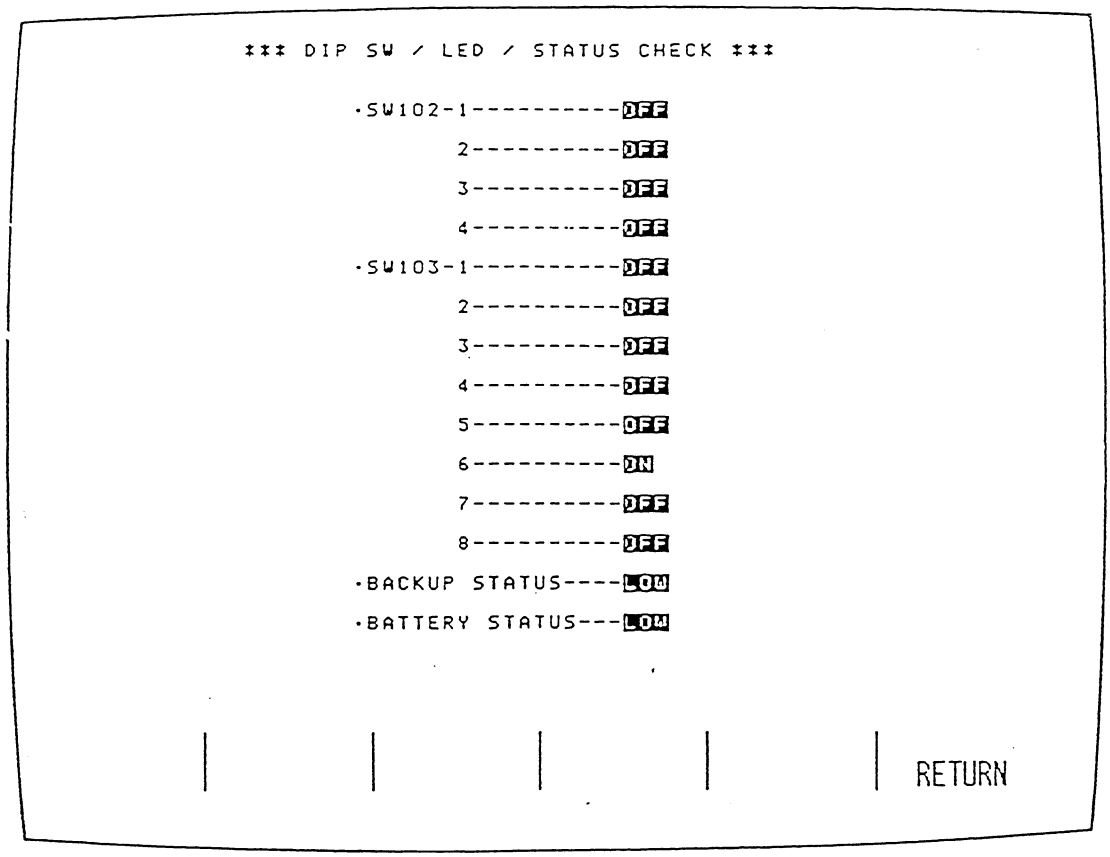
[Modification]

Pin-2 and pin-3: short
Pin-4 and pin-5: short
Pin-6 and pin-20: short

1200, 2400, 9600: Baud rate (bit/sec.)
PE: Paper empty
PO: Odd parity
B7: 7 bits data
B8: 8 bits data
S1: 1 stop bit

The following section (4.3.4.1.6 and 4.3.4.1.7) is displayed by pressing the "ETC" and "F0" keys simultaneously on the DIAGNOSTIC CHECK AND SYSTEM SETUP display. These sections are for your reference since these check programs are for product inspection at the factory.

4.3.4.1.6 DIP SW/LED/STATUS check



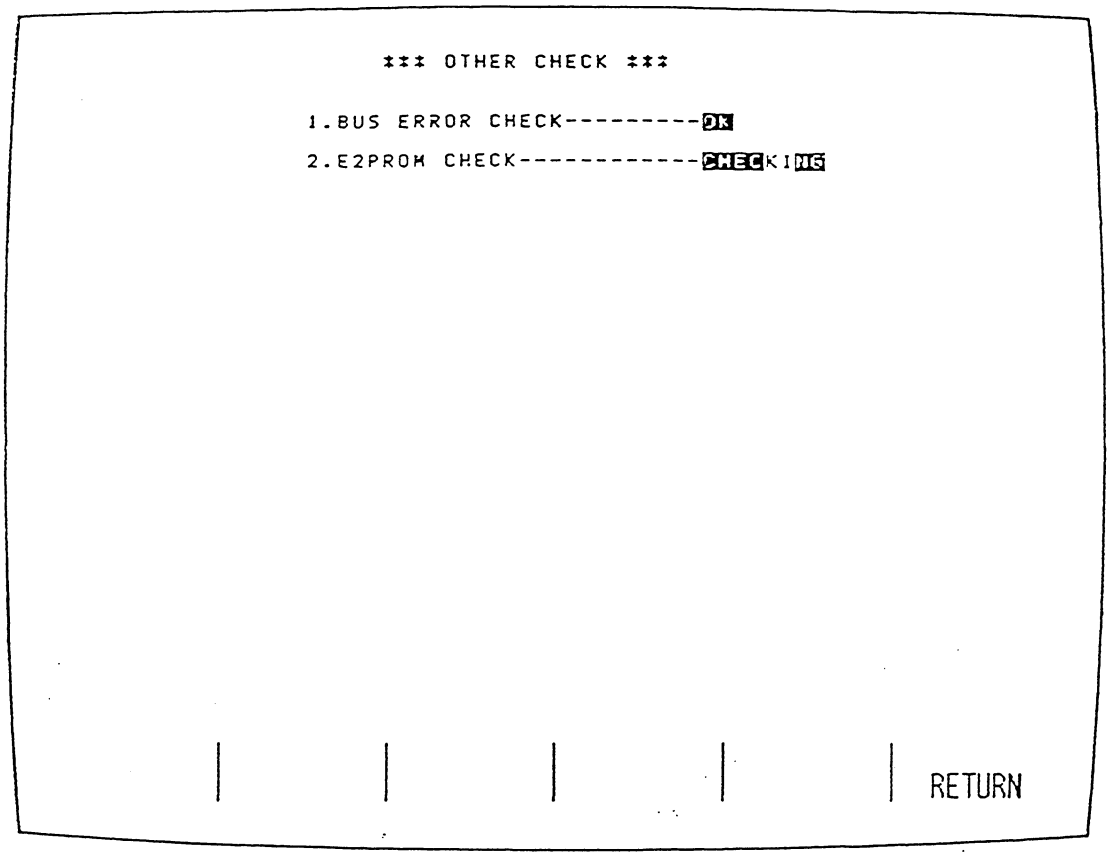
1) DIP switch check
The set condition on the DIP switch on the CPU board SW102 and SW103 appears on the screen.

2) LED check
Each LED (8 bits) on the CPU board sequentially lights and goes out one after another.

3) STATUS check
BACHUP STATUS and BATTERY STATUS appear on the CRT as follows:

BACKUP STATUS	BATTERY STATUS
Low: Normal condition	Low: Normal condition
High: Super-capacitor must be charged	High: Lithium battery must be replaced

4.3.4.1.7 Other checks

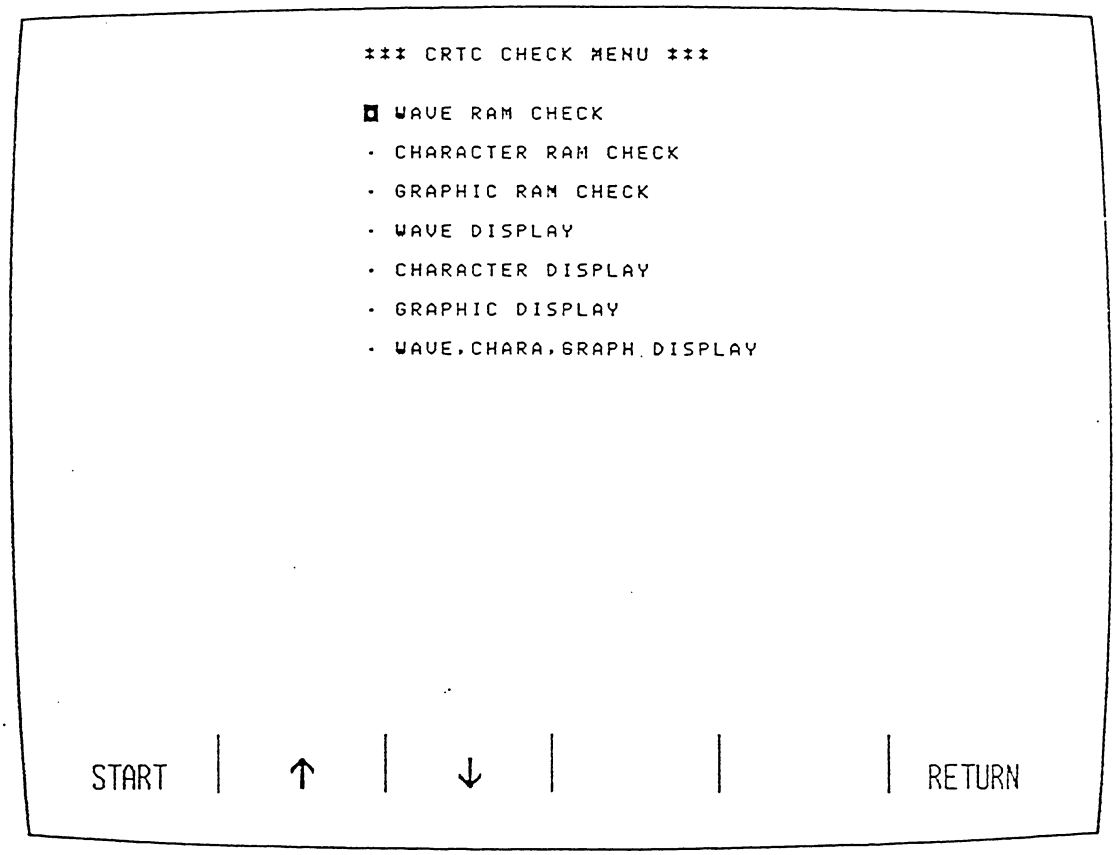


1) BUS ERROR check
The check is executed by accessing an address at which memory area does not exist. A detection of a bus error signal is confirmed by indicating "OK".

2) EEPROM check
The check is executed by comparing each byte after being written into the EEPROM with check byte "55"H to be written. All data of EEPROM are stacked before "55"H is written.

4.3.4.2 CRTC (CRT Control board) check

When CRTC CHECK is selected by pressing the F1 key on the CHECK MENU display, the following CRTC CHECK MENU appears on the CRT.



On the above display,

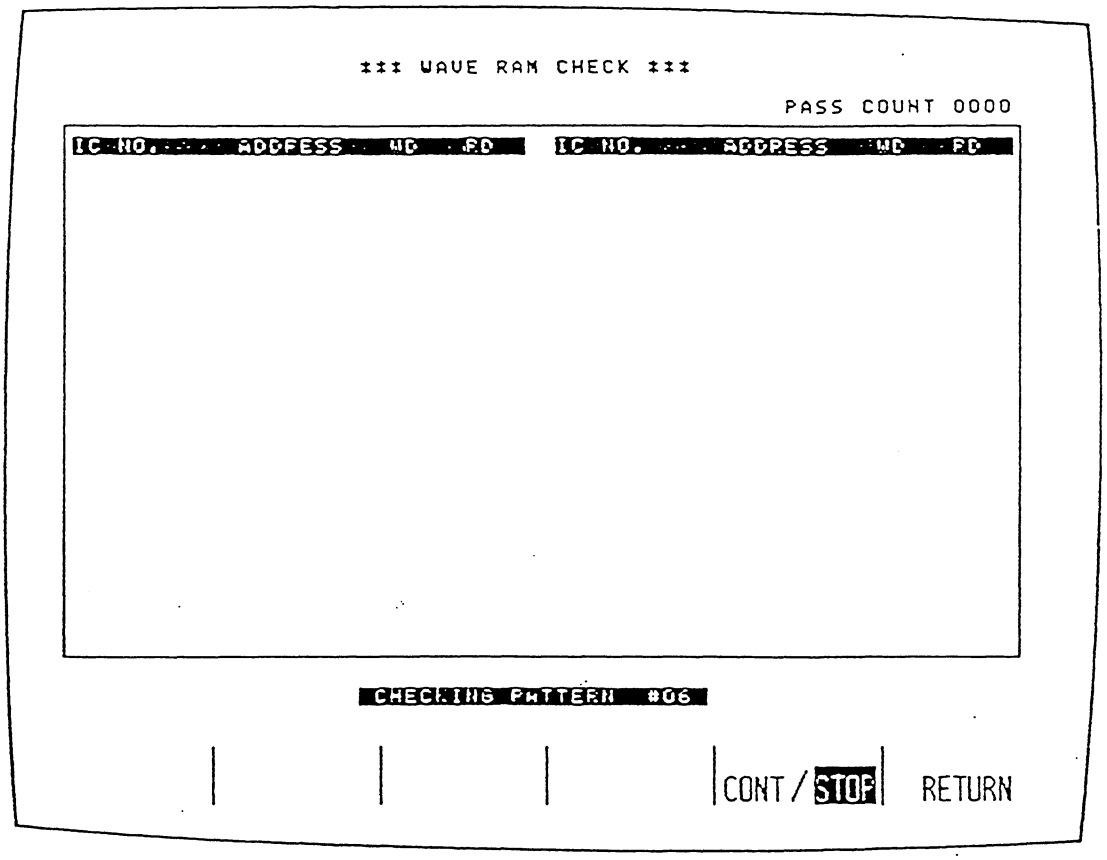
↑ ↓ : to select a check item from the check items on the CRT

START: to execute the program for selected check item while changing to the display for the check item.

RETURN: to return to the CHECK MENU display.

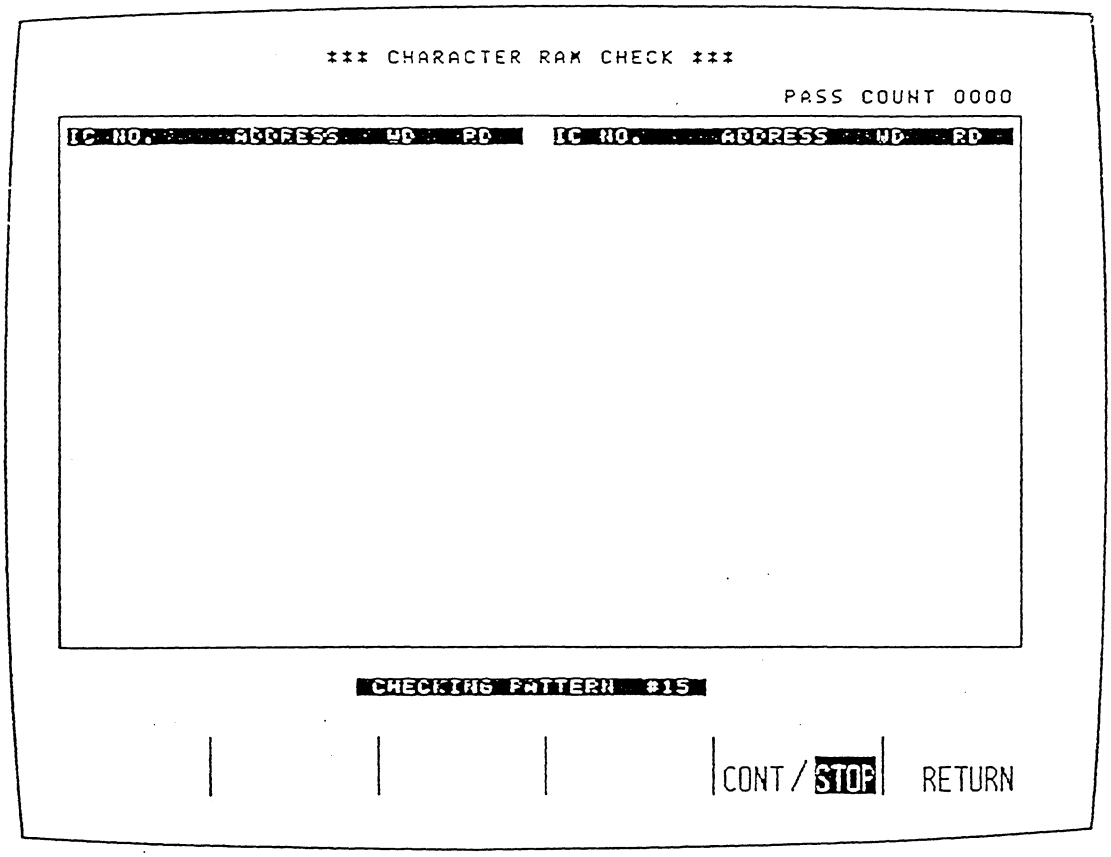
4.3.4.2.1 WAVE RAM check

Patterns No.1 to No.10 of Table-1 are used as the check pattern. The check is the same as the RAM CHECK on the CPU board.



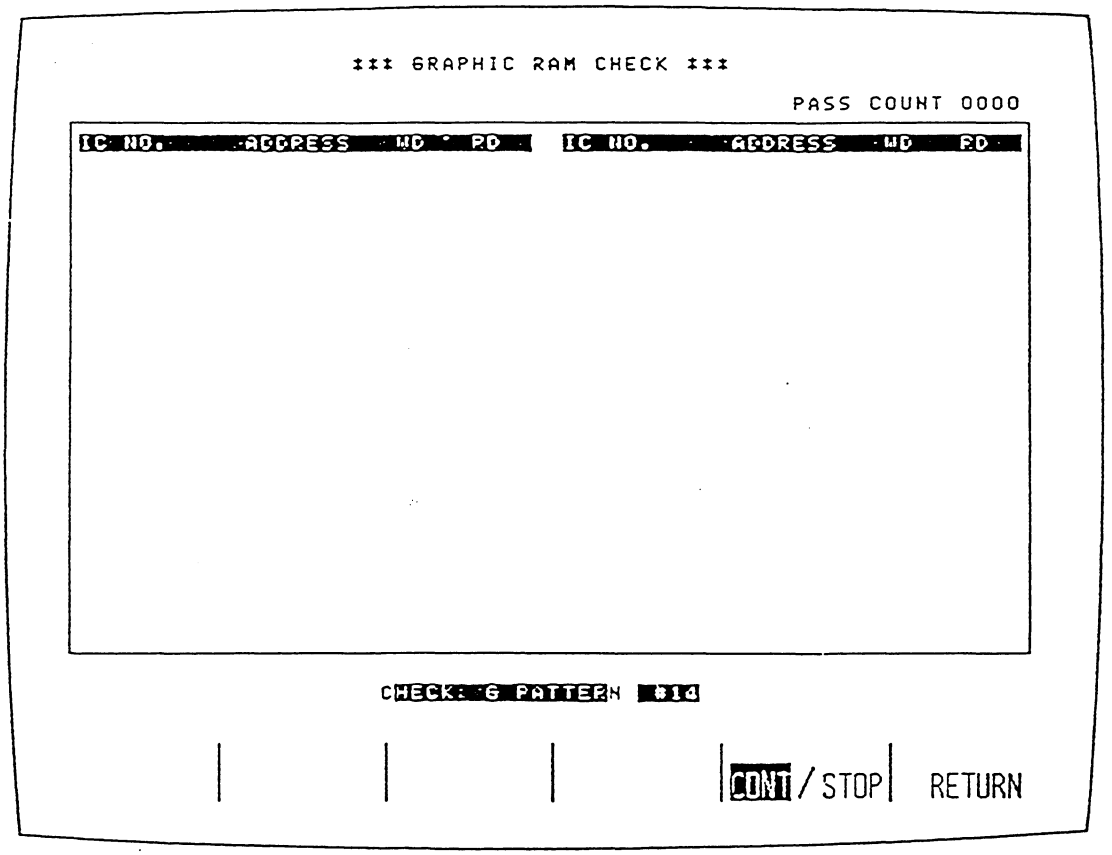
4.3.4.2.2 CCHARACTER RAM check

Pattern No.12 to No.15 of Table-1 are used as the check pattern. The check is same as the RAM CHECK on the CPU board.



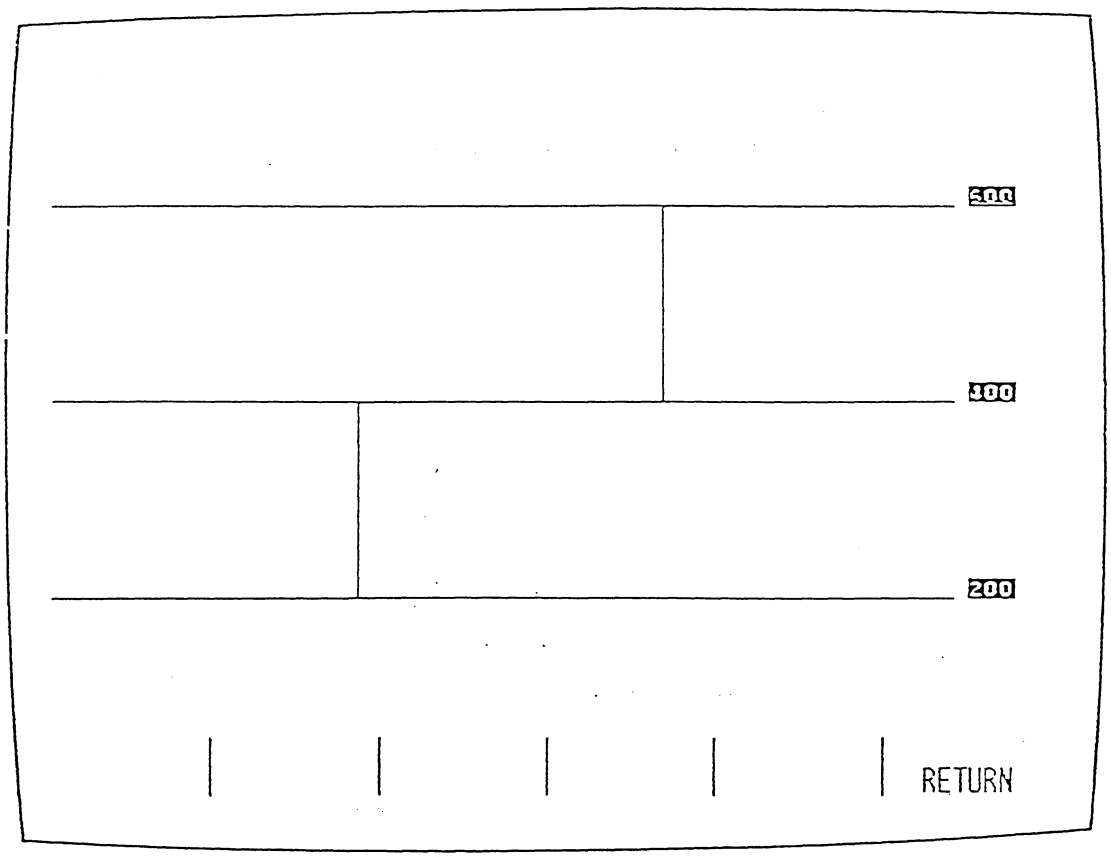
4.3.4.2.3 GRAPHIC RAM check

The check is same as the section 4.3.4.2.2.



4.3.4.2.4 WAVE, CHARA, GRAPH DISPLAY check

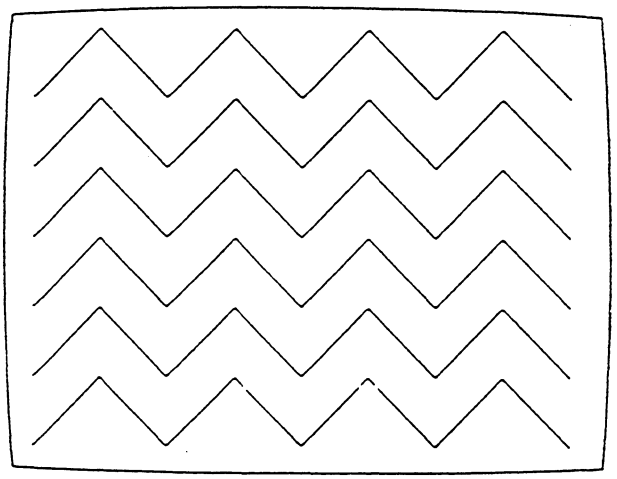
The following composite display with Waveform, Character and Graph appears on the CRT.



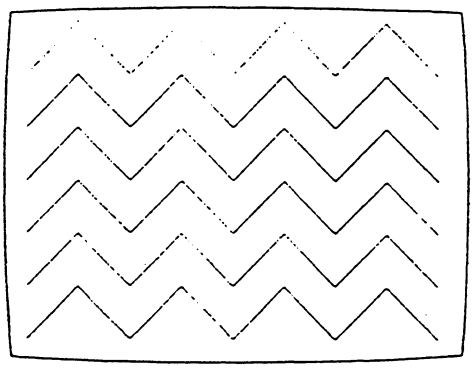
F5 key: By pressing the F5 key (RETURN), the display returns to the CRTC CHECK MENU.

4.3.4.2.4 WAVE DISPLAY check

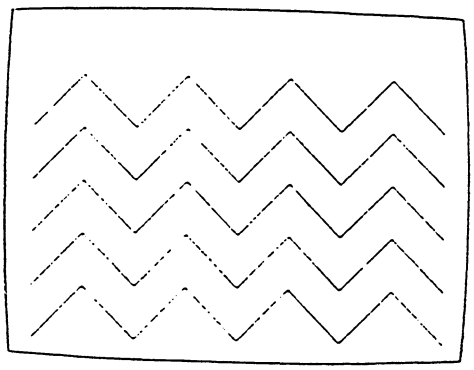
6 traces of sawtooth waveform appear on the CRT. The multifunction keys (F0-F5) provide the following function.



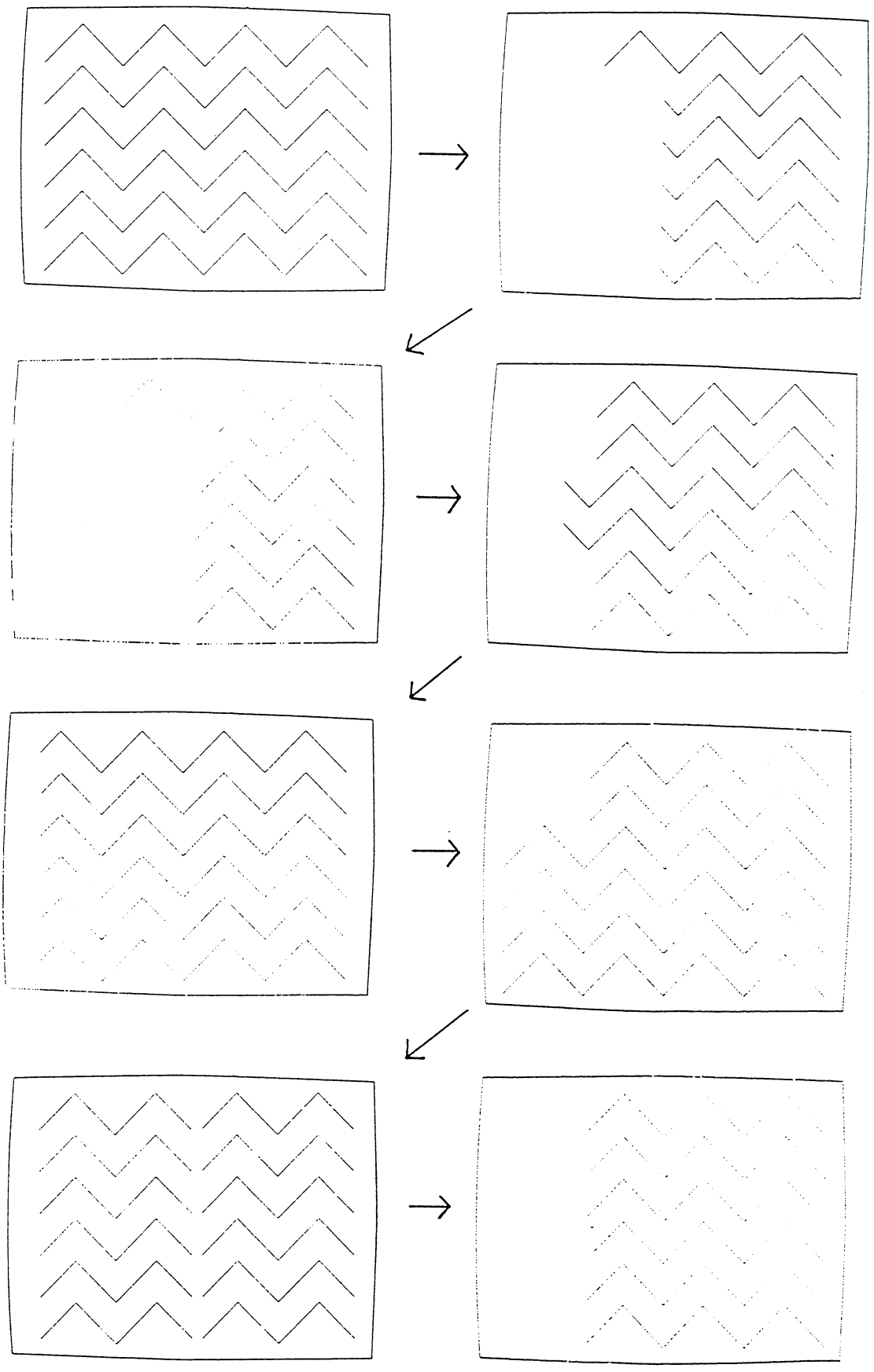
F0: By pressing the F0 key repeatedly, one trace with low intensity is shifted from top to bottom on the CRT.



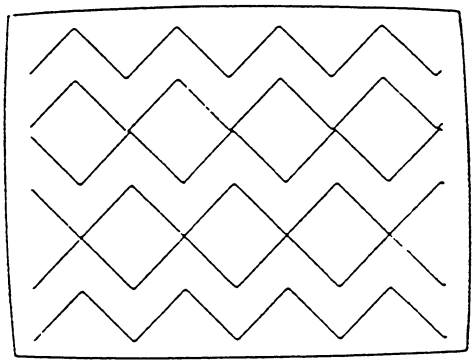
F1: By pressing the F1 key repeatedly, one trace with no intensity is shifted from top to bottom on the CRT.



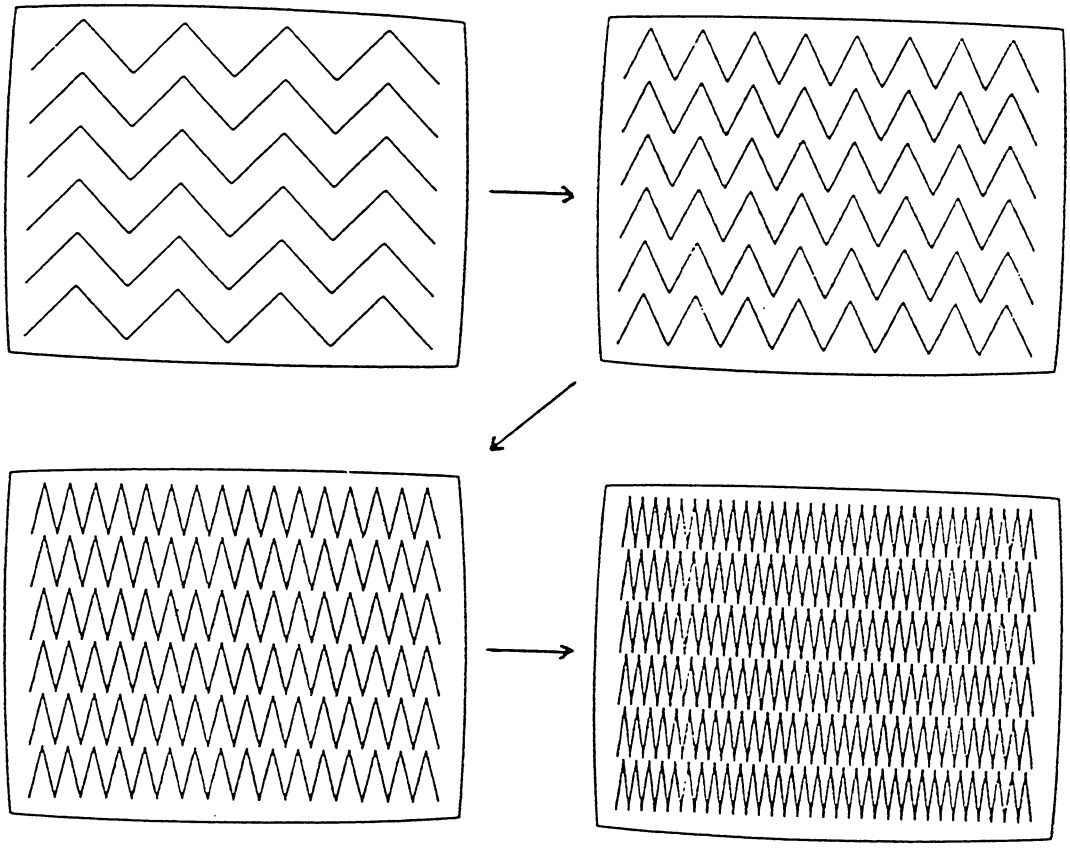
F2: By pressing the F2 key repeatedly, a blank area of the WAVE DISPLAY is shifted as follows:



F3: By pressing the F3 key repeatedly, 2 traces scrolled leftward are shifted two by two from top to bottom on the CRT.



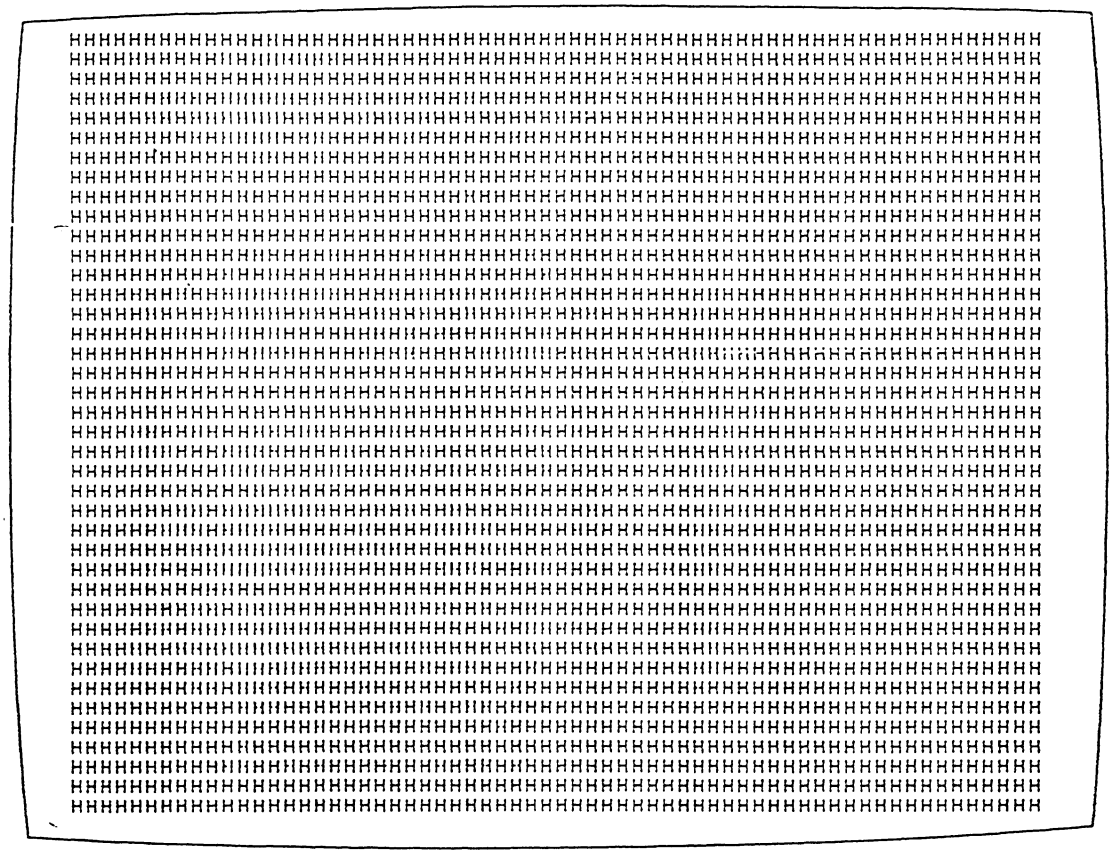
F4: By pressing the F4 key repeatedly, all the traces come to be horizontally compressed as follows:



F5: By pressing the F5 key, the display returns to the CRTC CHECK MENU.

4.3.2.5 CHARACTER DISPLAY check

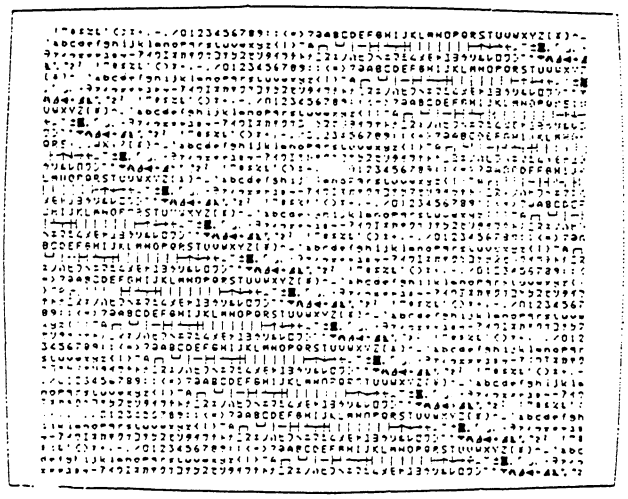
The following CHARACTER DISPLAY appears on the CRT.

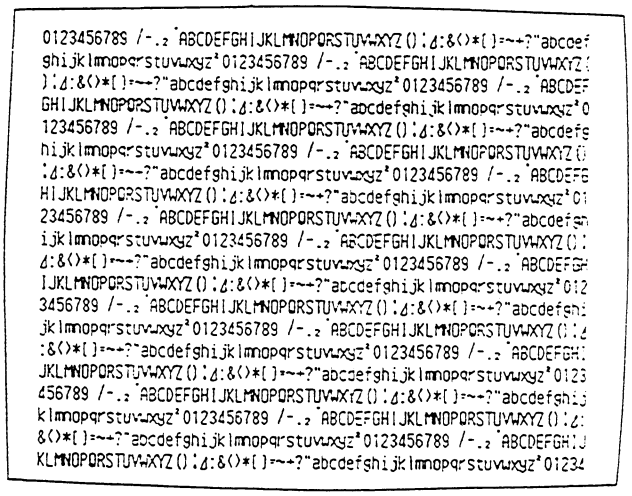


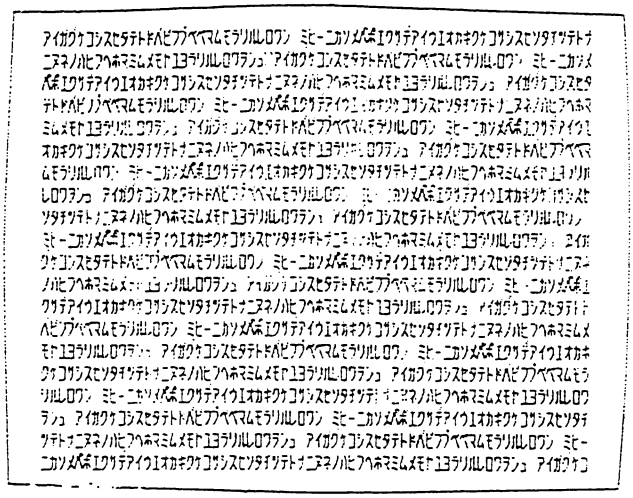
F0: By pressing the F0 key repeatedly, the display mode changes as follows:

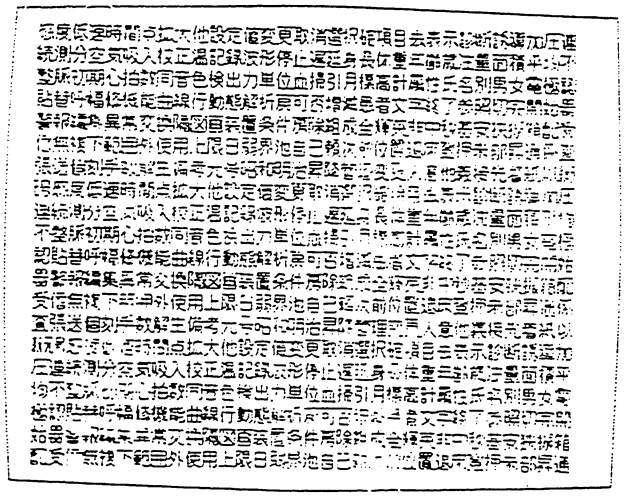
1) Reversed light
2) Blink
3) Reversed blink
4) Low intensity
5) Revesed light with low intensity
6) Blink with low intensity
7) Reversed blink with low intensity

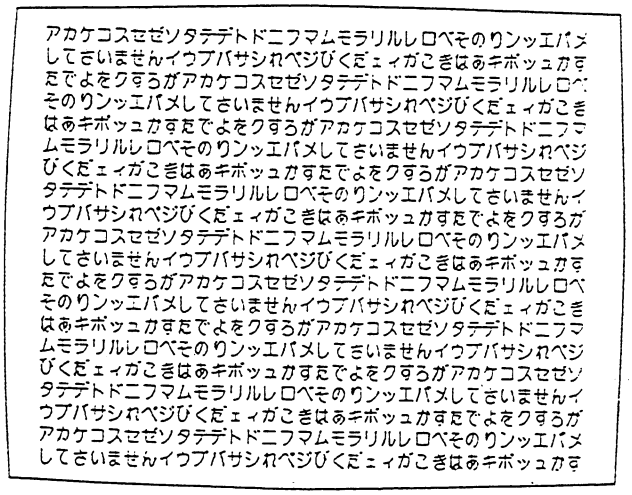
F1: By pressing the F1 key repeatedly, the character pattern changes as follows:

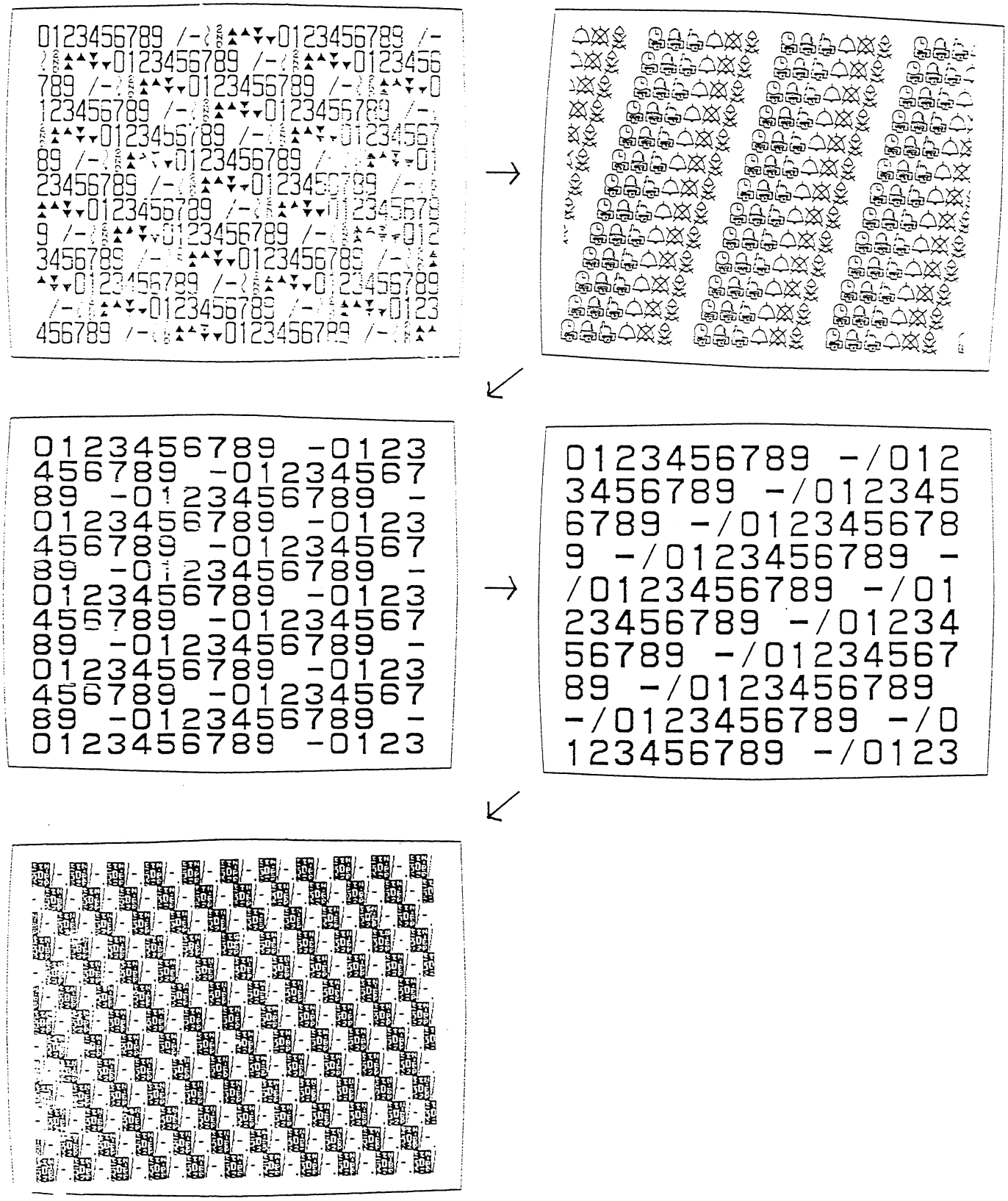










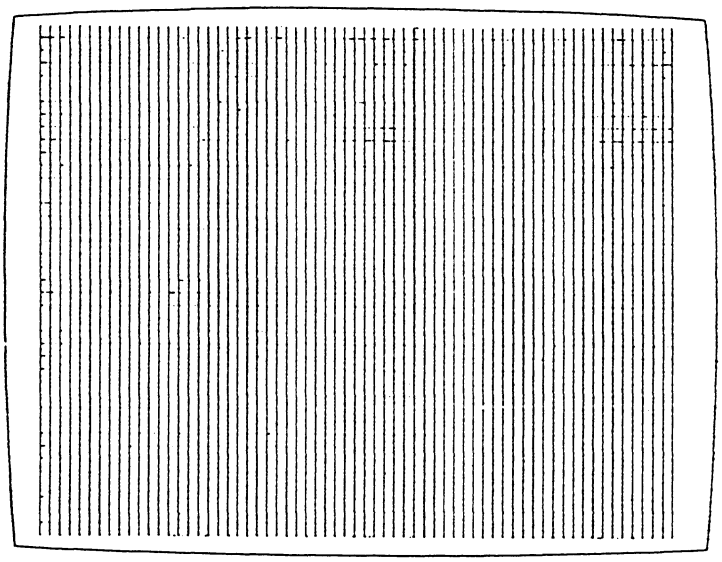


F2: By pressing the F2 key repeatedly, the display is changed to the lowest intensity mode or the normal intensity mode alternatively.

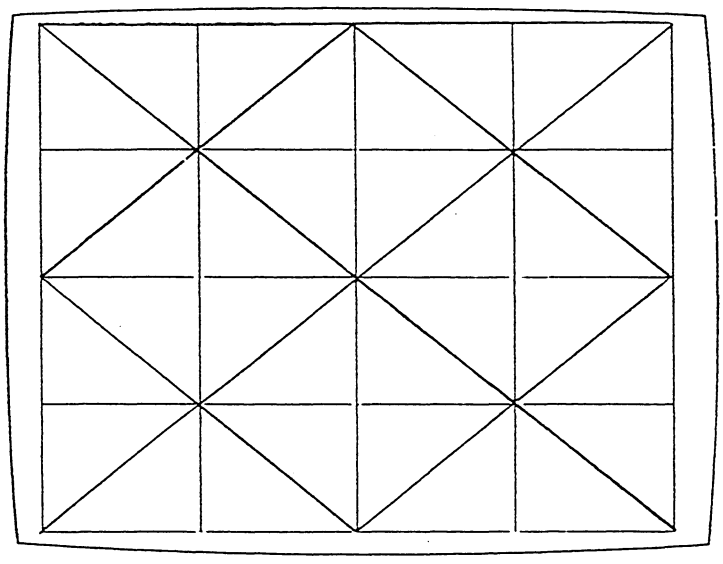
F3: By pressing the F5 key, the display returns to the CRTC CHECK MENU.

4.3.4.2.6 GRAPHIC DISPLAY check

The following graphic dispaly appears on the CRT.

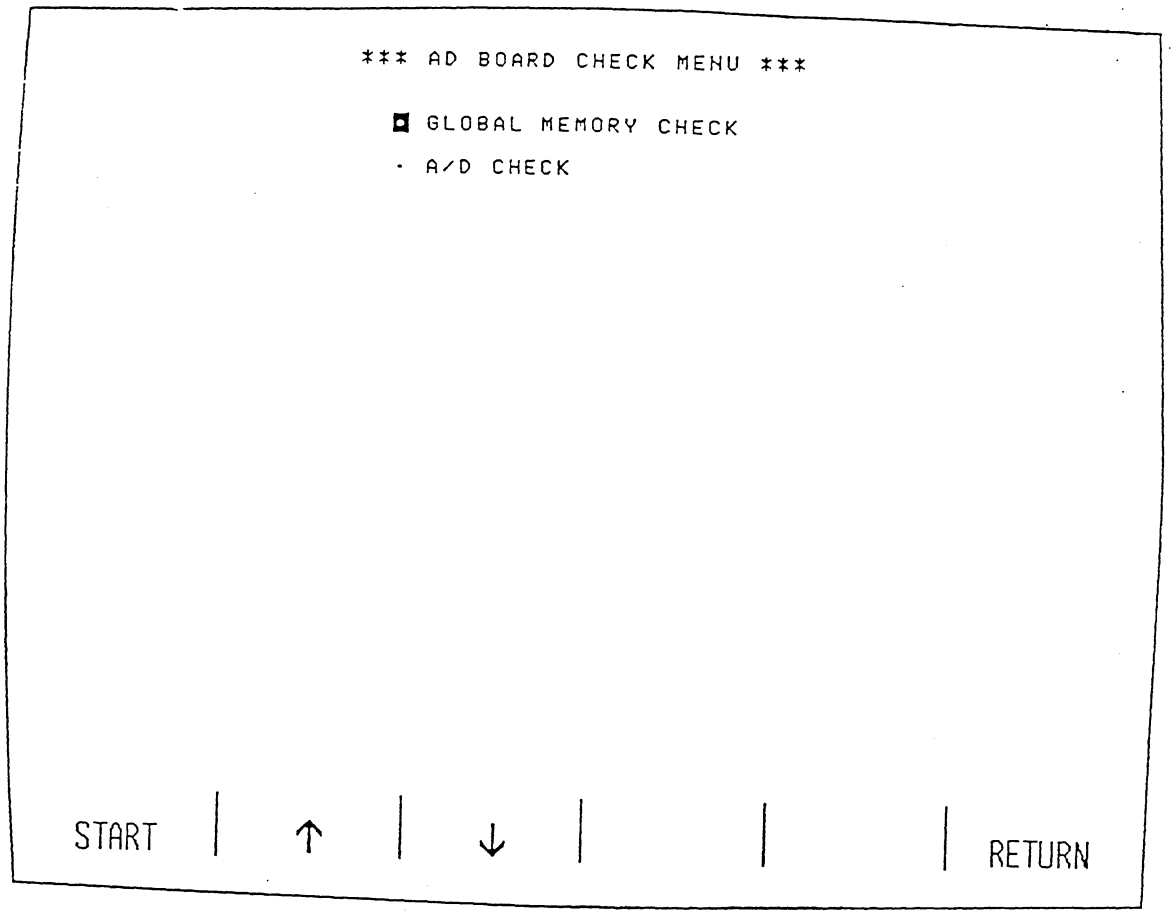


F0: By pressing the F0 key, the display changes as follows:



F5: By pressing the F5 key, the dispaly returns to the CRTC CHECK MENU.

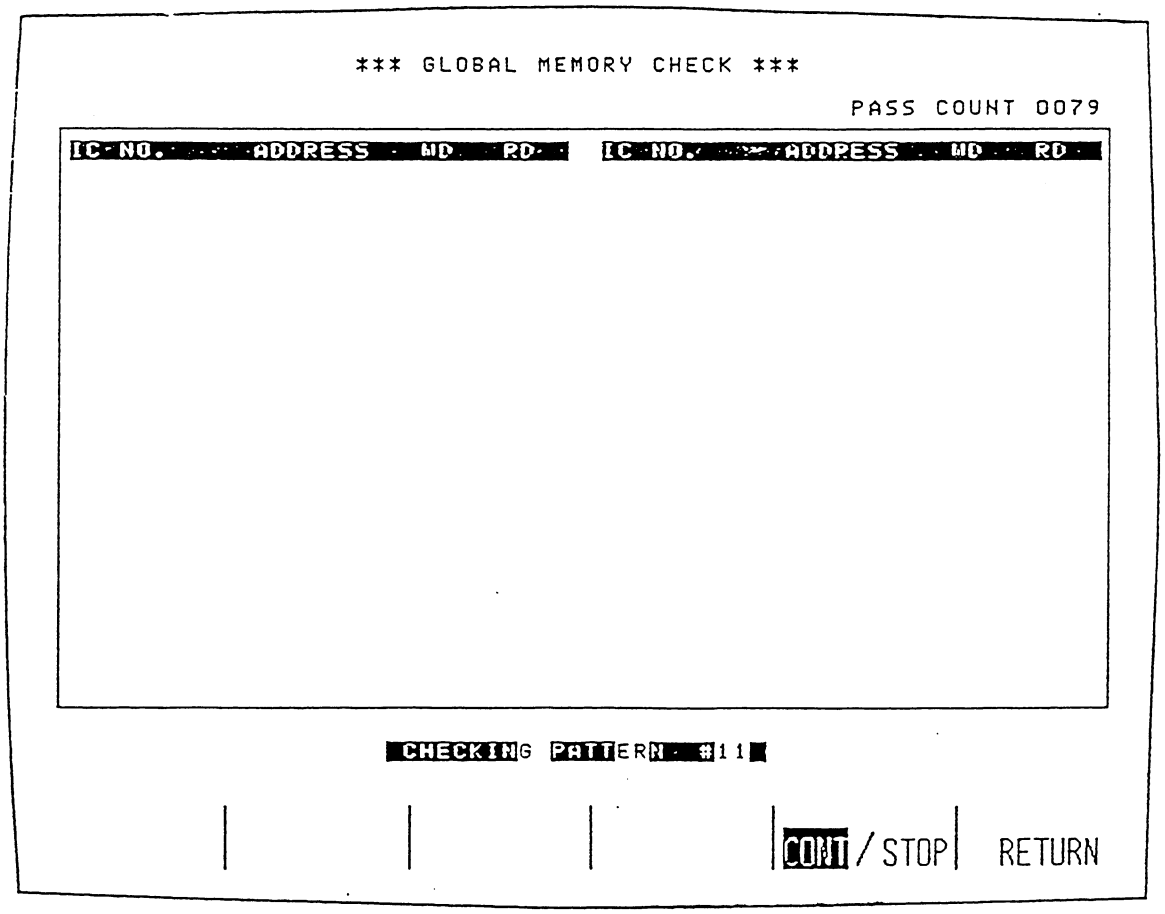
4.3.4.3 AD board check



↑ ↓ : to select the item for the check

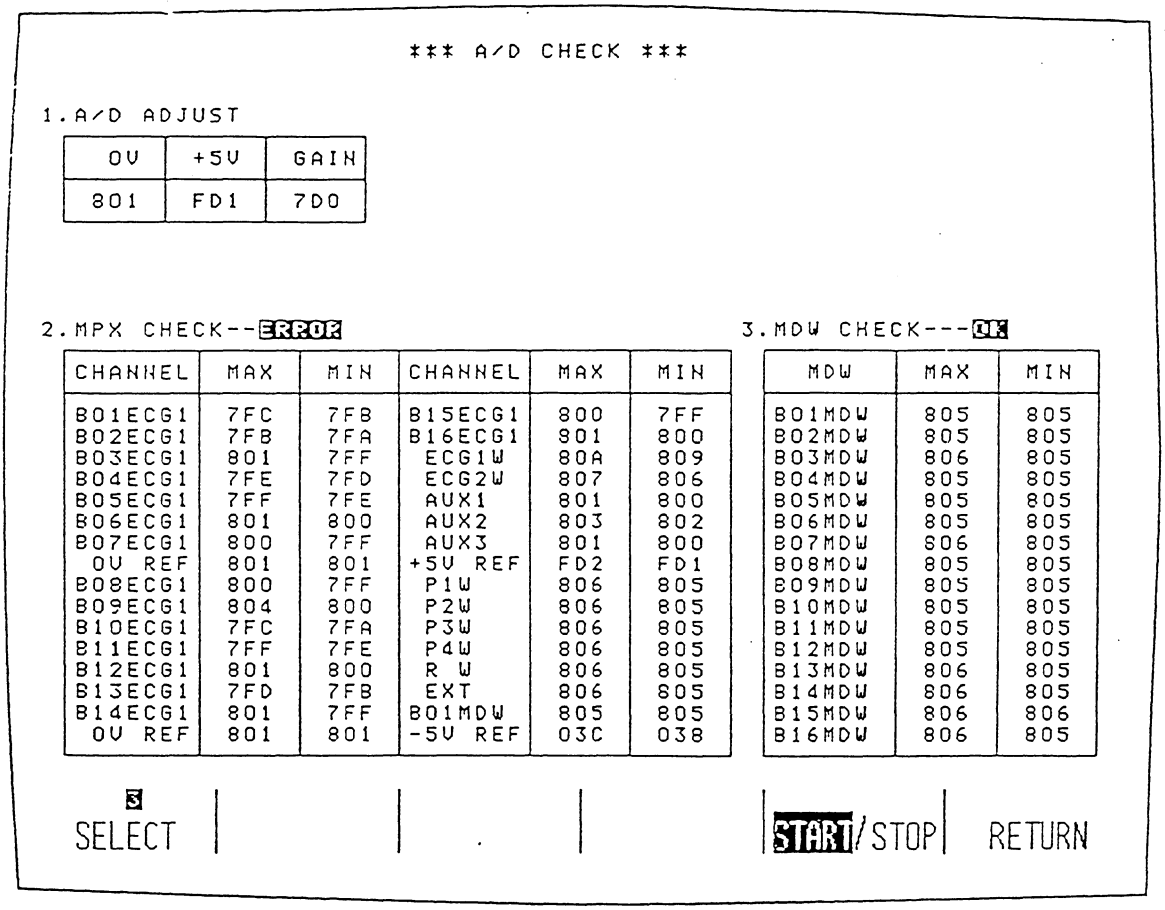
START: to execute the check program of the selected check item

4.3.4.3.1 GLOBAL MEMORY check



This check is same as the CPU board check.

4.3.4.3.2 AD check



*** A/D CHECK ***

1. A/D ADJUST

0V	+5V	GAIN
801	FD1	7D0

2. MPX CHECK--ERROR

CHANNEL	MAX	MIN	CHANNEL	MAX	MIN
B01ECG1	7FC	7FB	B15ECG1	800	7FF
B02ECG1	7FB	7FA	B16ECG1	801	800
B03ECG1	801	7FF	ECG1W	80A	809
B04ECG1	7FE	7FD	ECG2W	807	806
B05ECG1	7FF	7FE	AUX1	801	800
B06ECG1	801	800	AUX2	803	802
B07ECG1	800	7FF	AUX3	801	800
0V REF	801	801	+5V REF	FD2	FD1
B08ECG1	800	7FF	P1W	806	805
B09ECG1	804	800	P2W	806	805
B10ECG1	7FC	7FA	P3W	806	805
B11ECG1	7FF	7FE	P4W	806	805
B12ECG1	801	800	R W	806	805
B13ECG1	7FD	7FB	EXT	806	805
B14ECG1	801	7FF	B01MDW	805	805
0V REF	801	801	-5V REF	03C	038

3. MDW CHECK---OK

MDW	MAX	MIN
B01MDW	805	805
B02MDW	805	805
B03MDW	806	805
B04MDW	805	805
B05MDW	805	805
B06MDW	805	805
B07MDW	806	805
B08MDW	805	805
B09MDW	805	805
B10MDW	805	805
B11MDW	805	805
B12MDW	805	805
B13MDW	806	805
B14MDW	806	805
B15MDW	806	806
B16MDW	806	805

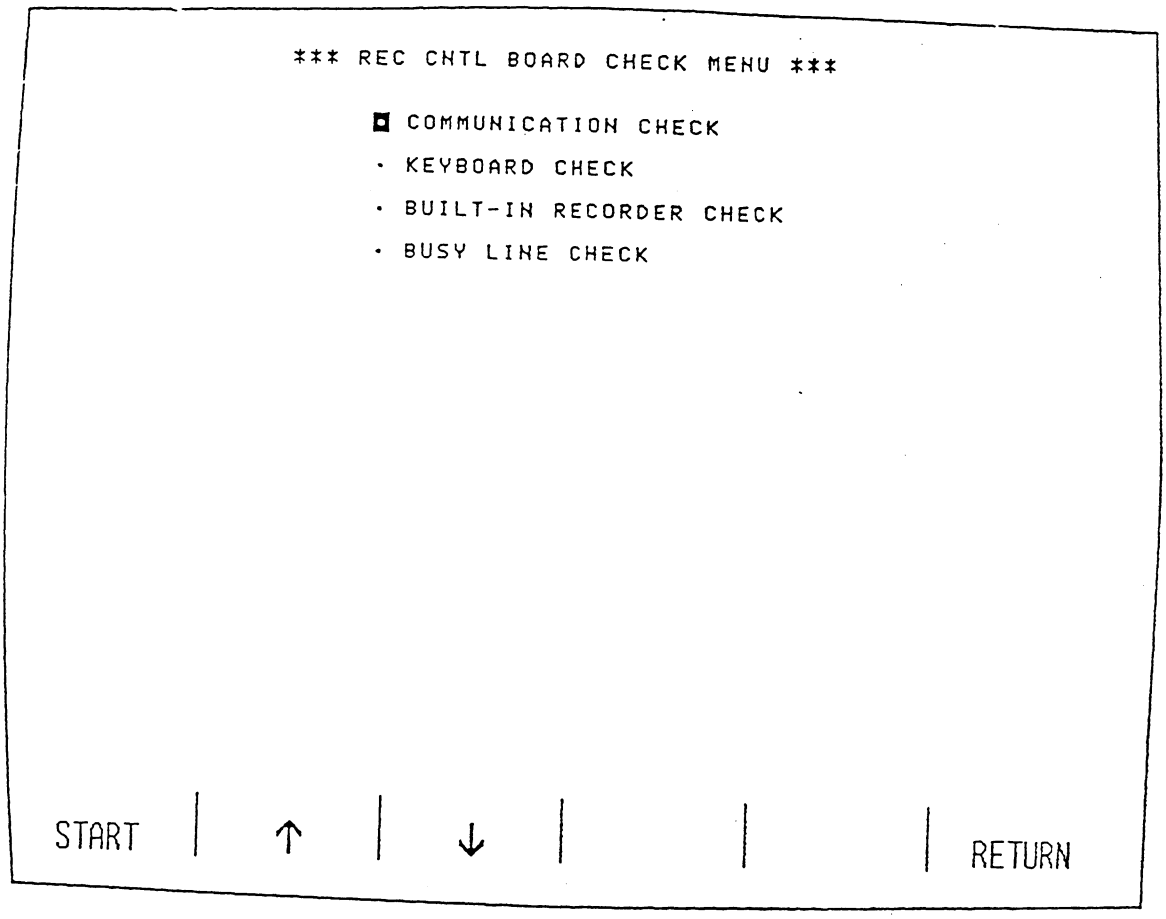
3 SELECT | | | START/STOP | RETURN

1) A/D ADJUST
Used to adjust A/D converter

2) MPX CHECK
Used to check multiplexing function for the A/D conversion. Check result is indicated by OK or ERROR.

3) MDW CHECK
Used to check selection function of the delayed ECG wavefrom (MDW). Check result is indicated by OK or ERROR.

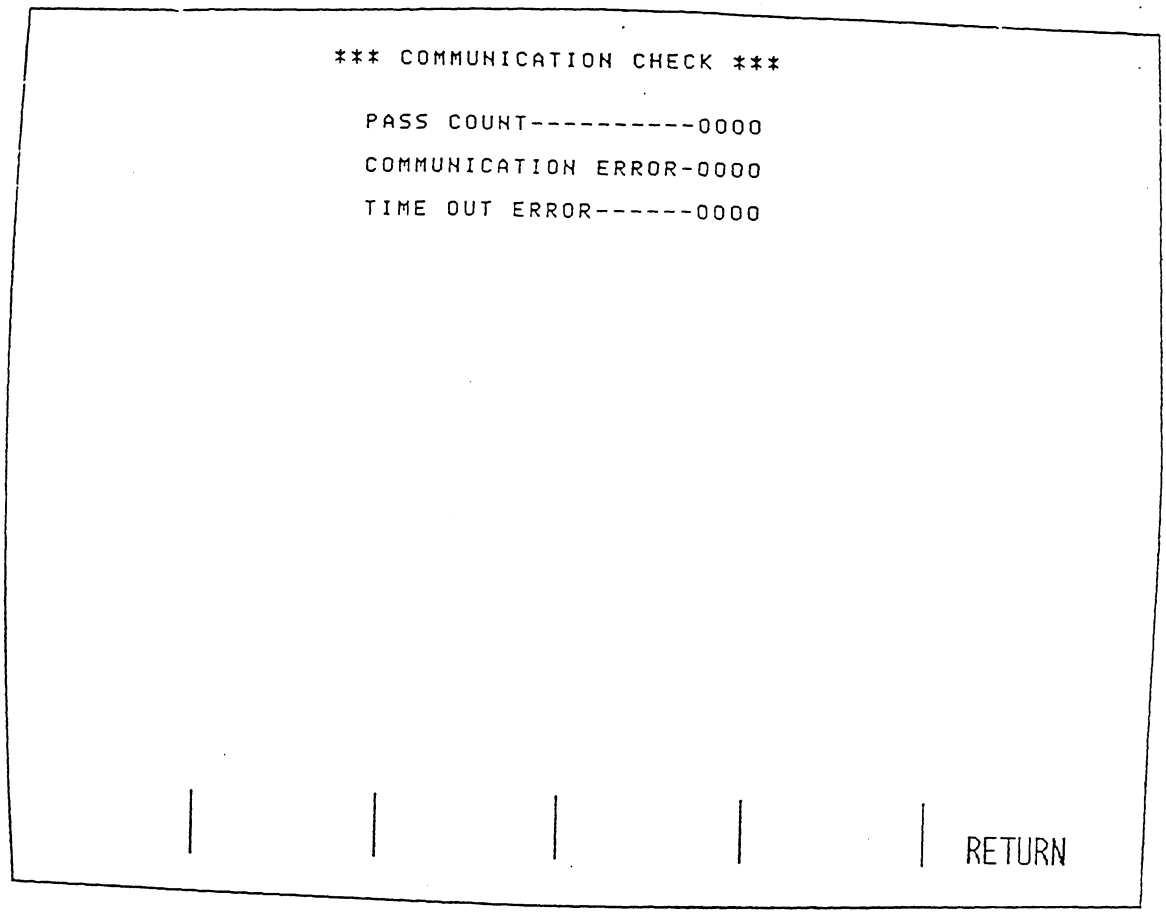
4.3.4.4 REC CNTL board check



↑ ↓ : to select the item for check

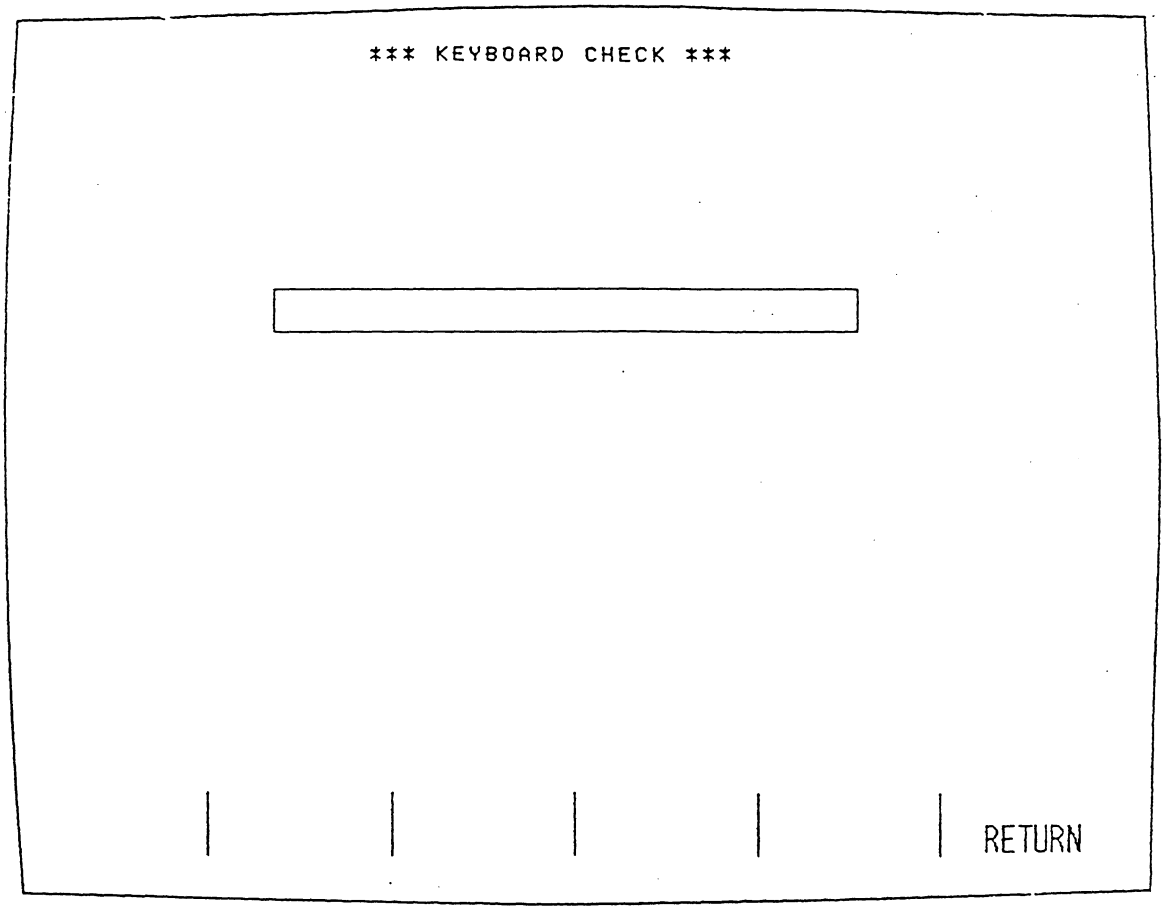
START: to execute the check program of the selected item

4.3.4.4.1 COMMUNICATION check



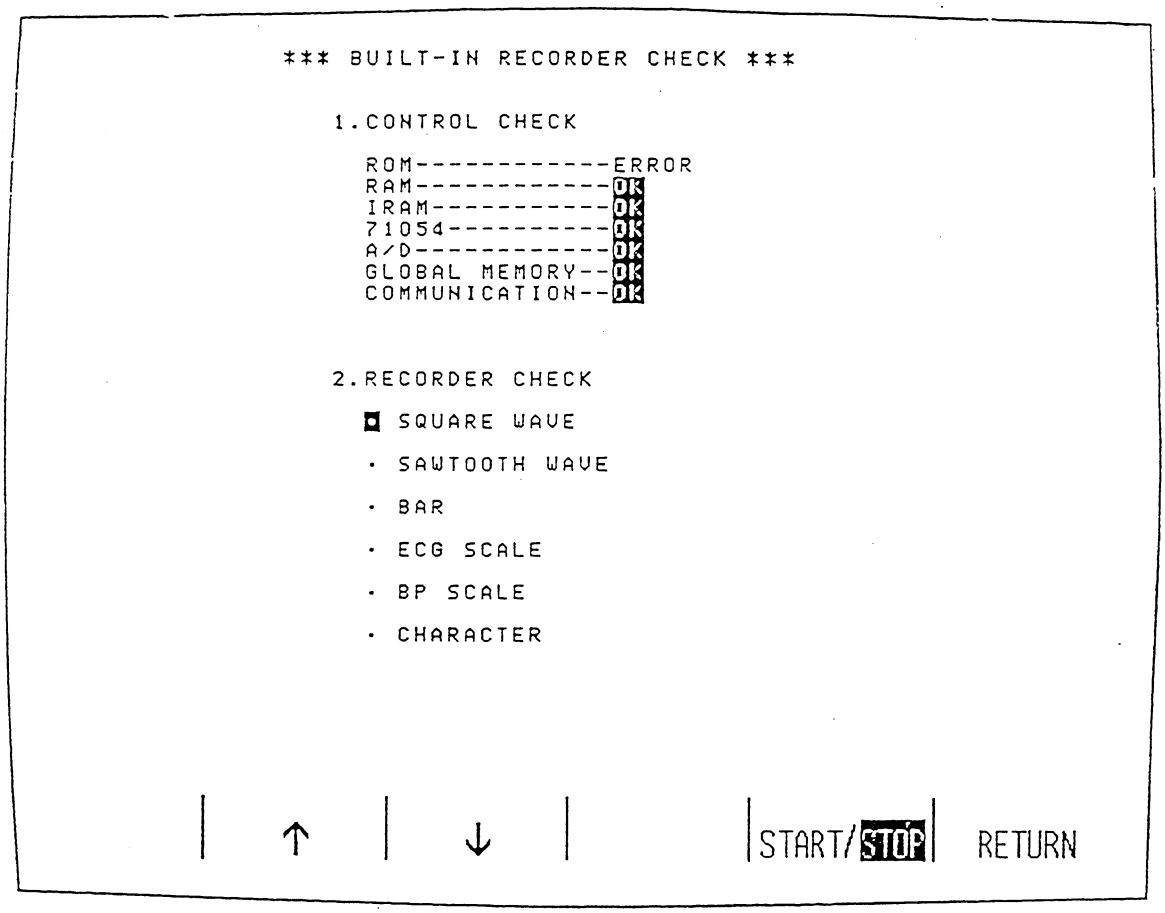
Checks the communciation between MU-820R central monitor main unit and JJ-800R signal exchanger. Connection cable (CNS-JJ8S) is required for this check.

4.3.4.4.2 KEYBOARD check



To check the optional keyboard. When a key on the keyborad is pressed, key name appears in the square on the screen together with key click tone.

4.3.4.4.3 BUIT-IN RECORDER check



↑↓ : Select the item for the check

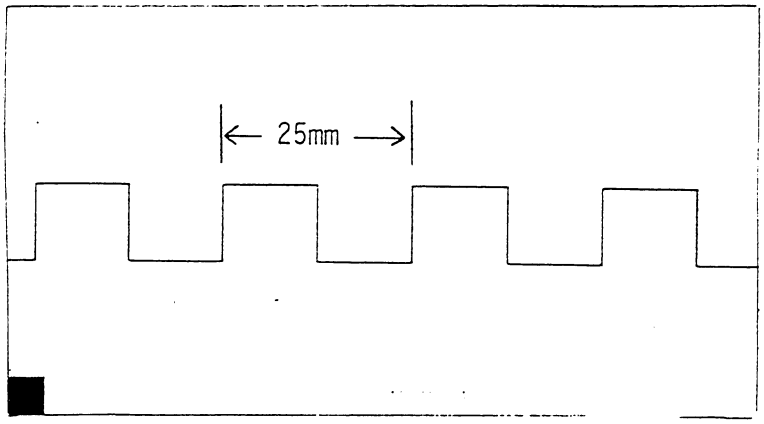
START/STOP: Executes the check program or stops the check.

RETURN: Returns the screen mode to the CHECK MENU screen

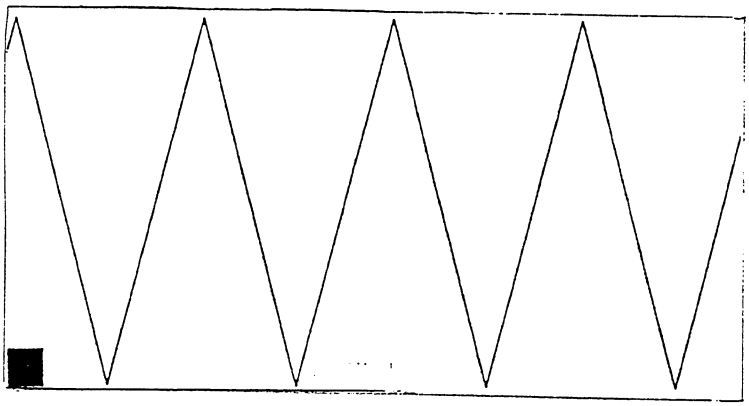
1) CONTROL CHECK
Each check result of the built-in recorder control check is indicated by OK or ERROR.

2) RECORDER CHECK
Activates the recorder to record each check pattern on the paper. Details are described on the next page.

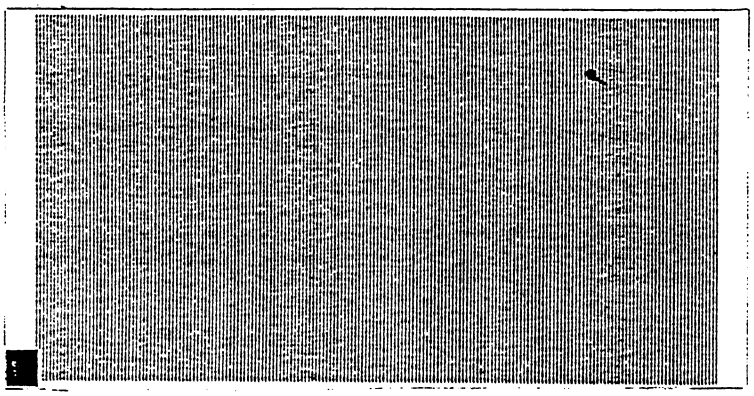
a) SQUARE WAVE check
Used to adjust the paper speed. Paper speed is 25mm/sec and the aquarewave interval is one second on the paper.



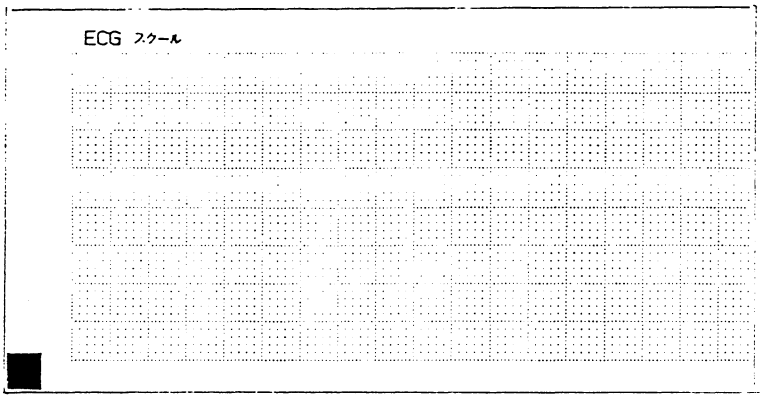
b) SAWTOOTH WAVE check
Used to check waveform trace accuracy.



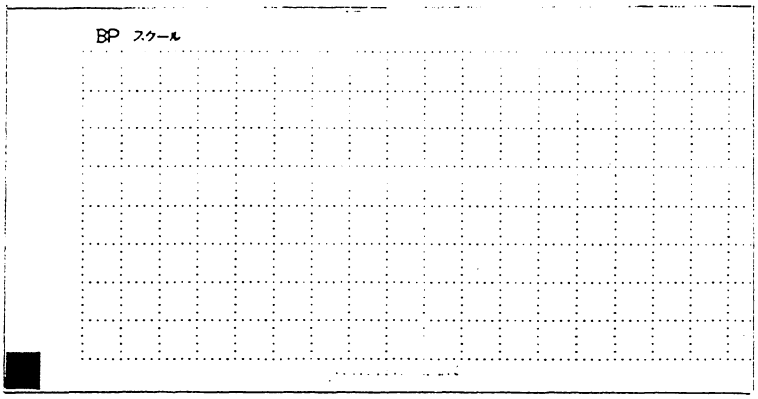
c) BAR check
Used to check paper feeding, dot missing, and print thickness.



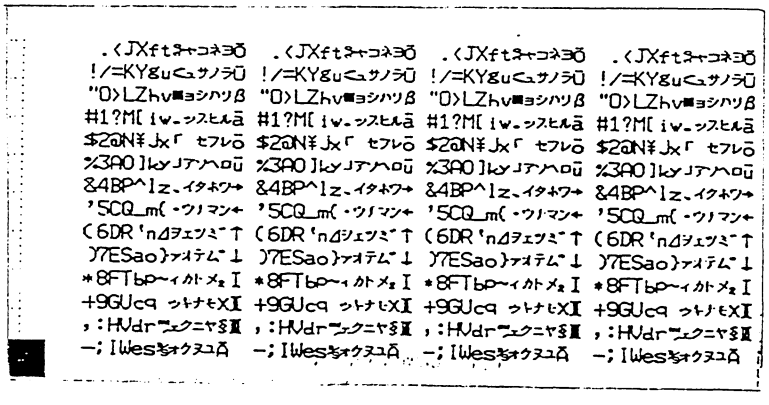
d) ECG SCALE check
Used to check the scale for the ECG waveform.



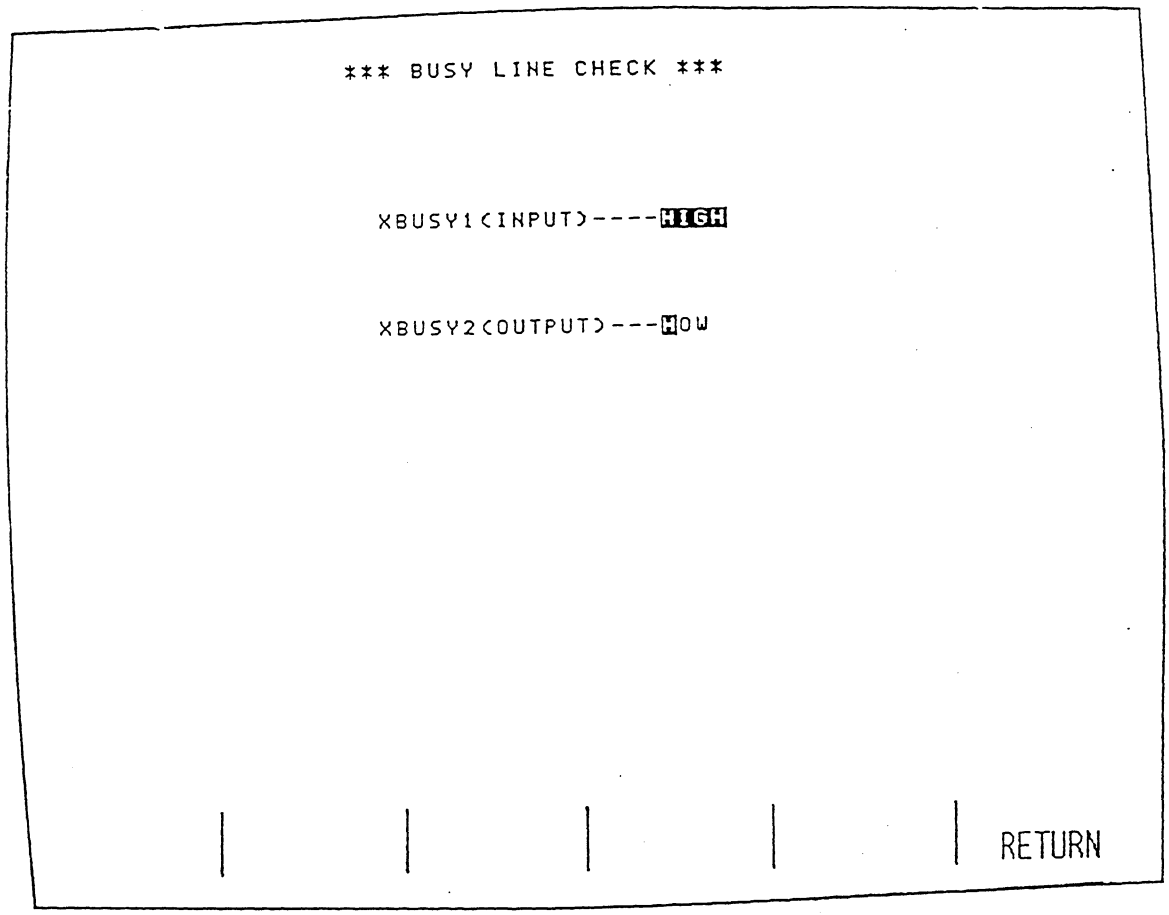
e) BP SCALE check
Used to check the scale for the blood pressure waveform.



f) CHARACTER check
Prints all the provided characters.



4.3.4.4.4 BUSY LINE check

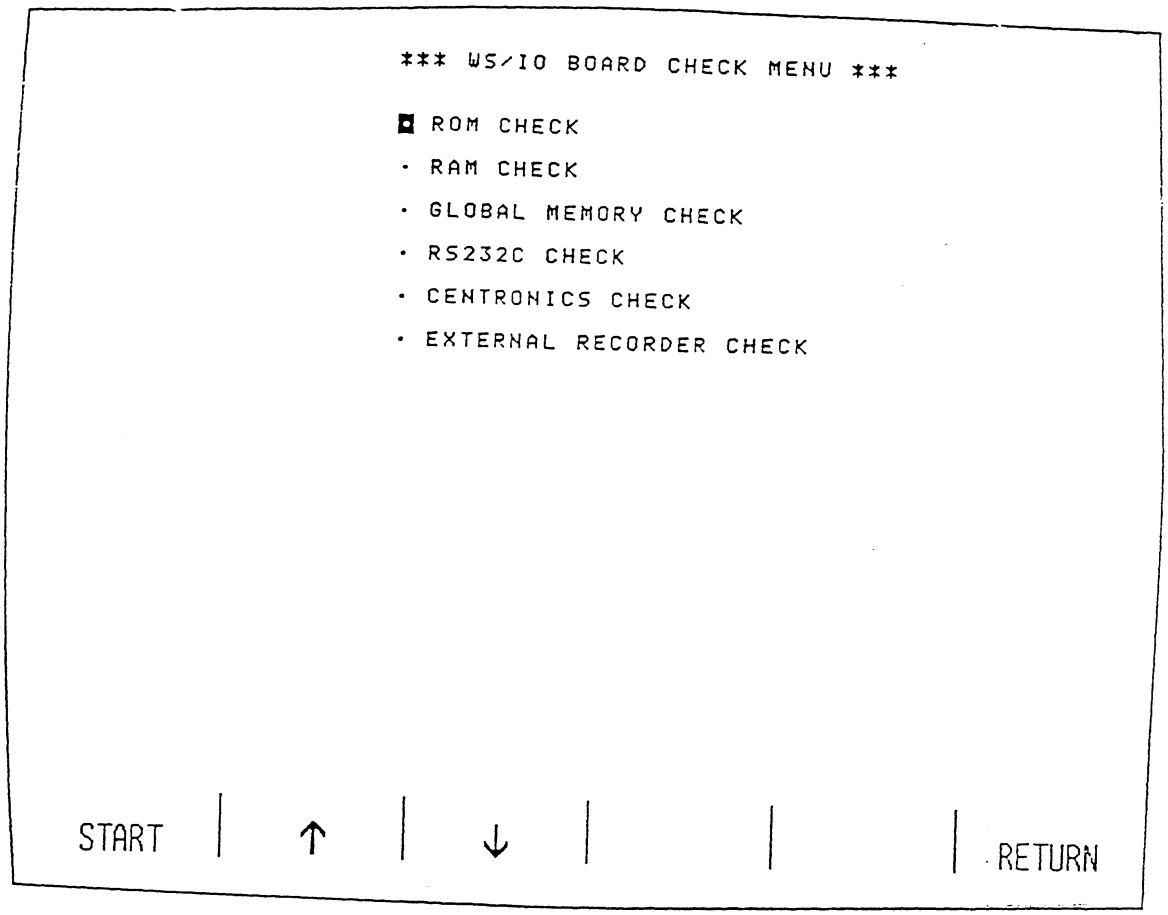


Checks the BUSY lines.

XBUSY1 (INPUT); When the +5V or 0V is applied across the pin-4 and pin-17 (E2 ground) of the connector CN104 on the REC CNTL board HIGH (+5V) or LOW (0V) is displayed on the CRT.

XBUSY2 (OUTPUT); Indicates the voltage output level across the pin-2 and pin-15 of the connector CN104 on the REC CNTL board. HIGH: +5V, LOW: 0V.

4.3.4.5 WS/IO board check



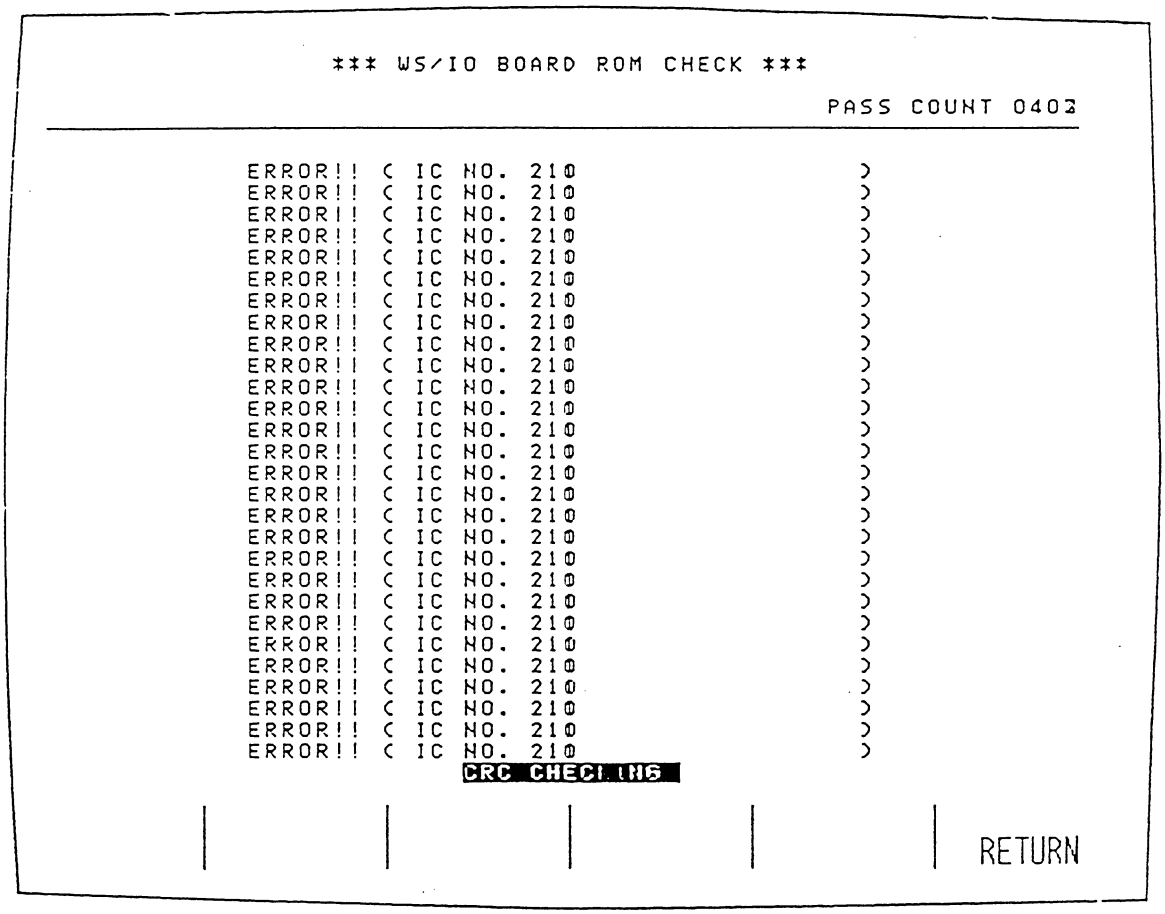
Above screen appears when WS/IO CHECK is selected on the CHECK MENU screen.

↑↓ : Selects the item for the check

START: Executes the check program of the selected item

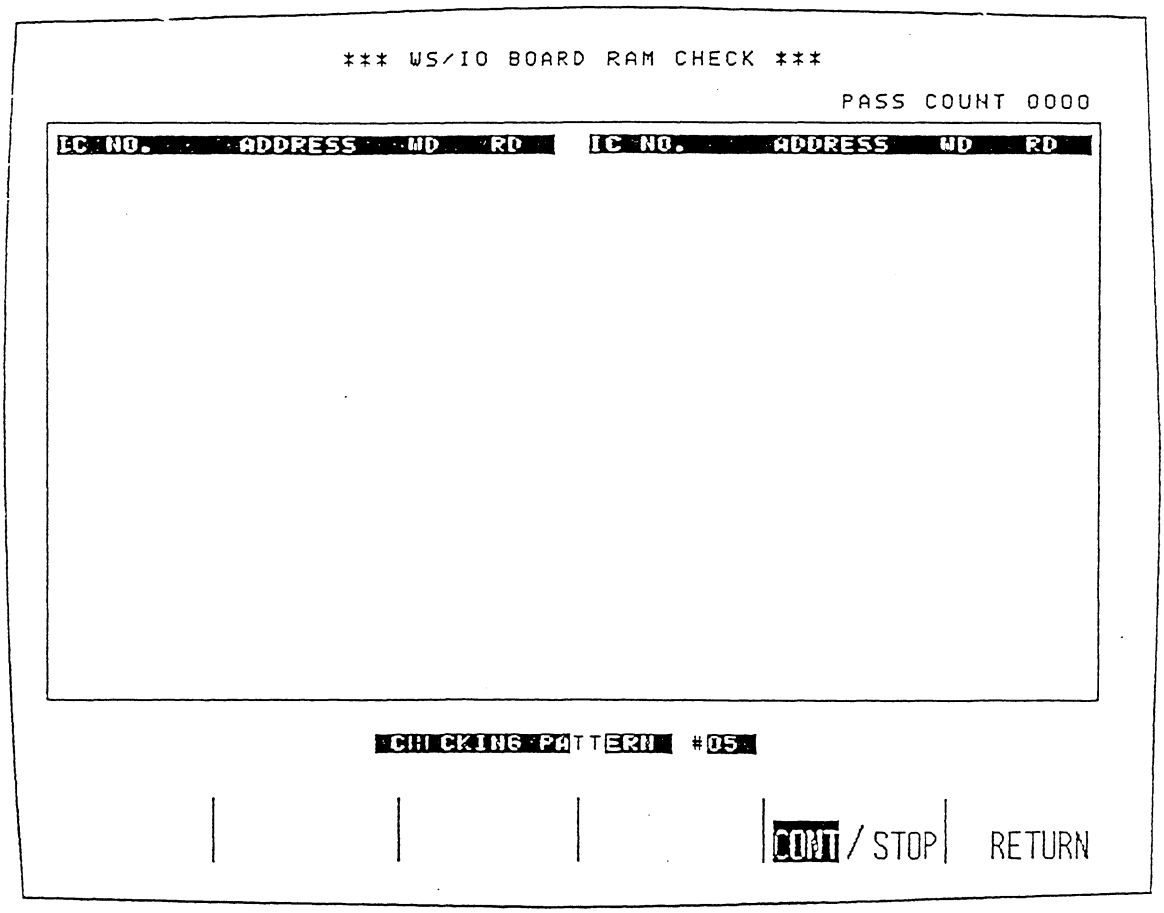
RETURN: Returns the screen to the CHECK MENU

4.3.4.5.1 ROM check



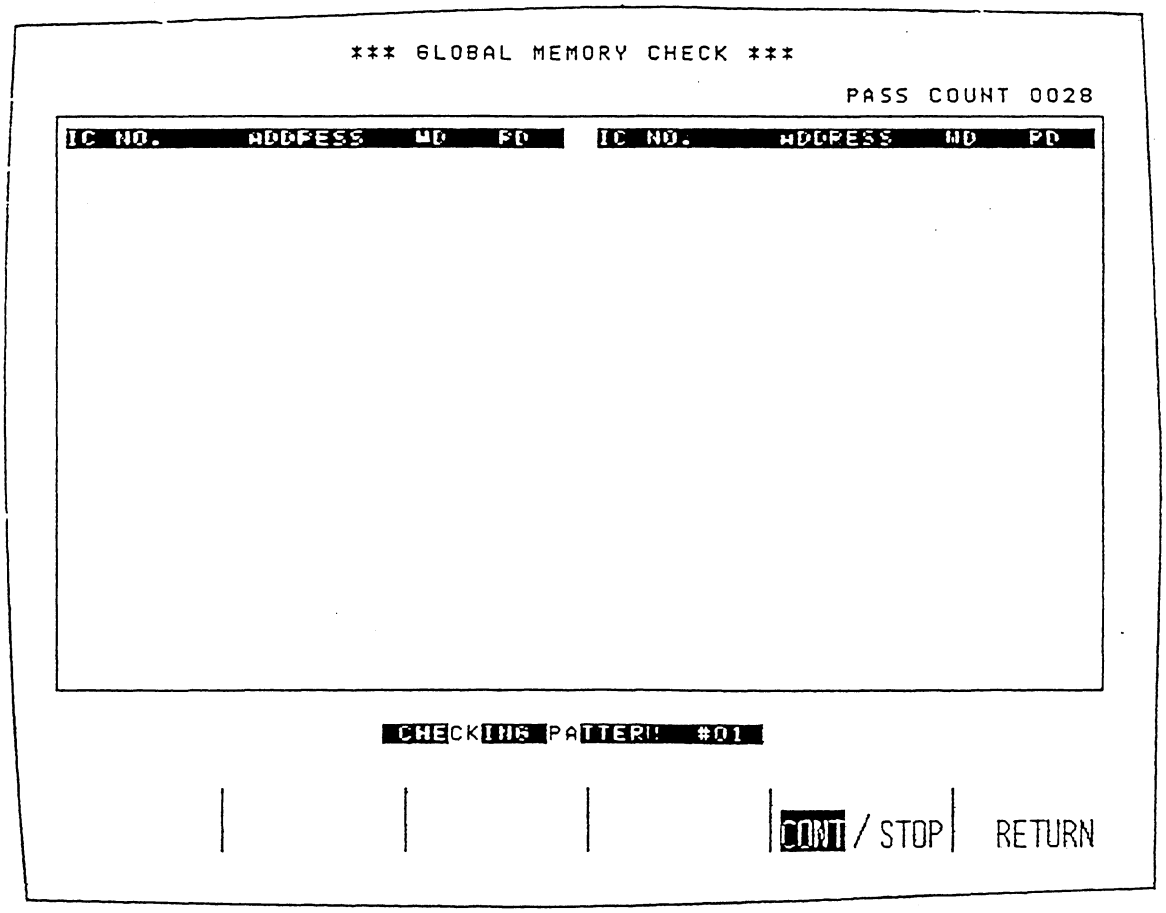
Above screen sample indicates that the ROM check program is running.
ROM chips are not yet mounted on the board, ERROR will be displayed on the CRT which does not indicate faulty component.

4.3.4.5.2 RAM check



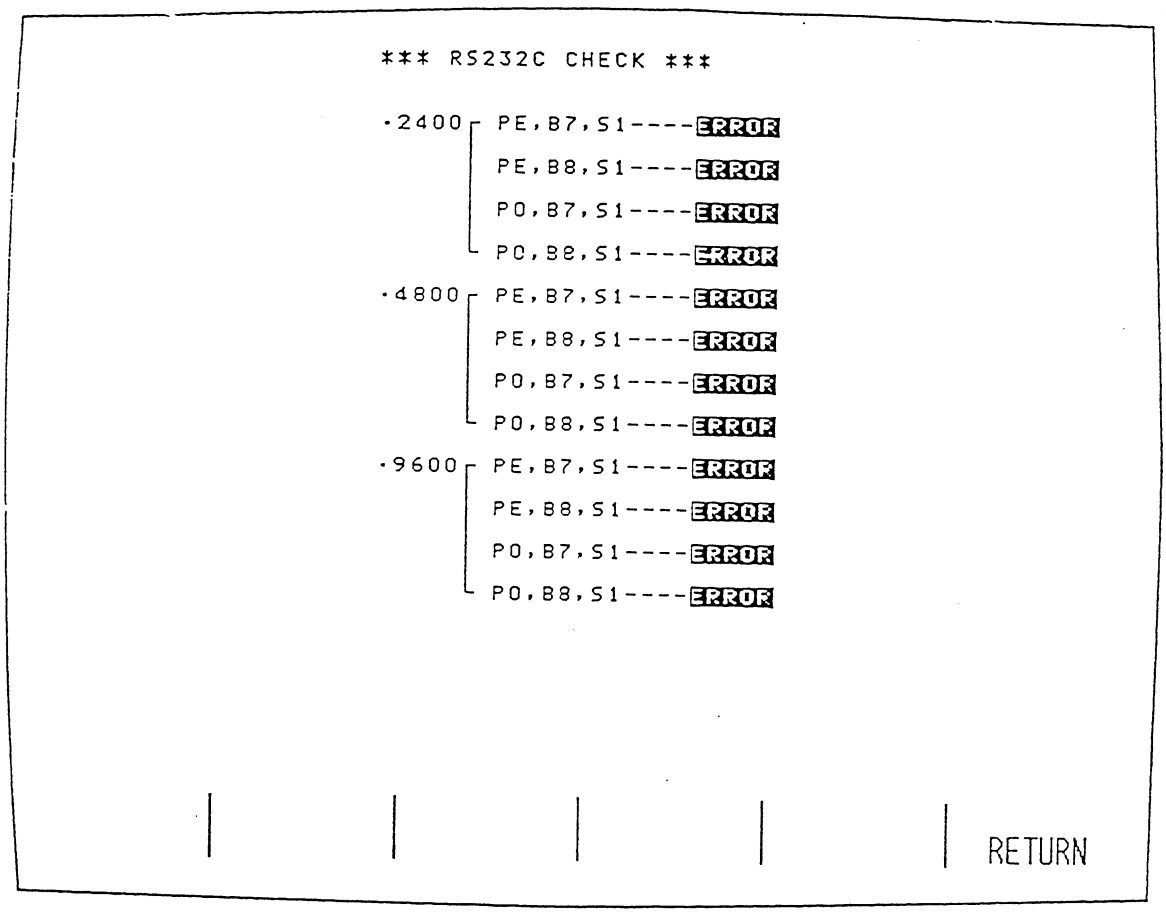
Above screen example indicates that the RAM check program is running. When the PASS COUNT indicates 0001 and there is no ERROR indication, RAM is normal.

4.3.4.5.3 GLOBAL MEMORY check



Above screen example indicates that the GLOBAL MEMORY (dual port RAM) check program is running. When the PASS COUNT indicates 0001 and there is no ERROR indication, global memory is normal.

4.3.4.5.4 RS232C check

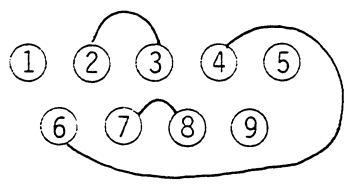


Above screen example indicates that the WS/IO serial data port check program is running.

For this check, Loop back jig is required to be connected to the SERIAL connector on the WS/IO board.

[loop back jug (D-SUB 9-pin male connector)

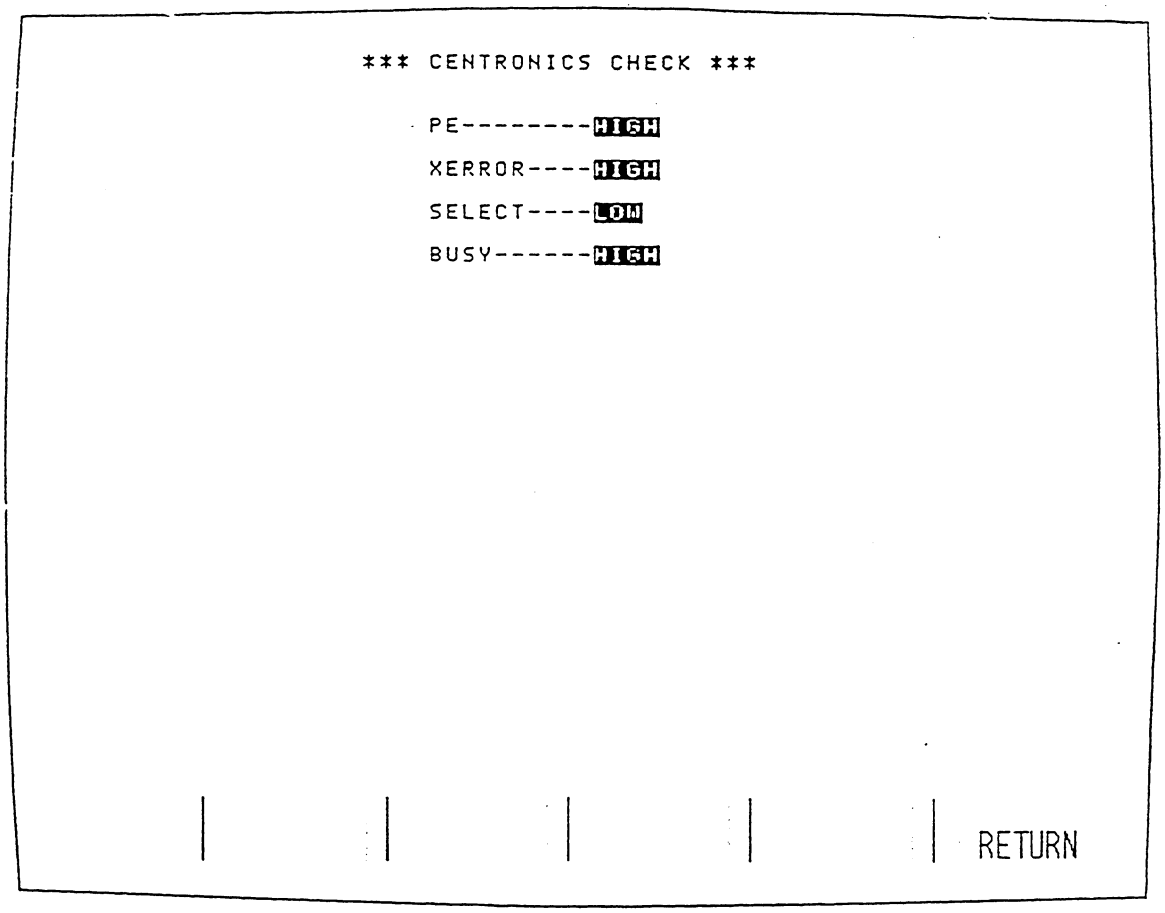
Short the pins as below.



Pin-2: TxD
Pin-3: RxD
Pin-6: DCD
Pin-7: RTS
Pin-8: CTS

All the items are indicated with OK when check results are normal. If not normal, ERROR will be indicated.

4.3.4.5.5 CENTRONICS check



Above screen example indicates that the WS/IO parallel data port check program is running.

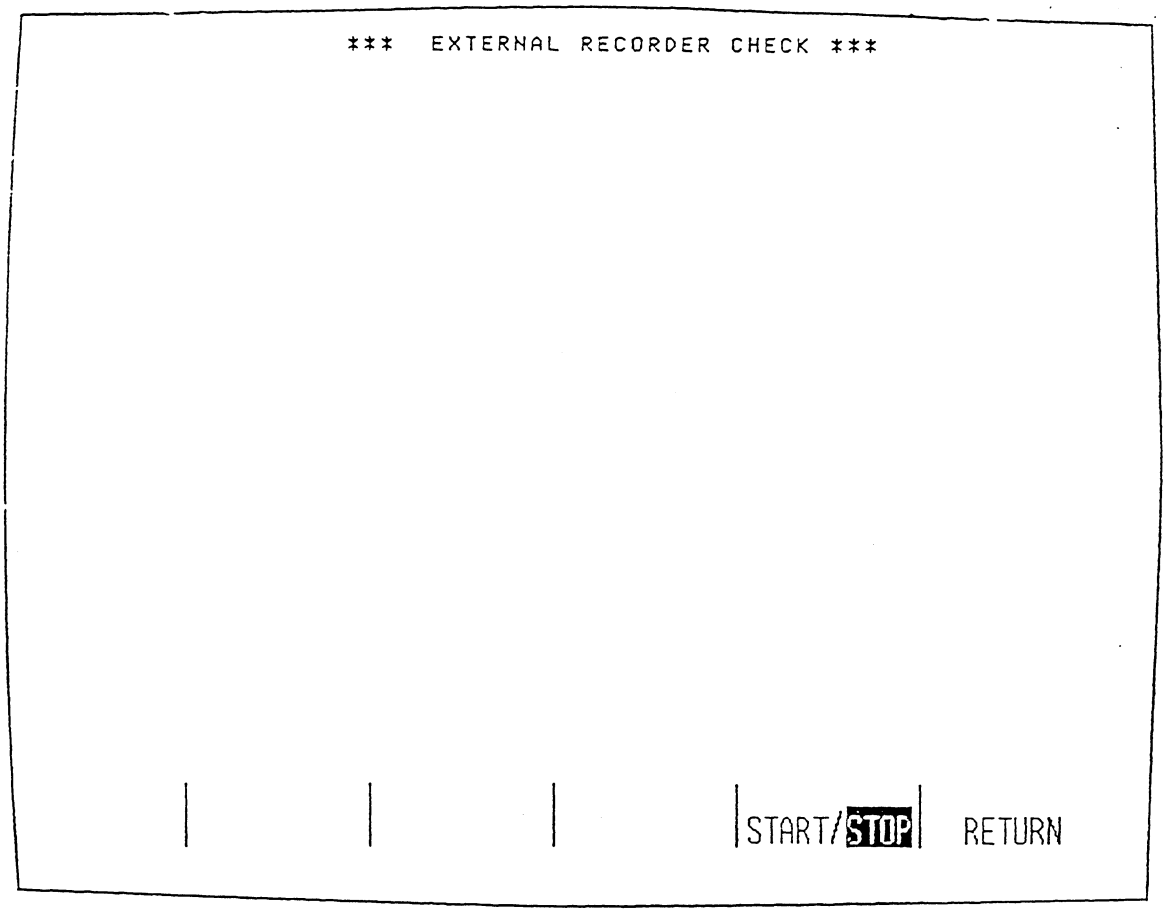
For this check, parallel data port check jig is required to be connected to the PARALLEL connector.

a) Check that the PE, XERROR, SELECT, and BUSY are indicated with HIGH or LOW according to the test signal of the jig (HIGH or LOW).

b) Confirm that the eight LED lamps of the jig light up one by one.

When the jig is not connected, all the items are indicated with HIGH.

4.3.5.6 EXTERNAL RECORDER check



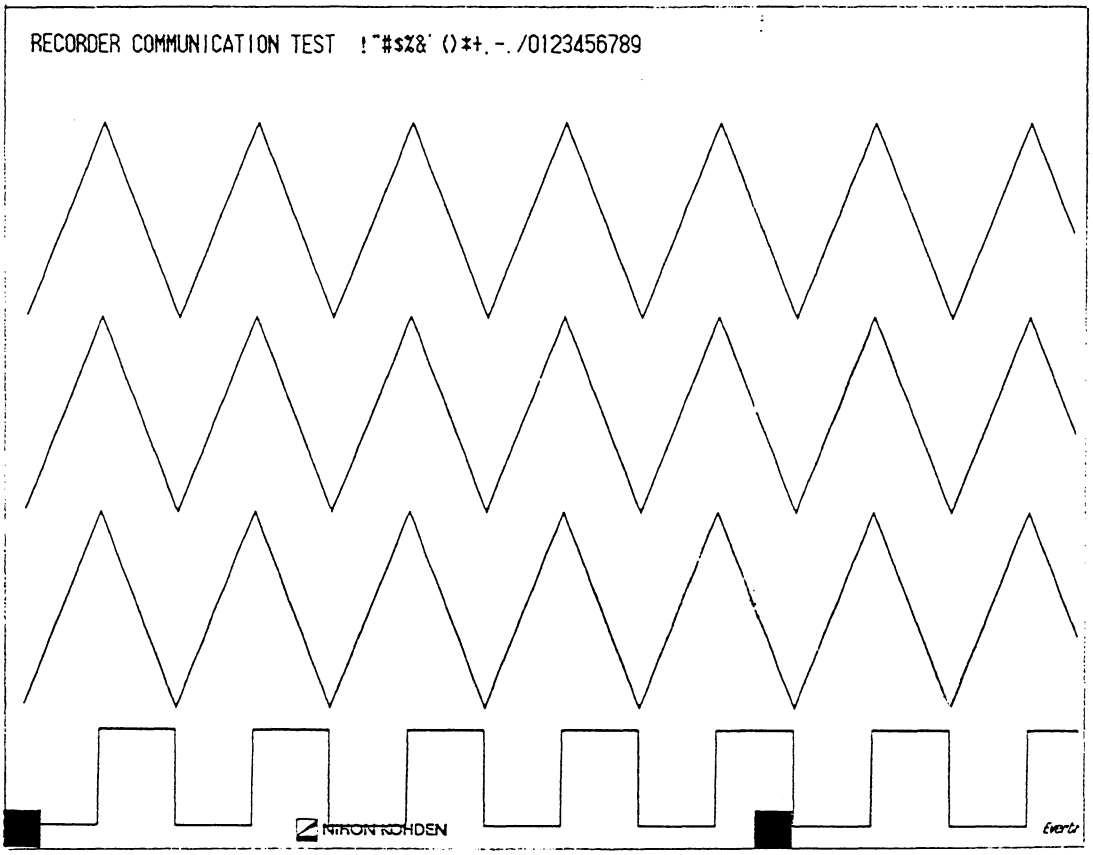
This program is used to check the external thermal array recorder WS-841RA/J/K. Connect the WS-841R to the central monitor main unit and turn power on of the recorder.

When the WS/IO check is normally completed, test pattern shown on the next page is printed on the paper.

If WS DISCONNECTED is dispalyed on the CRT, power of the recorder is off or the cable is not connected normally.

If COMMUNICATION ERROR is displayed, communiation between the central monitor main unit and the WS recorder is abnormal.

WS/IO EXTERNAL RECOEDER CHECK test pattern



Section 5

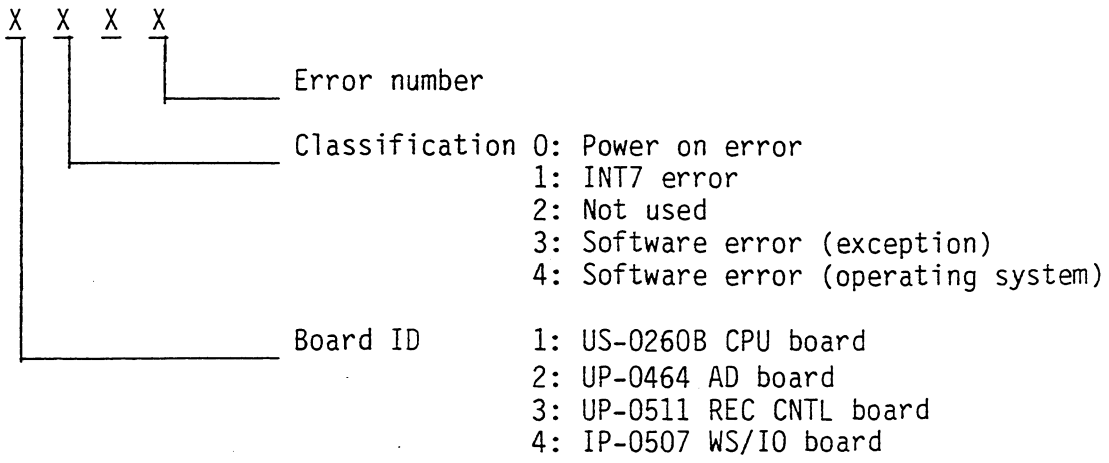
5. Troubleshooting

5.1 Error

5.1.1 Error code

1) Error code

The error code is registered with 4 digit haxa-decimal number on ERROR HISTORY according to the following list if an is found.



2) Classification

2-a) Classification 0: Power on error

Error number	Error	Error number	Error
0	Not used	8	Not used
1	ROM	9	EEPROM
2	RAM	A	Dual port error
3	71051	B	Not used
4	71054	C	Not used
5	8279	D	Not used
6	72001	E	A/D REF error
7	8255	F	Not used

2-b) Classification 1: INT7 ERROR

Error number	Error
0	Not used
1	Watch dog timer error
2	Power down error
3	Not used

2-c) Classification 2: Not used

2-d) Classification 3: Software error (exception)

Error number	Error	Error number	Error
0	Not used	8	Suprious interrupt
1	bus error	9	Undefined auto vector
2	Address error	A	Undefined trap
3	Illeagal instruction	B	Undefined unser interrput
4	Zero drive	C	Other error
5	Check (CHK) instruction	D	
6	Trap instruction	E	
7	Privilege instruction	F	

2-e) Classification 4: Software error (operating system)

Error number	Error
0	Not used
1	Fatal error
2	Minor error
3	Fork periodic (FORKP) error
4	Not used
5	Not used
6	Not used
7	Not used

5.1.2 Error code list and PC board replacement

This table shows PC board repalcement priority when an error code is displayed.

Error code	CPU board US-0260B	AD board UP-0464	REC CNTL BOARD UP-0511	WS/IO board UP-0507	Remarks
1001	1				
1002	1				
1003	1				
1004	1				
1005	1				
1009	1				
1101	1				
1102	1				Check +5V
200A	2	1			
200E	2	1			
300A	2		1		
4002	2			1	
4006	2			1	
4007	2			1	
400A	2			1	

1: First priority to replace.
2: Second priority to replace.

5.2 PC board replacement and malfunction

Malfuncion		PCB replacement priority							
		CPU	CRTC	SOUND	Operat-ion BD	CRT unit	SW REG	Power BD	Note
Switch	No key operation	2			1				
Sound	No sound generation	2		1					A
	No alarm sound	2		1	3				B
Display	No CRT display		2			1	3		C
	Distorted display		2			1	3		
	Wave, character or graph is not normal		1						
Power	Power lamp off				3		1	2	D
	No fan rotation						1	2	E
	Fuse for 60V blows								F
Others	Error lamp is lit	1			2		3		
	Display changes to to self check from normal display	1			2		3		

[NOTE]

A: Check integrity of speaker and speacker cable.

B: There is no check part before replacement since alarm sound is not fully fadeable by the alarm volume (fadeable by position change of J1 jumper on the UP-0265).

C: Check BRIGHT volume of the front and internal brightness control.

D: Check main fuse.

E: Confirm that the fan is connected and there is no obstrunctions to fan rotation.

F: Confirm that fan is running and the unit is not overheated.

Section 6

6. Adjustment

			Page
6.1	UP-0315	Regulator unit	6-1
6.2	UP-0262	CRTC board	6-1
6.3	VM-003P	CRT unit	6-2
6.4	UP-02602	CPU board	6-2
6.5	UP-0464	AD board	6-3
6.6	UP-0512	REC DRV board	6-3

6.1 UP-0315 Regulator unit

1) **+60V adjustment** (VR001)
Adjust the VR001 to set 60V (tolerance ±0.6V) at test pin "+60V"

2) **Ampere adjustment (VR002)**
Connect a load and a voltmeter in parallel between "+5V" and "E2" and connect an Ampere meter in series with the load. Adjust the VR002 for protecting the +5V switching regulator circuit against excessive current so that 5V starts to drop down at test pin "+5V" when the load current is 9A.

3) **+5V adjustment (VR003)**
Adjust the VR003 to set +5V (Tolerance ±0.01V) at the test pin "+5V" without a load.

6.2 UP-0262 CRTC board

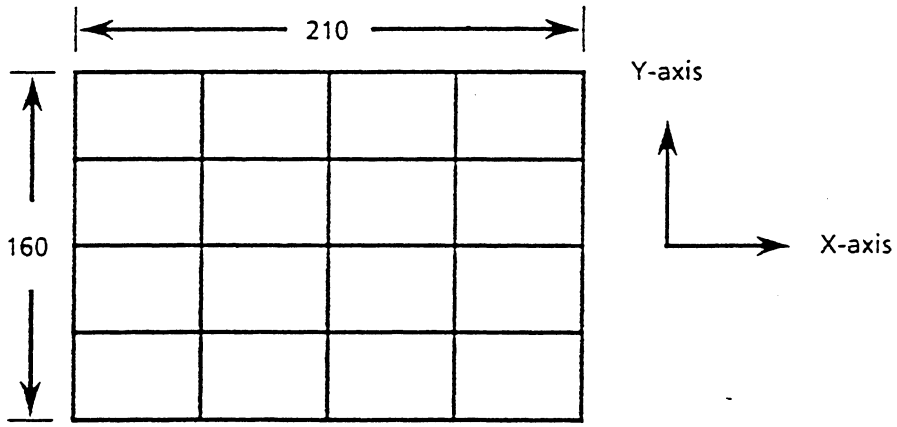
1) **DCLK adjustment (VC001)**
Adjust the VC001 (variable capacitor) so that a clock pulse of 64MHz povides a delay time of 2.5ns (Tolerance ±0.5ns) at thest pin "DCLK".

6.3 VM-003P CRT unit

1) V.HOLD (VR002)
If a display moves X-axisward on the CRT, adjust the VR002 to fix the display.

2) H.HOLD (VR001)
If a display moves Y-axisward on the CRT, adjust the VR001 to fix the display.

3) HEIGHT (VR003)
Adjust the VR003 to be set at 210mm (Tolerance ±2%) long X-axixward after displaying "GRAPHIC DISPLAY" in the Manual Self Check program on the CRT as below.



4) WIDTH (L002)
Adjust the L002 to be set at 160mm (Tolerance ±2%) long Y-axisward on the CRT as above.

5) V.LIN (VR004)
Adjust the VR004 to compensate for Y-axisward linearity on the CRT.

6) FOCUS (VR005)
Adjust the VR005 so that the grid pattern can be observed most clearly on the CRT.

6.4 UP-02602 CPU board

1) Real time clock (VC101)
Adjust the VC101 so that a 1Hz clock (Tolerance ±0.00001) is acquired between test pin "STDP" and "E2".

6.5 UP-0464 AD board

1) +5VREF (VR703)
Adjust the VR703 to set +5V at test pin +5VREF.

2) -5VREF (VR704)
Adjust the VR704 to set -5V at test pin -5VREF.

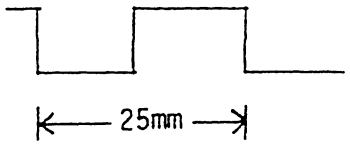
3) A/D GAIN (VR702)
Call up the Self Check Menu No.1 and adjust the VR702 so that A/D ADJ GAIN reads "7D0".

4) A/D OFFSET (VR701)
Call up the Self Check Menu No.1 and adjust the VR701 so that the A/D OFFSET reads "800".

6.6 UP-0512 REC DRV board

1) MARK detect level (built-in recorder)
Adjustment is done with a test jig at test pin "MK".

2) Paper speed (built-in recorder)
Call up the Self Check Menu BUILT-IN RECORDER CHECK and by measuring the squarewave interval on the paper of 25mm/sec speed, adjust the VR102 to set the interval to 25mm.



3) Thermal head drive voltage
Adjustment is done at test pin VTH to set the specified voltage as below.

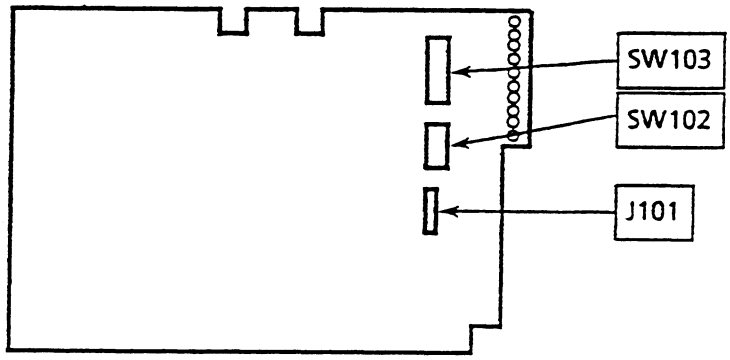
NOTE: This table is for MU-820RA/J/K only.

Thermal head resistance (Ohm)	Thermal head drive voltage VTH-ETH (V)0 within +/-0.1 V
161- 170	9.7
171- 180	10.0
181- 190	10.2
191- 200	10.5
201- 210	10.8
211- 220	11.0
221- 230	11.2

Section 7

7. Internal switch and jumper setting

7.1 UP-02602 CPU board



DIP switch SW102

Bit	Function	Initial set
1	No use	OFF
2	No use	OFF
3	No use	OFF
4	ON: Watch Dog Timer does not work	OFF

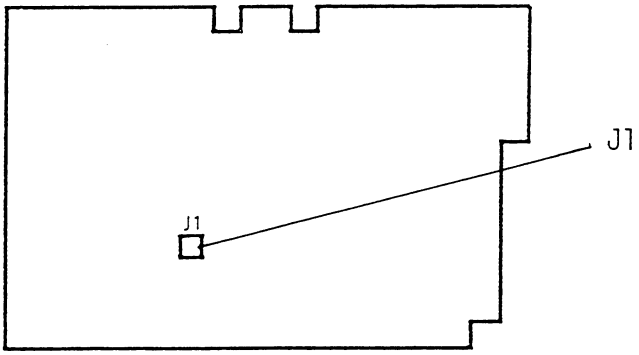
DIP switch SW103

Bit	Function	Initial set
1	No use	OFF
2	No use	OFF
3	No use	OFF
4	No use	OFF
5	No use	OFF
6	No use	OFF
7	ON: Used for additional RAM	OFF
8	ON: Used in debug mode	OFF

Jumper J101

ROM name	Short termimal position (initial set
27512	2A-2B, 4A-4B, 6A-6B, 8A-8B

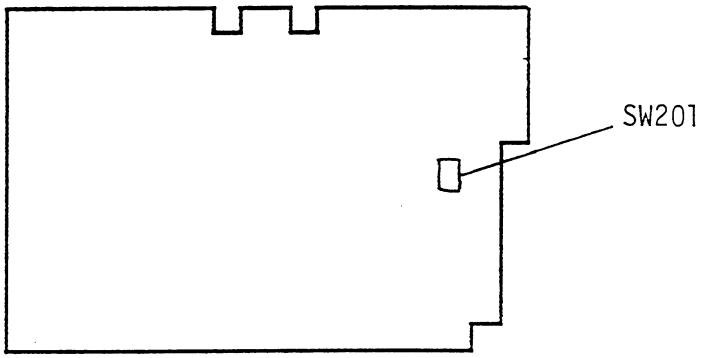
7.2 UP-0262 CRTC board



Jumper J1

Jumper	Function	Initial set
J1	Short: Used to INT5(O) Output	Open

7.3 UP-0507 WS/IO board



DIP switch SW201

Bit	Function	Initial set
1	XACK	ON
2	BUSY	OFF
3	XACK	OFF
4	BUSY	ON

Section 8

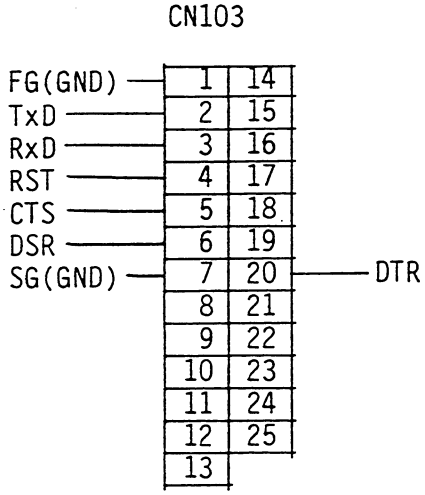
8 Connector pin assignment

Page

Connectors on the rear panel
UP-02602 CPU board (RS-232C) 8-2
UP-0464 AD board (JJ-W) 8-2
UP-0511 REC CONTL borad (JJ-S, VIDEO) 8-3
UP-0507 WS/IO board (WS) 8-3
IO panel (SERIAL, PARALLEL) 8-4

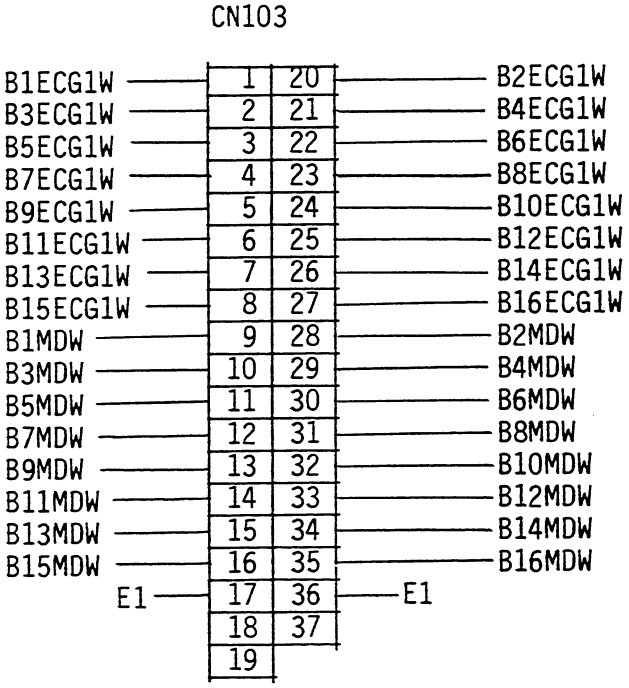
8.1.1 UP-02602 CPU board

RS-232C connector



8.1.2 UP-0464 AD board

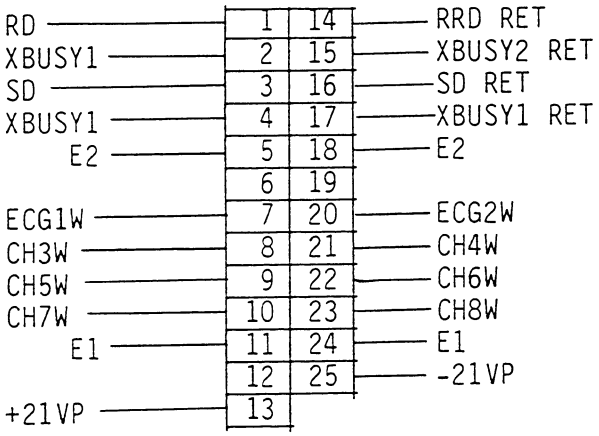
JJ-W connector



8.1.3 UP-0511 REC CNTL board

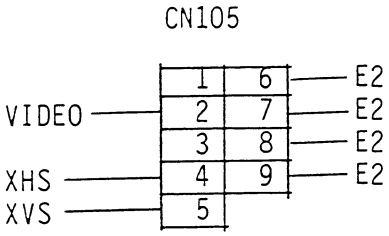
JJ-S connector

CN104



VIDEO connector

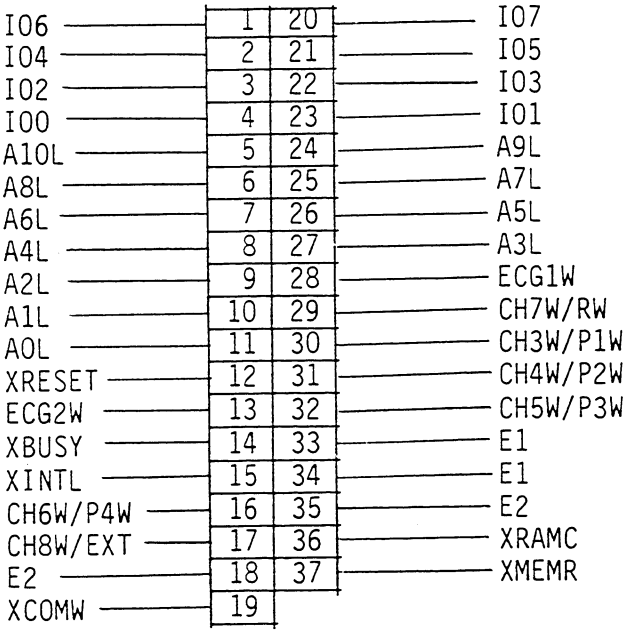
CN105



8.1.4 UP-0507 WS/IO board

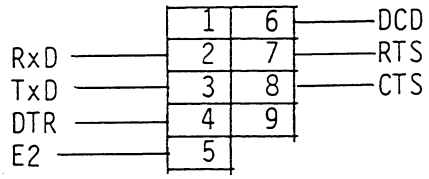
WS connector

CN105



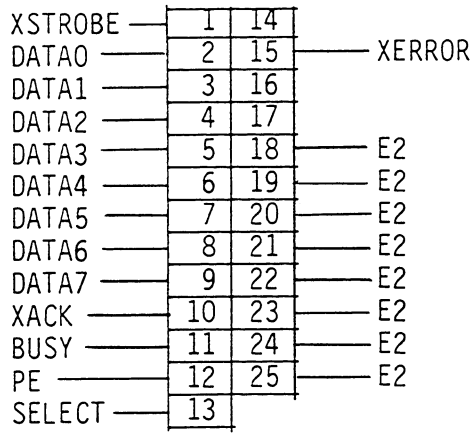
8.1.5 IO panel

SERIAL connector



PARALLEL connector

CN103



Section 9

9. IC data list

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	HA17903	9-6
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	uPD71054	9-7
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On REC DRV board	HA17901	9-16
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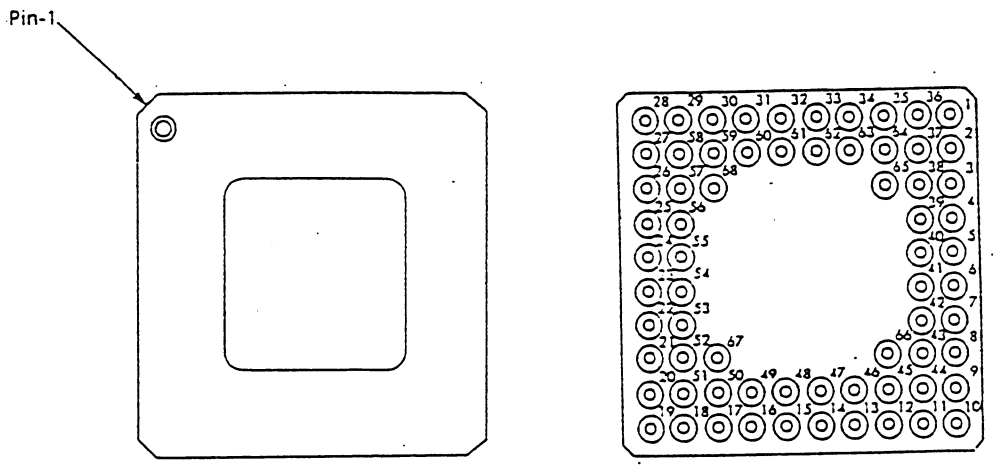
	SWC-01	9-17

16-bit Micro Processing Unit

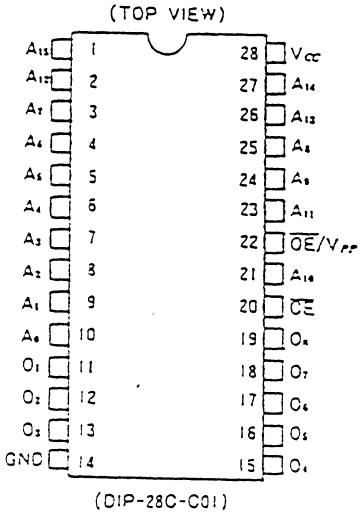
(Top view) (Bottom view)



1	N/C	18	A_9	35	D_1	52	A_{12}
2	$\overline{DTACK}$	19	N/C	36	$\overline{AS}$	53	A_{15}
3	$\overline{BGACK}$	20	A_{14}	37	$\overline{LDS}$	54	A_{18}
4	$\overline{BR}$	21	A_{16}	38	$\overline{BG}$	55	V_{CC}
5	CLK	22	A_{17}	39	V_{CC}	56	V_{SS}
6	$\overline{HALT}$	23	A_{19}	40	V_{SS}	57	A_{23}
7	$\overline{VMA}$	24	A_{20}	41	$\overline{RES}$	58	D_{14}
8	E	25	A_{21}	42	$\overline{VPA}$	59	D_{11}
9	$\overline{BERR}$	26	A_{22}	43	$\overline{IPL_2}$	60	D_9
10	N/C	27	D_{15}	44	$\overline{IPL_0}$	61	D_6
11	FC_2	28	D_{12}	45	FC_1	62	D_3
12	FC_0	29	D_{10}	46	N/C	63	D_0
13	A_1	30	D_8	47	A_2	64	$\overline{UDS}$
14	A_3	31	D_7	48	A_5	65	R/$\overline{W}$
15	A_4	32	D_5	49	A_8	66	$\overline{IPL_1}$
16	A_6	33	D_4	50	A_{10}	67	A_{13}
17	A_7	34	D_2	51	A_{11}	68	D_{13}

MBM27C512

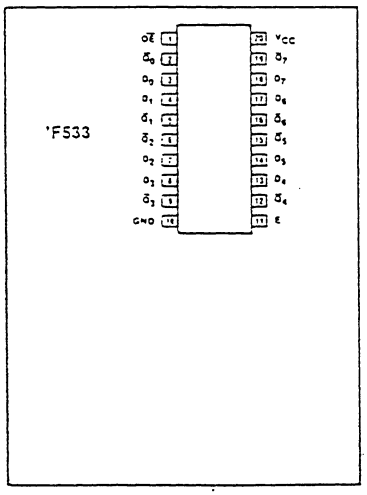
ROM



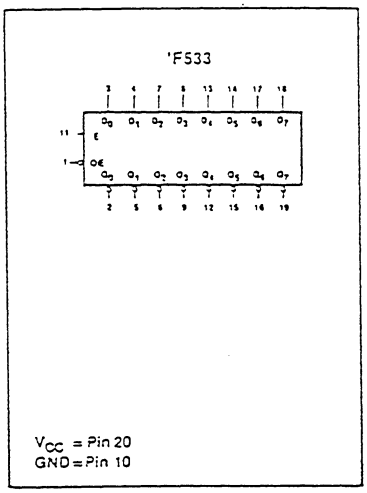
54/74F533

Octal Transparent Latch (3-state)

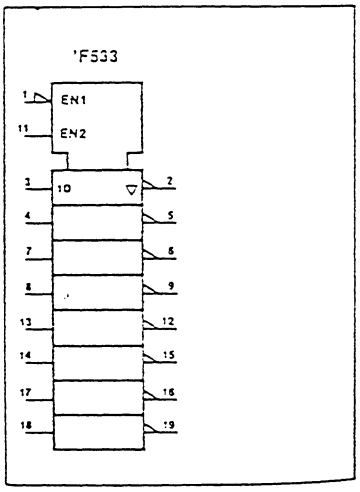
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74F533	6.0ns	41mA

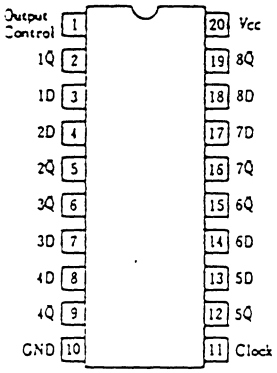
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

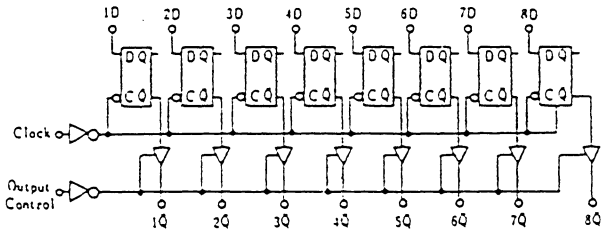
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_0-D_7 ('F533 & 'F534)	Data Inputs	1.0/1.0	20μA/0.6mA
E ('F533)	Latch Enable Input (Active HIGH)	1.0/1.0	20μA/0.6mA
$\overline{OE}$ ('F533 & 'F534)	Output Enable Input (Active LOW)	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{O}_0$-$\overline{O}_7$ ('F533 & 'F534)	3-State Outputs	150/33	3mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

HD74HC534

Octal D-Type Flip-Flop (with Inverted 3-State Outputs)





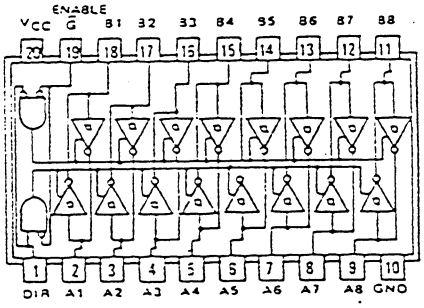
Output Control	Clock	D	HD74HC374 Q	HD74HC534 $\overline{Q}$
L	↑	H	H	L
L	↑	L	L	H
L	L	X	No Change	No Change
H	X	X	Z	Z

X : Don't Care
Z : High Impedance

LS5640

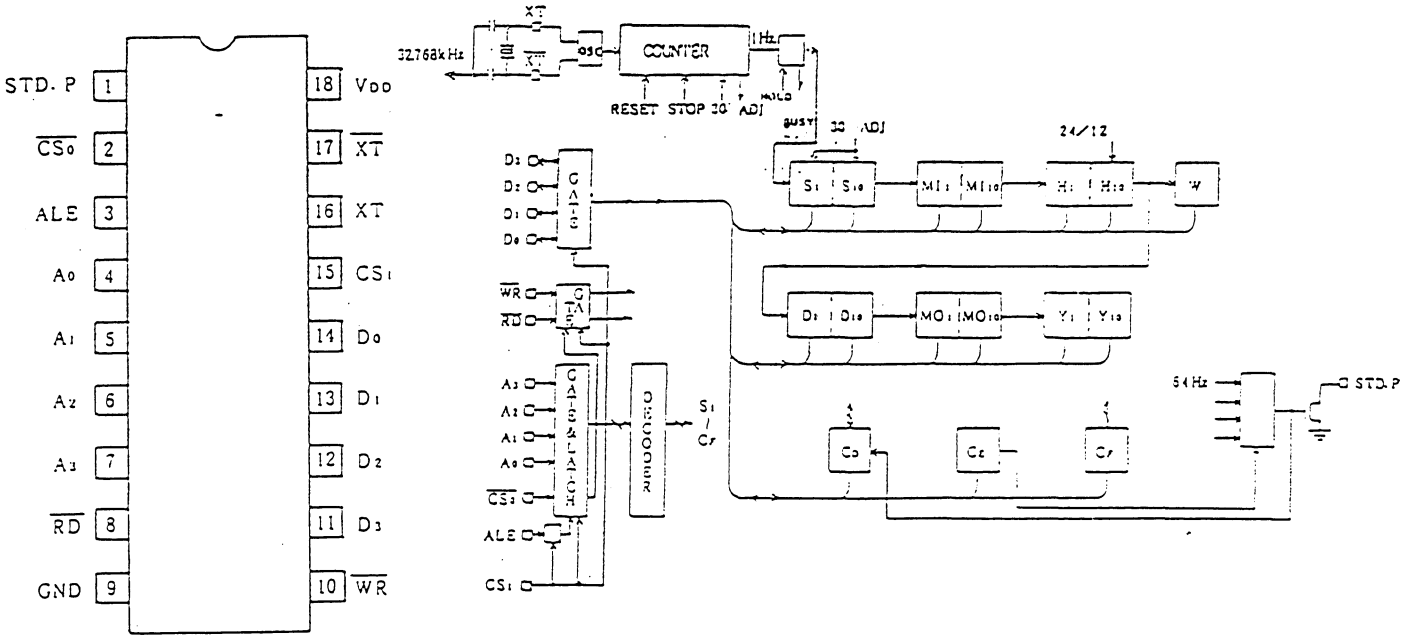
Inverted 3-State Outputs

OCTAL BUS TRANSCEIVERS



SN54LS640 (J) SN74LS640 (J, N)
SN54LS642 (J) SN74LS642 (J, N)

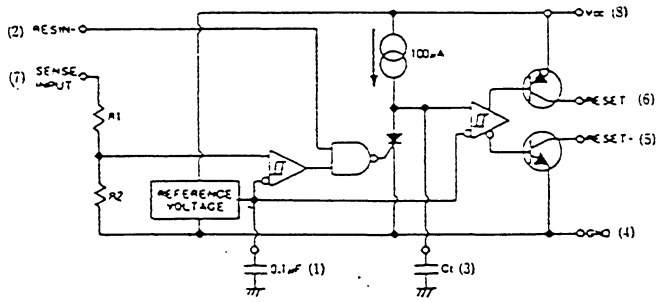
MSM6242RS

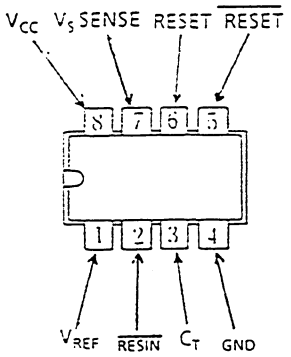


TL7705A/7705-B

5V Power Supervisor

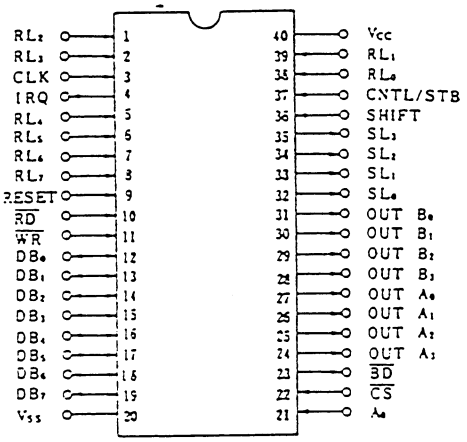
[BLOCK DIAGRAM]





uPD8279C/D-2

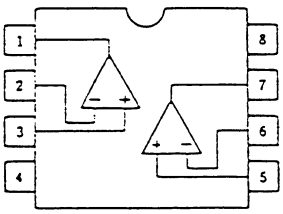
Programmable keyboard/Display Controller

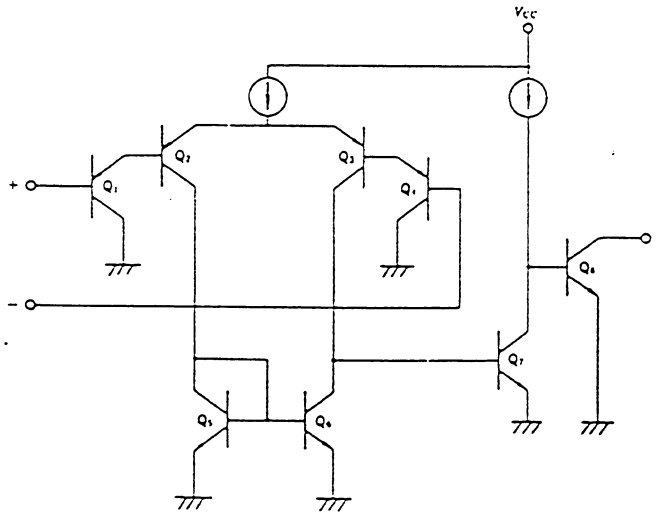


CLK	: Clock Input	RL_{0-7}	: Return Lines
RESET	: Reset Input	SHIFT	: Shift Input
$\overline{CS}$	: Chip Select	CNTL/STB	: Control/Strobe Input
$\overline{RD}$	: Read Input	$OUTA_{0-3}$	: Display (A) outputs
$\overline{WR}$	: Write Input	$OUTB_{0-3}$	: Display (B) outputs
A_0	: Buffer Address	$\overline{BD}$	: Blank Display output
IRQ	: Interrupt Request output	DB_{0-7}	: Data Bus:Bi-Directional)
SL_{0-3}	: Scan Lines		

HA7903

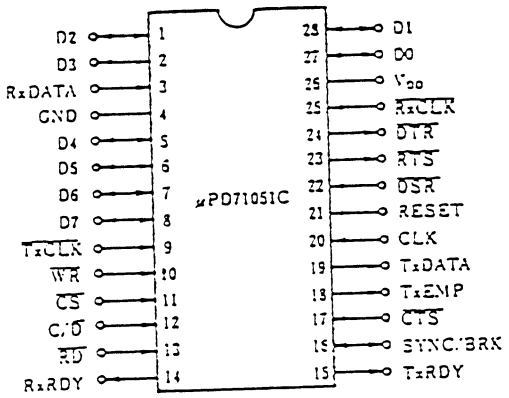
Dual Comparators





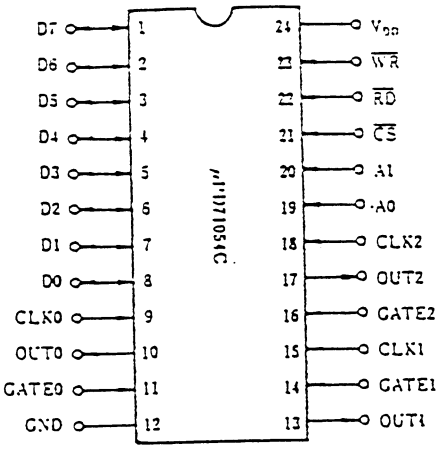
uPD71051C

Serial Interface Controller



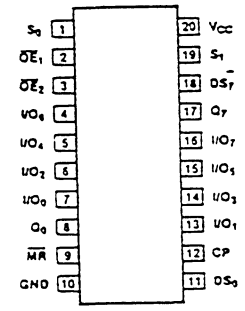
uPD71054C

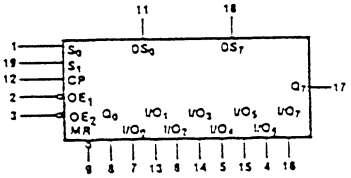
Programmable Interval Timer



54/74F299

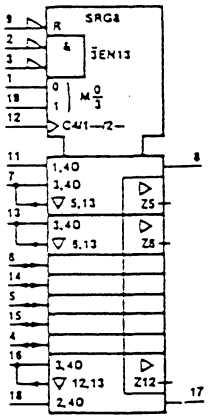
8-Input Universal Shift/Storage Register (3-state)





V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL (IEEE/IEC)



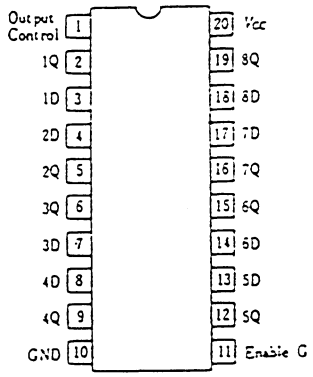
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

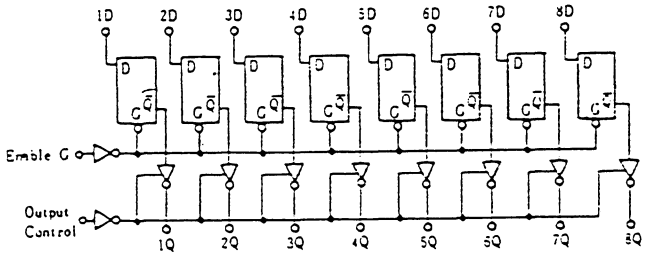
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA0.6mA
DS_0	Serial Data Input for Right Shift	1.0/1.0	20μA/0.6mA
DS_7	Serial Data Input for Left Shift	1.0/1.0	20μA/0.6mA
S_0, S_1	Mode Select Inputs	1.0/2.0	20μA/1.2mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20μA/0.6mA
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)	1.0/1.0	20μA/0.6mA
I/O_0, I/O_7	Parallel Data Inputs or 3-State Parallel Outputs	1.0/1.0 150/33	20μA/0.6mA 3.0mA/20mA
Q_0, Q_7	Serial Outputs	50/33	1.0mA/20mA

NOTE
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

HD74HC373

Octal D-Type Transparent Latches (with Inverted 3-state Outputs)



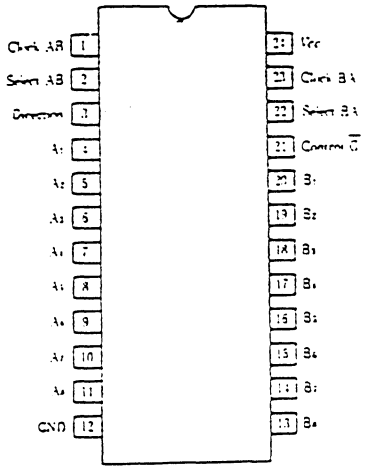


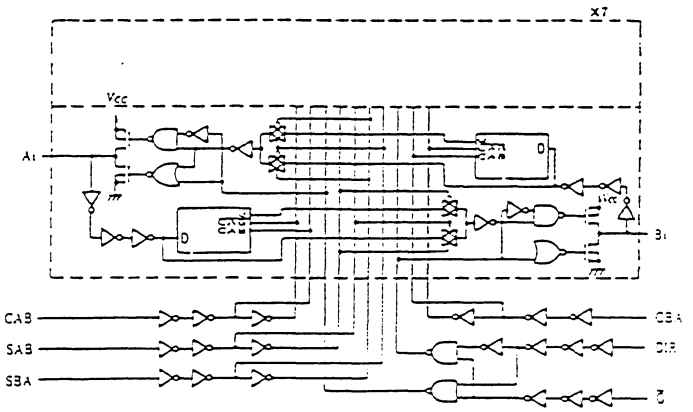
Output Control	Enable G	D	HD74HC373 Q	HD74HC533 $\overline{Q}$
L	H	H	H	L
L	H	L	L	H
L	L	X	No Change	No Change
H	X	X	Z	Z

X : Don't Care
Z : High Impedance

HD74HCT646

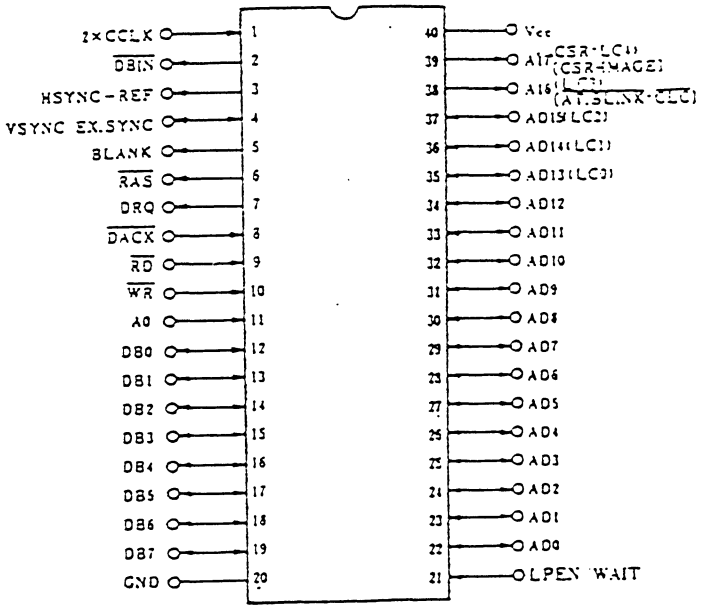
Dual Direction Buffer





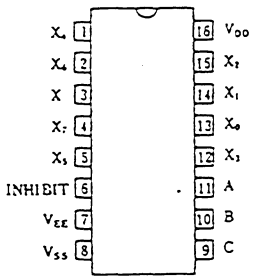
uPD7220AD-2

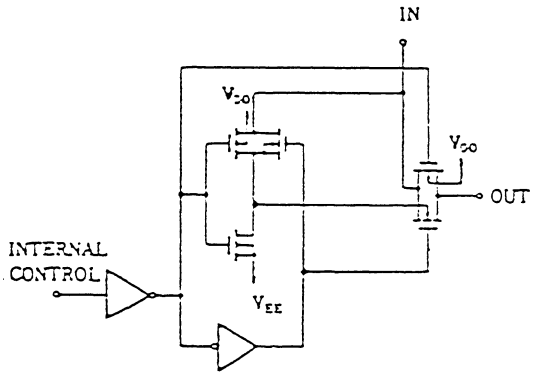
Graphic Display Controller



4051

8-Channel Analog Multiplexer/Demultiplexer

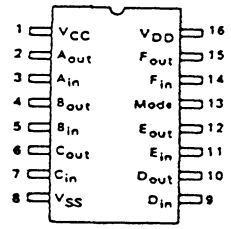




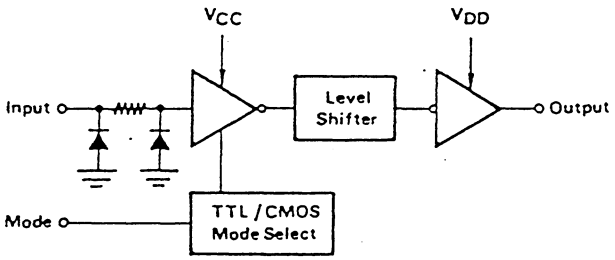
4504

Hex Level Shifters for TTL To CMOS or CMOS To CMOS

PIN ASSIGNMENT



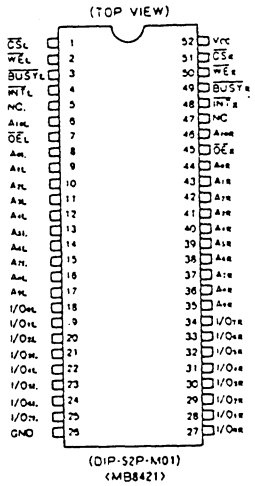
LOGIC DIAGRAM

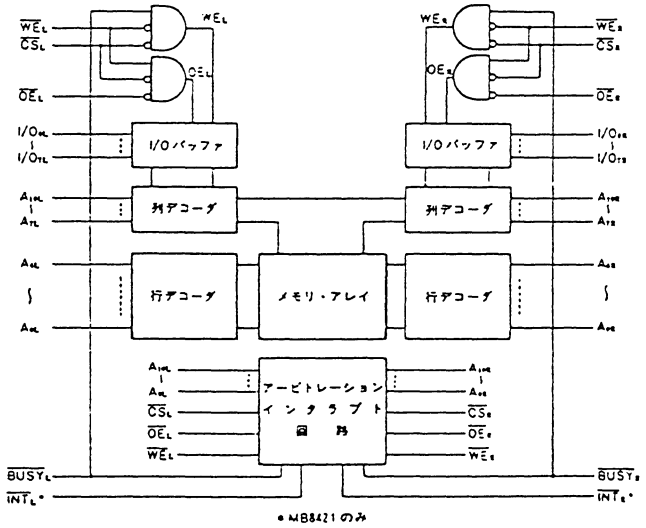


Mode Select	Input Logic Levels	Output Logic Levels
1 (V_{CC})	TTL	CMOS
0 (V_{SS})	CMOS	CMOS

MB8421

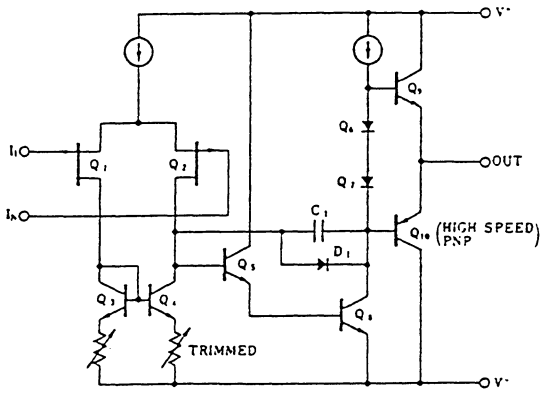
16kbyte Dual Port Static RAM

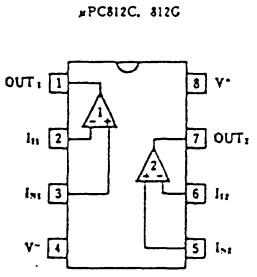




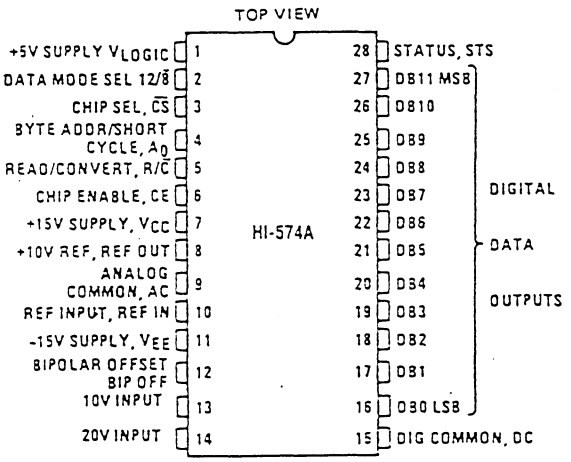
uPC812

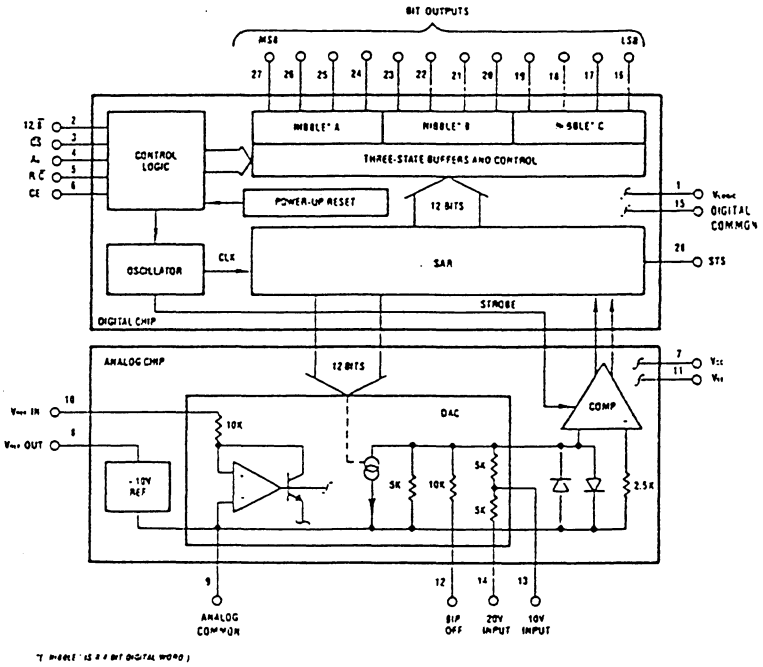
J-FET Input Dual Operational Amplifier





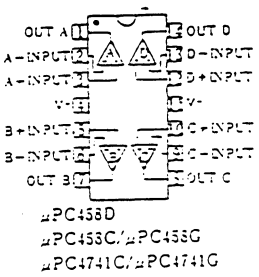
Fast, Complete 12-Bit A/D Coverter with Microprocessor Interface





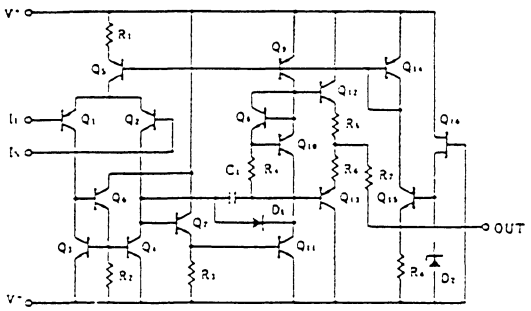
uPC458

Quad Low Noise Operational Amplifier



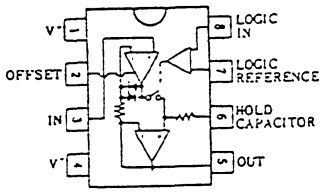
μPC458D
μPC458C/μPC458G
μPC4741C/μPC4741G

Equivalent Circuit (1/4)

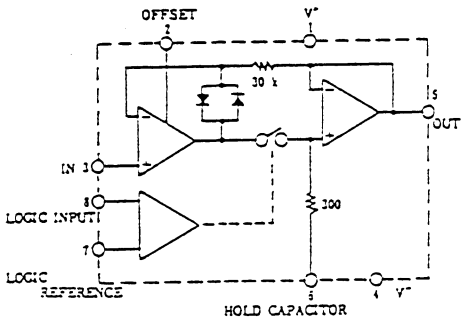


uPC649

Sample and Hold cicuit



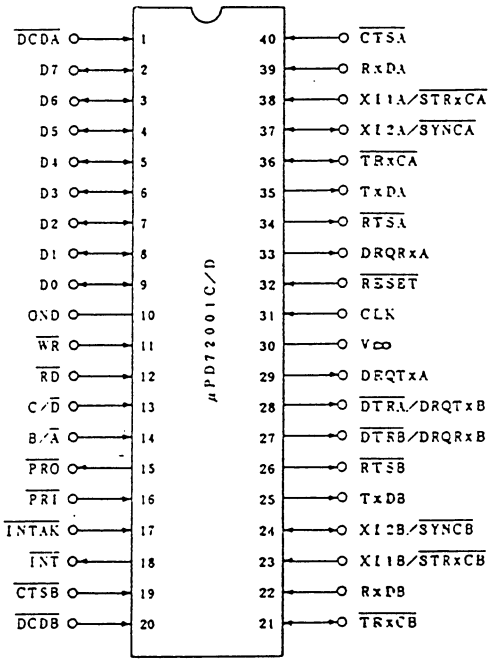
Block Diagram



uPD72001

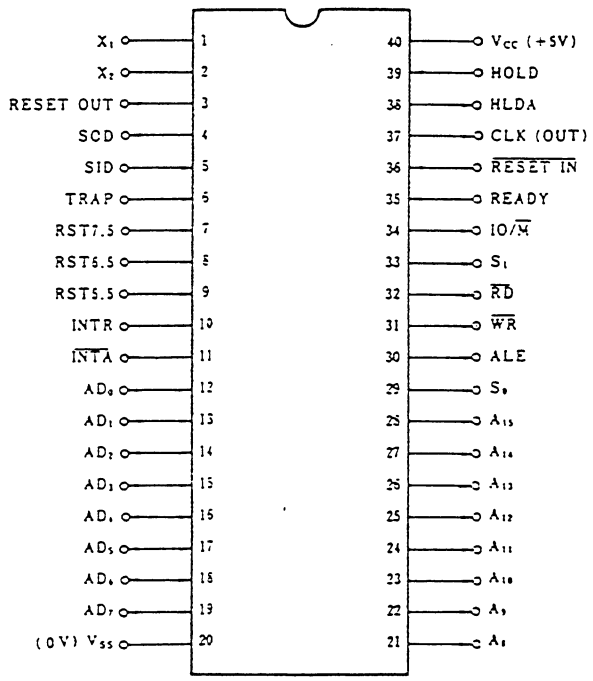
AMPSC (Advanced Multi-Protocol Serial Controller)

(Top View)



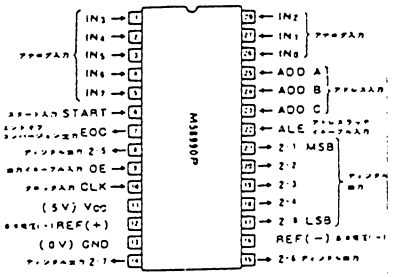
80C85A

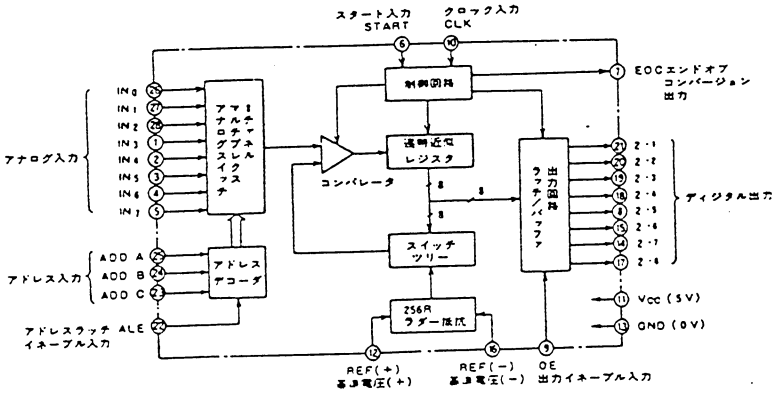
Single Chip 8-Bit CMOS Microprocessor



M58990P

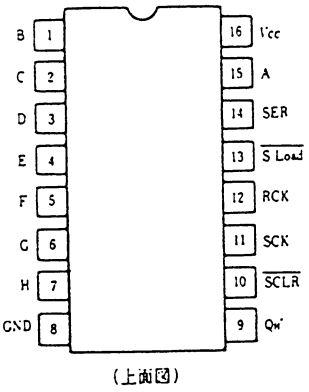
8 Bit 8-Channel A/D Converter



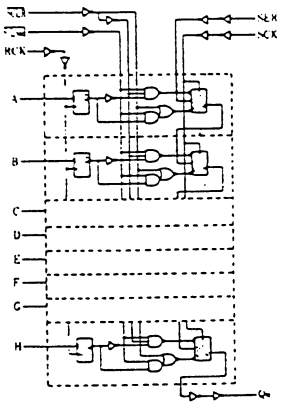


HC597

8 Bit Latch/Shift Register

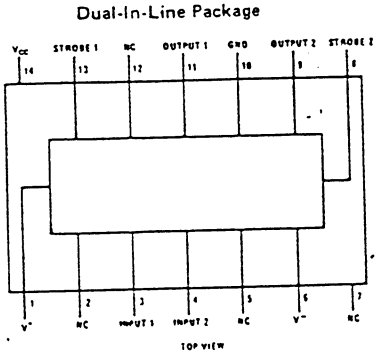


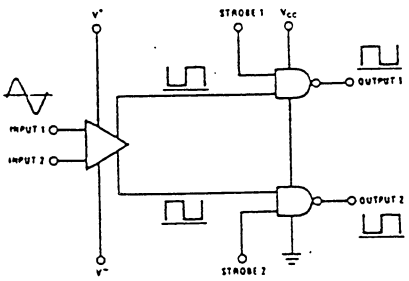
(上面図)



LM361

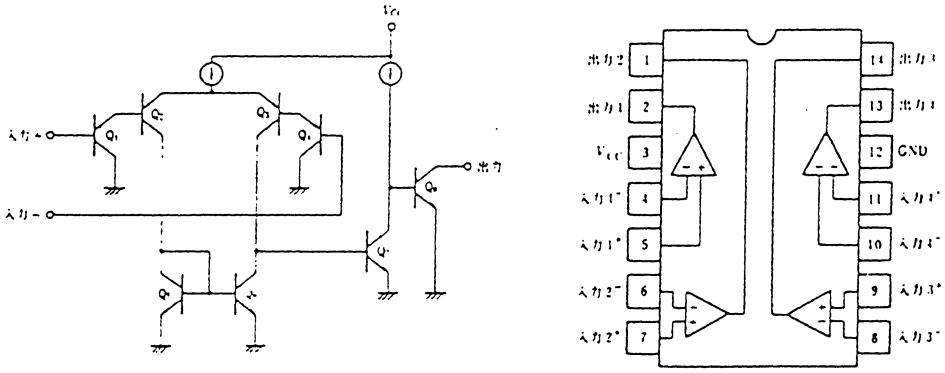
High Speed Differential Comparator





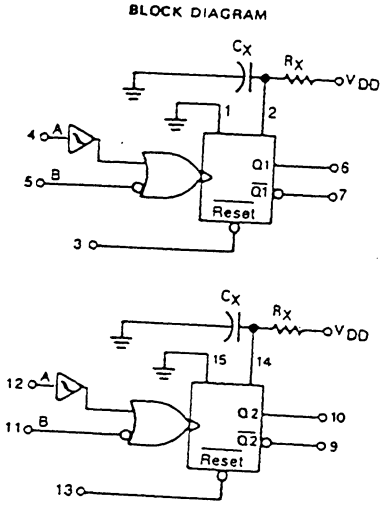
HA17901

Quad Comparators



14538

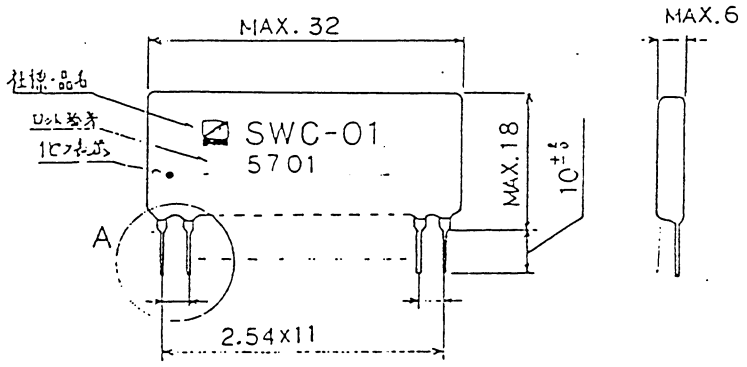
Dual Precision Retriggerable/Resettable Monostable multivibrator



R_X and C_X are external components.
V_{DD} = Pin 16
V_{SS} = Pin 8, Pin 1, Pin 15

SWC-01

Switching Regulator Controller (Hybrid)



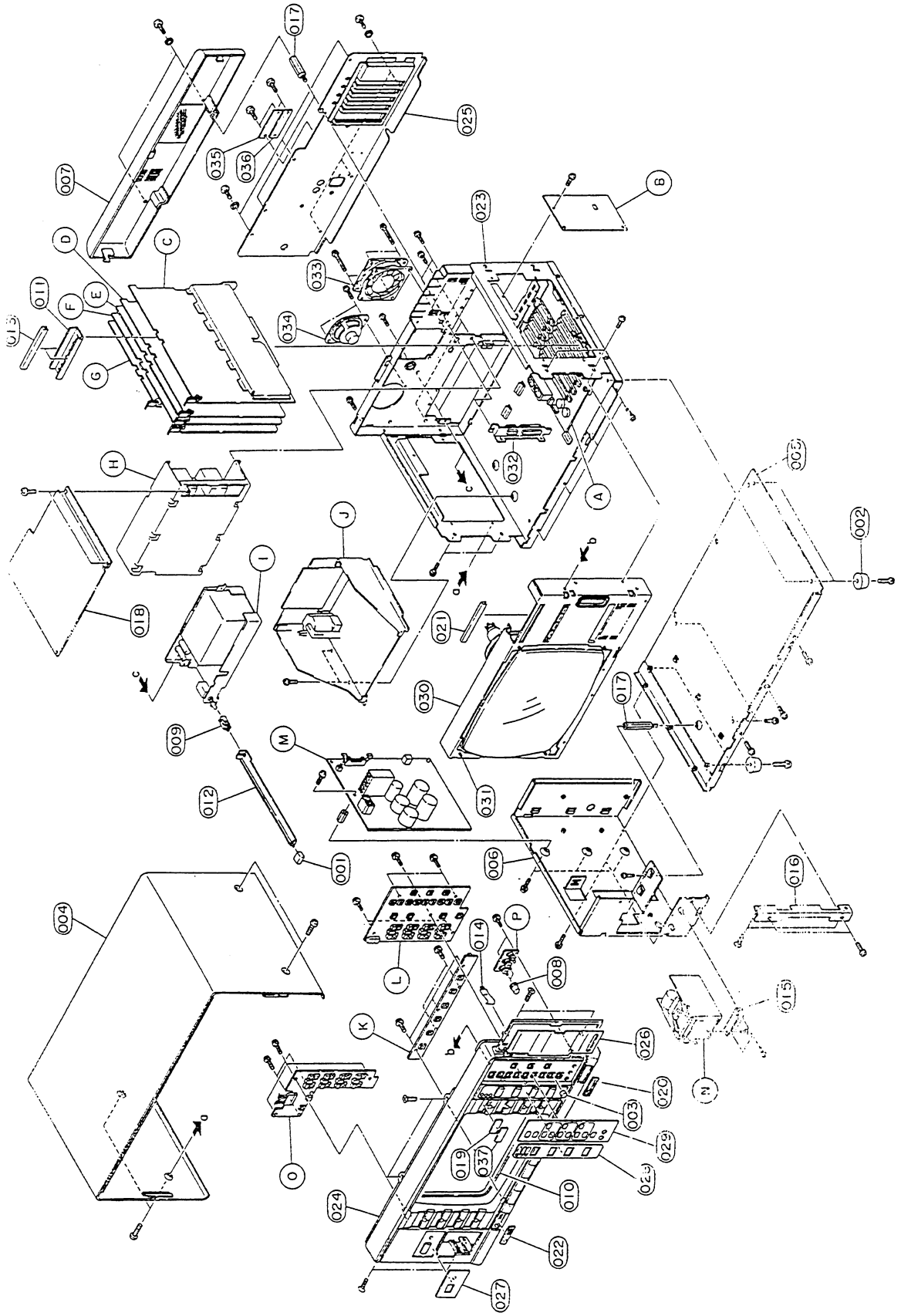
Section 10

10. Mechanical part list

Mechanical part list

MU-820RA/J/K

Index	Code No.	Description
1	5690306	Switch knob BS15-01 ivory
2	6000435	Rubber foot (with washer) K-30, 30-dia
3	6003316	Magnet HICOREX-18B-503
4	1112-016432A	CNS cover
5	1112-016441A	Bottom chassis-1
6	1112-016593A	Recorder unit chassis
7	1113-052498A	Rear cover
8	1114-154858	VR touch knob
9	1114-171795B	Switch holder
10	1114-179323A	CRT sponge
11	1114-179341A	PC board holder
12	1114-179359D	Extension shaft
13	1114-179403	U-shape rubber
14	1114-181204A	Front grounding spring
15	1114-196278	Recorder holder
16	1114-200292A	MU-800R reocrder unit coupling bracket
17	1114-200309A	Spacer bolt (31.5L)
18	1114-202896	Enforcement plate
19	1114-202922	CNS name sheet under panel
20	1124-013368	NK name plate-3
21	1124-036067B	Color indication sheet
22	1124-038813	CNS switch panel
23	1142-000633A	Chassis assembly
24	1142-000678A	Front frame assembly
25	1122-006219	CND rear plate A (MU-820RA)
	1123-017972	CNS rear plate K (MU-820RJ/K)
26	1123-017624A	CNS inside door panel A
27	1124-038172B	Recorder operatio panel A
28	1124-038831A	CNS operation panel A
29	1143-006037B	CNS sheet panel assembly
30	1112-017387	CNS front chassis
31	1114-179332A	CRT spacer
32	1114-200327	Connector holder (IO)
33	4840352	Fan motor FBH-08A12M
34	4700601	Speaker EAS-65P34S 160 ohm
35	1194-007724	CNS-8200A name plate 5B
	1194-007867	CNS-8200J name plate 5B
	1194-007858	CNS-8200K name plate 5B
36	1194-007742	MU-820RA name plate 5B
	1194-007876	MU-820RJ name plate 5B
	1194-007849	MU-820RK name plate 5B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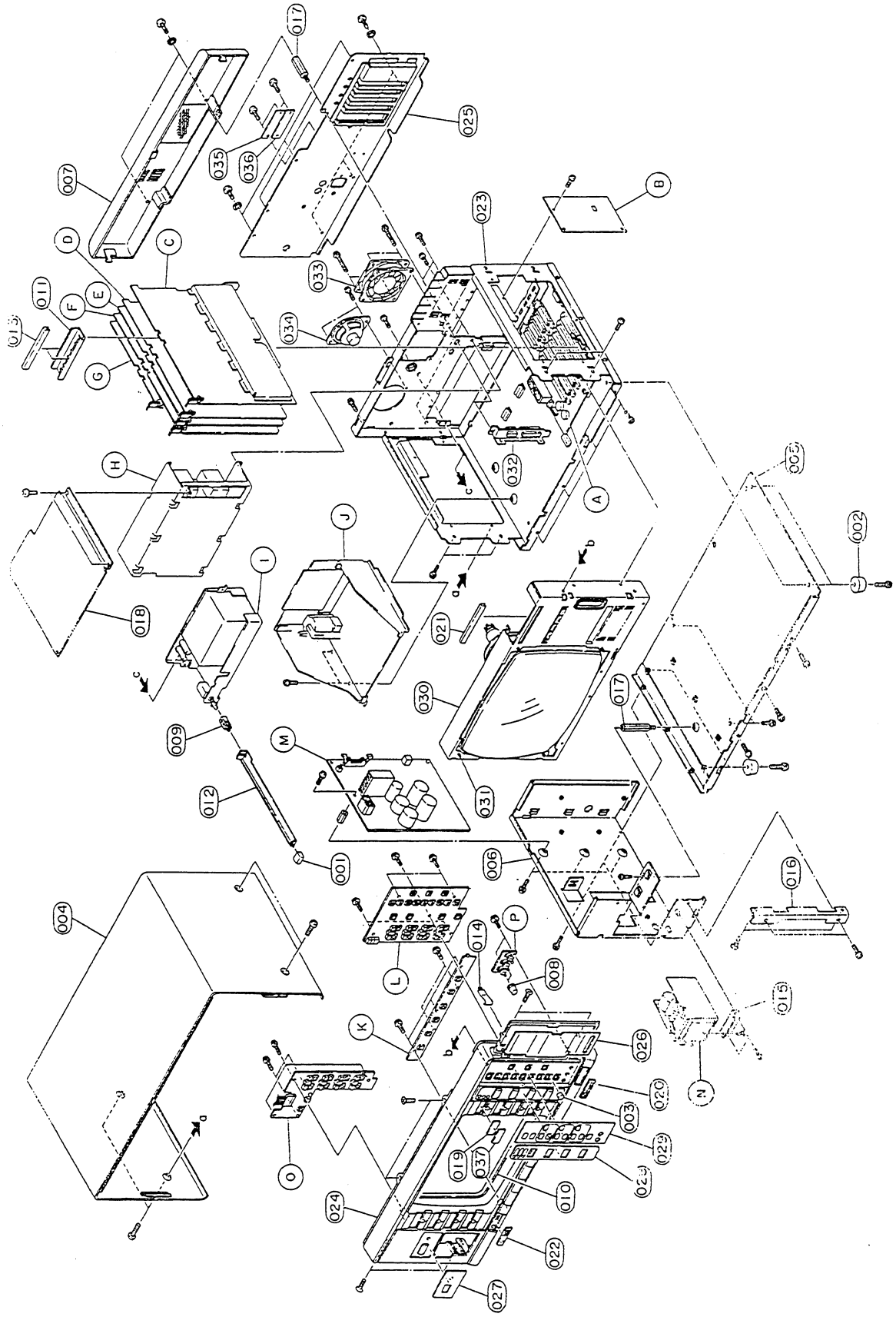
Index	Code No.	Description
A	UP-0539	Mother obard
B	UP-0265	Sound control board
C	UP-0262	CRTC board
D	UP-02602	CPU board
E	UP-0464	AD board
F	UP-0511	REC CNTL board
G	UP-0507	WS/IO board
H	UP-0315	Regulator board
I	SC-001RA	Transformer unit (MU-820RA)
	SC-001RJ	Transformer unit (MU-820RJ)
	SC-001RK	Transformer unit (MU-820RK)
J	VM-003P	CRT unit
K	UP-0564	Operation board2
L	UP-0481	Operation board1
M	UP-0512	REC DRV board
N	RG-712P	Recorder unit
O	UP-0483	Operation board4
P	UP-0482	Operation board3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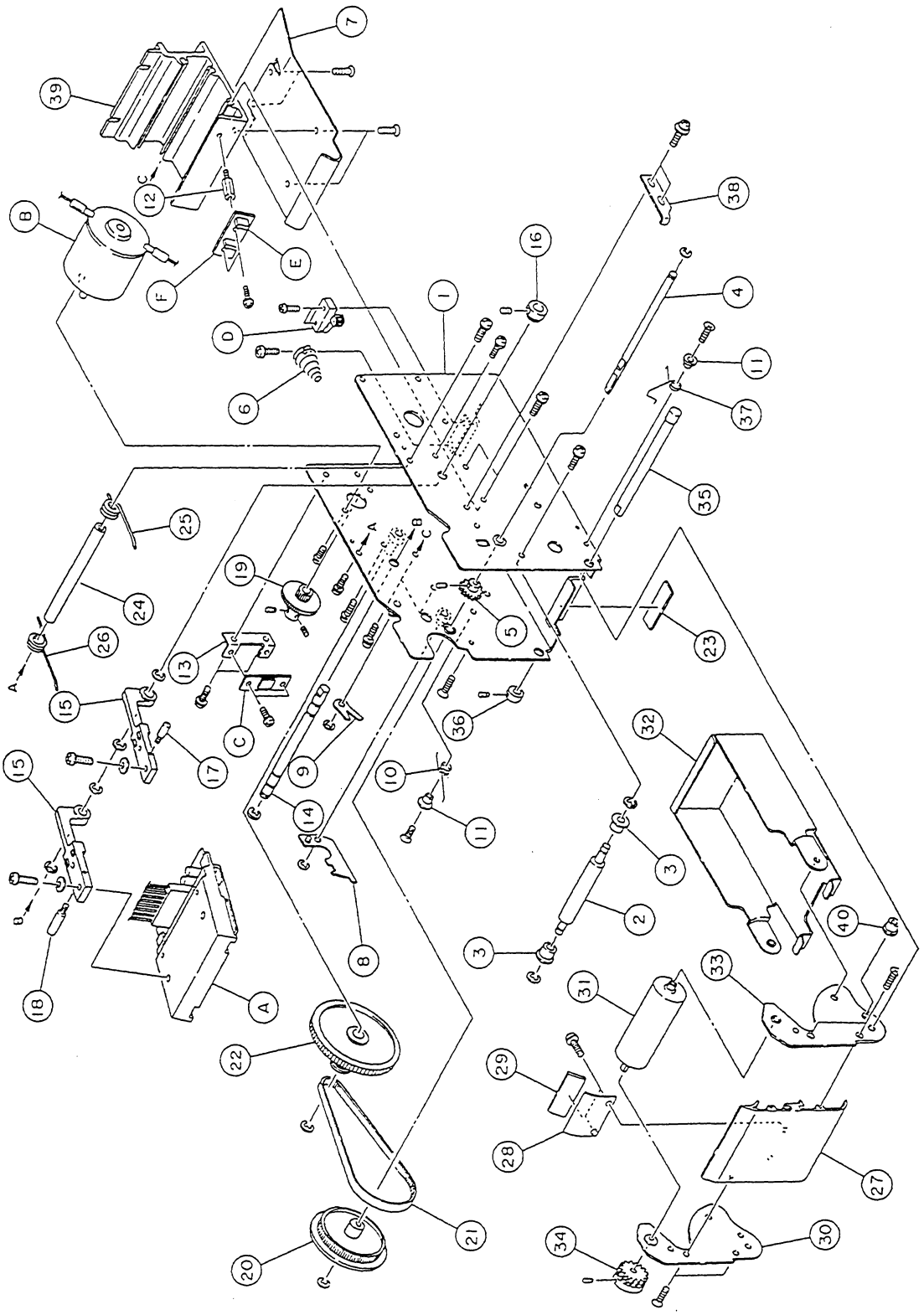
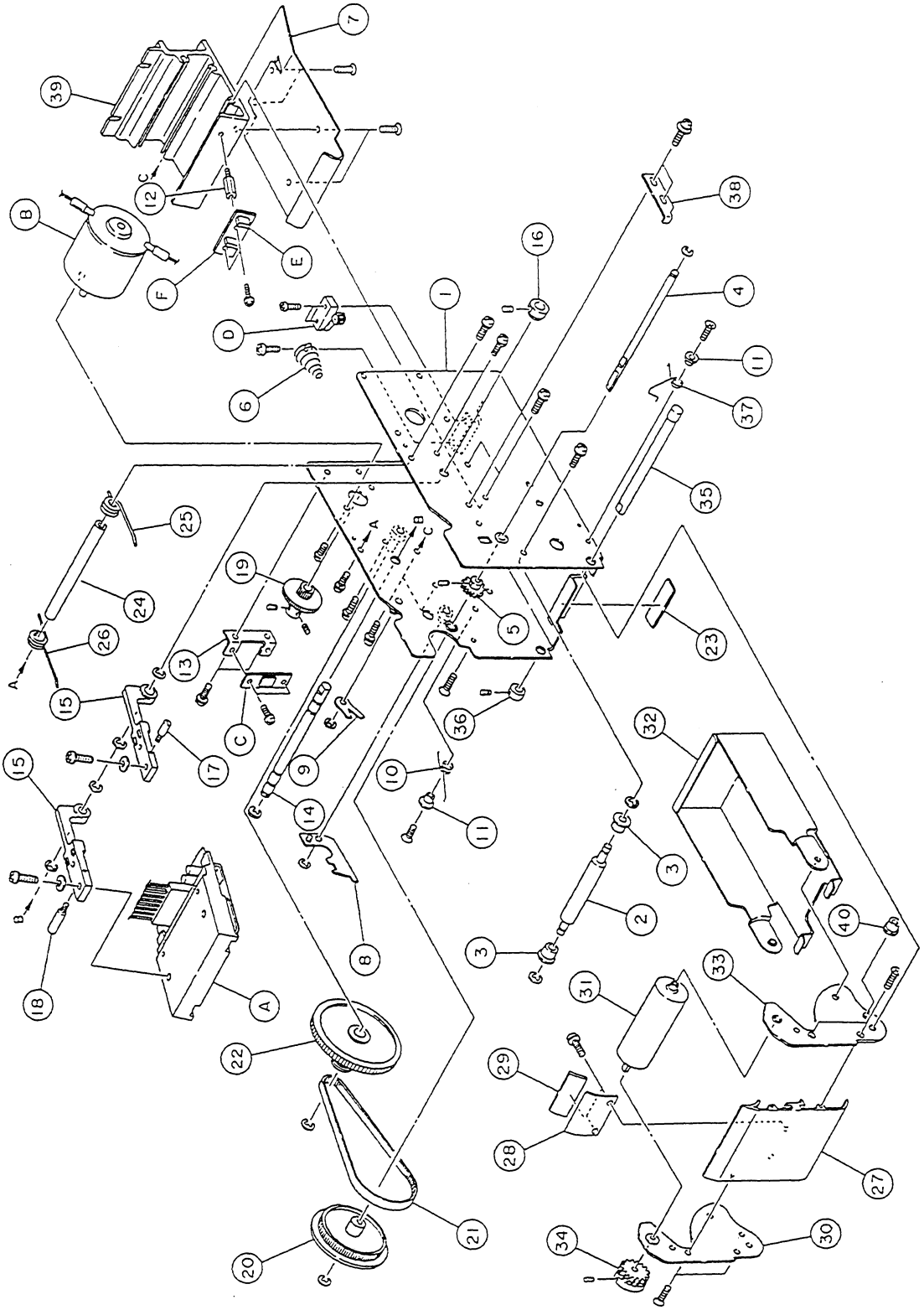
Mechanical part list

RG-712P

Index	Code No.	Description
1	1143-006198	Recorder unit main chassis 1A ASSY
2	1114-170412	Guide shaft 1
3	1114-169878A	Guide flange
4	1114-170395D	Transmission shaft 1
5	1144-012001A	Transmission gear 1 ASSY
6	1114-208738	Magazine release spring 1
7	1114-206678	Guide plate 1
8	1144-011983A	Release lever 2 ASSY
9	1114-169851A	Release arm
10	1114-170038A	Release lever spring 1
11	1114-170074	Magazine stopper spring shaft
12	6491261	Hexagonal socket bolt
13	1114-206713	Sensor mounting plate A
14	1114-170403A	Head rotary shaft 1
15	1114-170029A	Head mounting bracket
16	1114-169922	Head shaft collar
17	1114-170475	Head guide pin 1A
18	1114-170466	Head guide pin 1B
19	1144-014677	Motor gear ASSY
20	1114-170448	Timing pulley 60
21	5903612	B106MXL3.2 BELT
22	1114-170555	Pulley gear 18-108
23	1114-170092C	Cushion rubber
24	1114-206704	Pressure adjusting shaft 1A
25	1114-207062	Pressure spring 1A
26	1114-205955	Pressure spring 1B
27	1123-015573A	Magazine 1
28	1114-170519	Back tension spring
29	1114-170501A	Felt
30	1144-014668	Magazine plate 1B ASSY
31	1114-170386D	Platen roller 1
32	1114-170386D	Paper box 1
33	1144-014686	Magazine plate 1A ASSY
34	1144-012358A	Transmission gear 2 ASSY
35	1114-170484	Magazine rotary shaft 1
36	1114-169913	Magazine shaft collar
37	1114-170047F	Magazine stopper spring
38	1114-206722	Magazine stopper A
39	1113-054184	Main frame
40	1114-199506	Spacer



Index	Code No.	Description
A	1800063	Thermal array head EUX-C18A8HC01
B	4810456	Motor EN35-T107N1B (12V)
C	4790673	Magnetic sensor FP-2R-02
D	3280111	Switch SS-5GLZ
E	0600334	Photo reflector PS6002
F	9521544	Board 9521544



Section 11

11. Electrical part list

		Page
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CD-023P	Chassis	11-3
RG-712P	Recorder unit	11-3
UP-0262	CRTC board	11-4
UP-0265	Sound control board	11-6
UP-0315	Regulator unit	11-7
UP-0464	AD board	11-8
UP-0481	Operation board, main	11-11
UP-0482	Operation board, VR	11-12
UP-0483	Operation board, left	11-12
UP-0507	WS/IO board (QI-809P)	11-12
UP-0511	REC CNTL board	11-13
UP-0512	REC DRV board	11-15
UP-0539	Mother board	11-17
UP-0564	Operation board, bottom	11-17
YS-009P0	CNS-JJW connection cable	11-20
YS-009P1	CNS-JJS connection cable	11-20
SC-001RA	Transformer unit	11-20
SC-001RJ	Transformer unit	11-21
SC-001RK	Transformer unit	11-21
UP-0372	CRT PWB board	11-22
UP-03731	CRT MAIN PWB board	11-22
VM-003P	CRT unit	11-24

Abbreviations

CN CONNECTOR

ACN	Square
ACN1	Square, plug
ACN2	Square, receptacle
BCN	Card edge
CCN	Round
CCN1	Round, plug
CCN2	Round, receptacle
CN	Coaxial plug or other types
CORD	Accessory cord
NCN	Nylon connector and pins
PCN	For use on PC board, short plug, terminal board

C CAPACITOR

MPC	Metallized fim
OFC	Oil
TAC	Tantalum
TC02	Tantalum, tubelar
TC04	Tantalum, vertical
VC	Variable
C	Barium titanate, paper, etc.
CEC1	Ceramic, withstanding voltage; <100V
CEC2	Ceramic, withstanding voltage; ≥100V
CM	Module
ECB	Electrolytic, block
CE02	Electrolytic, tubelar
CE04	Electrolytic, vertical
FLC	Plastic film, ±5%
FLCB	Plastic film, block
FLC1	Plastic film, vertical
FLC2	Plastic film, tubelar
MCC	Mica

D DIODE

D	Diode, array, for small signal
DB	Block, power, bridge
DP	Power, silicon diode, etc.
LCD	Liquid crystal idsplay
LED	Light emitting diode, LED array
LEDC	LED charactor
SCR	Silicon controlled rectifier(SCR, thyristor)
ZD1	Zenor, ≤5V
ZD2	Zenor, ≤10V
ZD3	Zenor, ≥10V

IC INTEGRATED CIRCUIT

ADIC	A/D or D/A converter
AIC	Analog (log. amp., comparator, switch, sample & hold etc.)
CPU	CPU, CPU peripheral device; (RAM, I/O port, etc.)
DIC	Digital (timer, NMOS, PMOS, registor, etc.)
MIC	CMOS
OPIC	Operational amp. buffer amp., etc
REG	Regulator
TIC	TTL

Q TRANSISTOR

TR	Uni-junction, etc.
TRA	Type 2SA; PNP, high speed
TRB	Type 2SA; PNP, low speed
TRC	Type 2SC; NPN, high speed
TRD	Type 2SD; NPN, low speed
TRP	Photo-electric device, photo-fiber, etc.
FET	FIELD EFFECT TRANSITOR
FET	Type 3SK/3SJ(dual gate, N-ch/P-ch)
FETJ	Type 2SJ (mono gate, P-ch)
FETK	Type 2SK (mono gate, N-ch)

SW SWITCH

ATT	Attenuator
DSW	Digital
PSW1	Push button, 1 button type
"	" " , " "
PSW9	Push button, 9 button type
PSW0	Push button, 10 button type
RSW	Rotary
SW	Micro, DIP, Toggle(tumbler), disc, etc.

T TRANSFORMER

CH	Choke coil
FBTF	Flyback
L	Inductance(coil)
MATF	Matching (IPTF, OPTF, IFTF)
PLTF	Pulse, oscillation TF
PT	Power(except for switching purpose)
T	High voltage, differential, HV unit, power supply, etc.
YOKE	Deflecting yoke

MOTOR

ACMO	AC (including gear head)
DCMO	DC (including gear head)
FAMO	Fan
PUMO	Pulse step (with gear head)

TUBE

CRT	Cathode ray tube
GA	Gas arrestor
NE	Neon tube, neon discharge tube
TUBE	Vacuum tube

R RESISTOR

RM	R module(including R and C)

RV VARIABLE RESISTOR

POT	Potentiometer
TPOT	Potentiometer on PCB, >15mm in dia.
TVR1	Carbon on PCB
TVR2	Carbon on PCB
TWVR	Wirewound on PCB
VR	On panel
VR1	On panel, <30mm in dia.
VR2	On panel, ≥30mm in dia.
WVR	Wirewound, large current

MISCELLANEOUS

GAGE	Gauge
METR	Meter, digital meter, manometer, electromagnetic counter, etc.
PRB	Pick-up, microphone, ultrasonic probe, etc.
SP	Speaker, headphone, earphone, buzzer, etc.
TD	Transducer, galvanometer coil, pressure meter, differential pressure meter
THP	Thermal/temperature sensor/probe, thermometer, etc.
SOCK	Socket, cap
FH	Fuse holder
FUSE	Fuse
TERM	Terminal, lug board, etc.
BUS	Bus bar
LAMP	Lamp. bracket
BATT	Battery, battery holder, recharger, etc.
UNIT	Display/recorder/printer/disc-drive unit, etc.
MD	Module, unit, hybrid IC, etc.
TH	Line filter, thermistor, varistor, CdS, etc.
RY	Relay, reed relay, solenoid relay
ANT	Antenna
XTAL	Crystal
HEAD	Thermal head/array, discharge head/array
VALV	Valve, electomagnetic valve,

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
CD-023P Chassis				
CD-023P		4700601	1	SP EAS-65P34S 16OHM
CD-023P		367719	1	FAMO ASF82371
CD-023P		5416185	1	NCN MLP-03
CD-023P		5416194	3	NCN SLF-01T-1.3
CD-023P		5425977	1	PCN HIF3A-20D-AC(50)
CD-023P		5426646	1	PCN HKP-20FS02-10BT(30)
CD-023P		5426833	1	PCN HKP-26FS02-13BT(50)
CD-023P		5427298	1	PCN M62-06-3035SA
CD-023P		5427467	1	PCN M62-12-3039SA
CD-023P		5427592	1	PCN M62-03-0003SA
CD-023P		5428243	1	PCN M62M83-02
CD-023P		5428252	2	PCN M62C84-4 SOCKET CONTACT
CD-023P		5429438	1	PCN HIF3A-30D-AC(20)
CD-023P		5429447	1	PCN M62-03-0003SA1
CD-023P		5501271	1	CORD Regulator Unit Connection Cord
CD-023P		5501289	1	CORD CRT Unit Connection Cord1
CD-023P		5501298	1	CORD CRT Unit Connection Cord2
CD-023P		5501948	1	CORD CNS WS Power Cord
CD-023P		5502056	1	CORD W1-88692-0 Connection Cable
CD-023P		5502261	1	CORD F3BA-FDED-10D-9F
CD-023P		5551831	1	PCN HKP-6FS02-3BT(50)
RG-712P Recorder unit				
RG-712P		1800063	1	HEAD EUX-C18A8HC01
RG-712P		4790673	1	TD Magnetic Sensor FP-2R-02
RG-712P		4810456	1	DCMO EN35-T107N1B (12V)
RG-712P	CNJ201	5426771	1	PCN HKP-14FS02-7BT(60)
RG-712P	IC201-IC202	0600236	2	TRP NJL5142EL-A Photoreflector
RG-712P	SW201	3280111	1	SW SS-5GL2

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-0262 CRTC board				
UP-0262	CN101	5427939	1	PCN PCN10EA-90P-2.54DS(05)
UP-0262	C101-C124	4317516	24	CEC1 TP D55Y5V1H 103Z 5-W
UP-0262	C125	3801717	1	ECO2 ECEB1CG101S 100uF/16V
UP-0262	C601	4315367	1	FLC1 ECQ-V 1H 334JZ3 (0.33uF)
UP-0262	IC101-IC102	1303822	2	MIC uPD74HCT640C
UP-0262	IC103-IC104	1303769	2	MIC uPD74HCT240C
UP-0262	IC105	1303778	1	MIC uPD74HCT244C
UP-0262	IC106	1303742	1	MIC HD74HCT138P
UP-0262	IC110	1303742	1	MIC HD74HCT138P
UP-0262	IC111	1302966	1	MIC uPD74HC30C(HD74HC30P)
UP-0262	IC112	1202405	1	TIC SN74LS00N
UP-0262	IC113	1203021	1	TIC SN74LS109
UP-0262	IC114	1206562	1	TIC 74F175PC(N74F175N)
UP-0262	IC115	1202405	1	TIC SN74LS00N
UP-0262	IC116	1205117	1	TIC 74F08PC
UP-0262	IC117	1202414	1	TIC SN74LS02N
UP-0262	IC118	1202566	1	TIC SN74LS157N
UP-0262	IC119	1203146	1	TIC SN74LS139
UP-0262	IC120	1303742	1	MIC HD74HCT138P
UP-0262	IC121	1205518	1	TIC 74F00PC 2INPUT NAND
UP-0262	IC122	1202762	1	TIC SN74LS32
UP-0262	IC123	1202637	1	TIC SN74LS03
UP-0262	IC201	1206464	1	CPU uPD7220AD-2
UP-0262	IC202	1205135	1	TIC 74F74PC
UP-0262	IC203	1205144	1	TIC 74F163APC
UP-0262	IC204	1206562	1	TIC 74F175PC(N74F175N)
UP-0262	IC206-IC207	1205135	2	TIC 74F74PC
UP-0262	IC208-IC209	1303796	2	MIC HD74HCT373P
UP-0262	IC210-IC213	1206473	4	CPU MB84256-10LP-G
UP-0262	IC214	1205126	1	TIC 74F32PC
UP-0262	IC215	1206535	1	TIC 74F109PC(N74F109N)
UP-0262	IC216-IC217	1205189	2	TIC 74F299PC
UP-0262	IC218	1206562	1	TIC 74F175PC(N74F175N)
UP-0262	IC219-IC220	1205135	2	TIC 74F74PC
UP-0262	IC221-IC222	1206571	2	TIC N74F245N(74F245PC)
UP-0262	IC223	1205126	1	TIC 74F32PC
UP-0262	IC225	1203895	1	TIC SN74LS393
UP-0262	IC226	1205117	1	TIC 74F08PC
UP-0262	IC227	1205108	1	TIC 74F04PC
UP-0262	IC229	1205527	1	TIC 74F02PC 4-2INPUT NOR

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-0262	IC301-IC302	1303831	2	MIC	HD74HCT646P
UP-0262	IC303	1206553	1	TIC	N74F162AN(74F162APC)
UP-0262	IC304-IC305	1205144	2	TIC	74F163APC
UP-0262	IC306-IC307	1206482	2	CPU	MB8464A-80LP-G
UP-0262	IC308-IC310	1206277	3	TIC	74F157
UP-0262	IC311-IC312	1303804	2	MIC	uPD74HCT374C
UP-0262	IC313	1206562	1	TIC	74F175PC(N74F175N)
UP-0262	IC314	1205518	1	TIC	74F00PC 2INPUT NAND
UP-0262	IC315	1205117	1	TIC	74F08PC
UP-0262	IC316	1206535	1	TIC	74F109PC(N74F109N)
UP-0262	IC317	1303074	1	MIC	uPD74HC4040C(HD74HC4040P)
UP-0262	IC320	1205135	1	TIC	74F74PC
UP-0262	IC321	1205108	1	TIC	74F04PC
UP-0262	IC322	1205189	1	TIC	74F299PC
UP-0262	IC323	1206295	1	TIC	74F194
UP-0262	IC324	1206179	1	TIC	74F20
UP-0262	IC325	1205153	1	TIC	74F164PC
UP-0262	IC401	1206428	1	CPU	MSD1206428 ADDR CNTL
UP-0262	IC402-IC404	1206473	3	CPU	MB84256-10LP-G
UP-0262	IC407-IC409	1303787	3	MIC	HD74HCT245P
UP-0262	IC501	1206437	1	CPU	MSD1206437 WAVE COMP
UP-0262	IC505-IC506	1206295	2	TIC	74F194
UP-0262	IC601	1303804	1	MIC	uPD74HCT374C
UP-0262	IC602	1206517	1	TIC	SN74S05
UP-0262	IC603	1203895	1	TIC	SN74LS393
UP-0262	IC604	1205518	1	TIC	74F00PC 2INPUT NAND
UP-0262	IC605	1205554	1	TIC	74F151PC MPX
UP-0262	Q601	4335069	1	TRC	2SC1213AKDTZ
UP-0262	Q602-Q605	0302451	4	TRC	2SC1730
UP-0262	RA101-RA114	4093436	14	RM	EXB-F9E-104
UP-0262	RA116	4093436	1	RM	EXB-F9E-104
UP-0262	RA117	4093124	1	RM	EXB-F9E 472J 4.7KOHM
UP-0262	SK101-SK103	5422846	3	SOKT	IC SOCKET DL-2-28A (01)
UP-0262	SK201	5422605	1	SOKT	IC SOCKET DL-2-40A (01)
UP-0262	SK301-SK302	5601359	2	SOKT	SIC01-064-361T
UP-0262	VC101	3890469	1	VC	TZ03R 300ER 5.2-30pF
UP-0262	X101	1752676	1	XTAL	TD308C(XC0-B) 64M

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-0265 Sound control board				
UP-0265	CN101	5427877	1	PCN PCN10EA-20P-2.54DS(05)
UP-0265	C001	4312503	1	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0265	C002-C008	4317525	7	CEC1 TP D55Y5V1H 104Z 5-W
UP-0265	C009-C010	4312503	2	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0265	C014	4317525	1	CEC1 TP D55Y5V1H 104Z 5-W
UP-0265	C101-C102	4315242	2	FLC1 ECQ-V 1H 333JZ3 (0.033uF)
UP-0265	C103	4315367	1	FLC1 ECQ-V 1H 334JZ3 (0.33uF)
UP-0265	C104	4315242	1	FLC1 ECQ-V 1H 333JZ3 (0.033uF)
UP-0265	C105	3801717	1	EC02 ECEB1CG101S 100uF/16V
UP-0265	C106-C107	3814089	2	TC02 STH1A4R7M 10V4.7uF
UP-0265	C108	4317579	1	CEC2 DD05-989SL 470K500 (47pF)
UP-0265	C109	4312503	1	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0265	C110	4315304	1	FLC1 ECQ-V 1H 104JZ3 (0.1uF)
UP-0265	C111-C112	4315269	2	FLC1 ECQ-V 1H 473JZ3 (0.047uF)
UP-0265	C113	4315162	1	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0265	C114-C116	4315304	3	FLC1 ECQ-V 1H 104JZ3 (0.1uF)
UP-0265	C117	4315162	1	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0265	C118	4315304	1	FLC1 ECQ-V 1H 104JZ3 (0.1uF)
UP-0265	C119	4317597	1	CEC2 DD05-989B 101K500 (100pF)
UP-0265	C120	4315304	1	FLC1 ECQ-V 1H 104JZ3 (0.1uF)
UP-0265	C121-C122	4312503	2	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0265	C123	3801717	1	EC02 ECEB1CG101S 100uF/16V
UP-0265	C124	4317552	1	CEC2 DD05-989SL 220K500 (22pF)
UP-0265	C125-C126	3801717	2	EC02 ECEB1CG101S 100uF/16V
UP-0265	C127	4317552	1	CEC2 DD05-989SL 220K500 (22pF)
UP-0265	C128-C129	4315206	2	FLC1 ECQ-B 1H 223JZ3 0.022uF
UP-0265	D101	4325089	1	ZD2 HZ5C1TE (4.9-5.1V)
UP-0265	D102	4320031	1	D 1S2076ATE
UP-0265	D103	1090276	1	ZD1 HZ2C1
UP-0265	IC101-IC102	1203333	2	TIC SN74LS174
UP-0265	IC103	1302957	1	MIC HD74HC14P(uPD74HC14C)
UP-0265	IC104-IC105	1301601	2	MIC HD14538BP (MC14538BCP)
UP-0265	IC106	1300638	1	MIC HD14053BP(MC14053BCP)
UP-0265	IC107	1252841	1	DIC Melody IC 7910I
UP-0265	IC108	1302939	1	MIC HD74HC04P(uPD74HC04C)
UP-0265	IC109	1302921	1	MIC uPD74HC02C(HD74HC02P)
UP-0265	IC110	1300638	1	MIC HD14053BP(MC14053BCP)
UP-0265	IC111	1253109	1	OPIC uPC358C DUAL
UP-0265	IC112	1252752	1	OPIC HA17082PS 2FET
UP-0265	IC113	1204947	1	AIC uPC1263C2 AUDIO AMP

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-0265	Q101	4330011	1	TRA	2SA836 C or D TZ
UP-0265	Q102	4335069	1	TRC	2SC1213AKDTZ
UP-0265	RA101	4093392	1	RM	EXB-F9L (10K+47)J
UP-0265	RA102	4093124	1	RM	EXB-F9E 472J 4.7KOHM

UP-0315 Regulator unit

UP-0315	CN001	5413981	1	NCN	172038-1 11P
UP-0315	CN002	5424755	1	PCN	HNC2-2.5P-2DS 2P
UP-0315	CN003	5415239	1	NCN	171363-1 17pin Receptacle Male
UP-0315	CN004	5428225	1	PCN	M60-02-30-114P
UP-0315	CN005	5424657	1	PCN	Housing HNC2-2.5S-2 2P
UP-0315	C003	3839757	1	FLC1	ECQ-V1H104JZ 0.1uF
UP-0315	C004	3839525	1	FLC1	ECQ-B1H102JZ 0.001uF
UP-0315	C008	3839525	1	FLC1	ECQ-B1H102JZ 0.001uF
UP-0315	C010	3801486	1	EC04	KME25VB2200 25/2200
UP-0315	C014	3801628	1	EC04	KME35VB1000 35/1000
UP-0315	C019	3820795	1	FLC1	ECQ-B1H 103JZ 0.01uF
UP-0315	D002	1090089	1	ZD3	HZ12LA2 Orange
UP-0315	D005	0940501	1	DB	S5VB20
UP-0315	D007	0910561	1	DP	S10SC4M 10A40V
UP-0315	D008-D009	0940261	2	DB	S4VB20 4A/200V
UP-0315	D010-D011	0800172	2	D	1S2076A(1S953(3)1S954)
UP-0315	F001	5621079	1	FUSE	179 120-2A
UP-0315	F002	5621088	1	FUSE	179 120-3.15A
UP-0315	F003-F006	5621079	4	FUSE	179 120-2A
UP-0315	IC001	1250219	1	REG	HA17723 (723CJ.Yellow)
UP-0315	IC002	1601893	1	MD	SWC-01
UP-0315	IC003	1253305	1	REG	uPC7808H Regulator
UP-0315	IC004	1253288	1	REG	uPC7908H Regulator
UP-0315	IC005-IC006	1204867	2	AIC	HA17903PS Comparator
UP-0315	LED001-LED007	1102246	7	LED	GL-3AR2 Red
UP-0315	L001	3750825	1	CH	SKC-203 100 uH
UP-0315	Q001	0950615	1	SCR	5P4M (5A400V)
UP-0315	Q001	5601323	1	SOKT	RT807
UP-0315	Q002	0101267	1	TRA	2SA1015-Y 120-240
UP-0315	Q003	5601323	1	SOKT	RT807
UP-0315	Q005	0302362	1	TRC	2SC1213A-C
UP-0315	Q006	0950615	1	SCR	5P4M (5A400V)
UP-0315	Q006	5601323	1	SOKT	RT807

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-0315	Q007	0101294	1	TRA 2SA1012-Y
UP-0315	Q007	5601323	1	SOKT RT807
UP-0315	Q009	0101267	1	TRA 2SA1015-Y 120-240
UP-0315	RA001	4090582	1	RM EXB-P84-103J 2.5 pitch
UP-0315	VR001	4160809	1	TPOT GF06P 2KOHM
UP-0315	VR002	4160613	1	TPOT GF06P 10KOHM
UP-0315	VR003	4160907	1	TPOT GF-06S(ET-6S) 1KOHM

UP-0464 AD board

UP-0464	CN101	5427939	1	PCN PCN10EA-90P-2.54DS(05)
UP-0464	CN102	5427895	1	PCN PCN10EA-32P-2.54DS(05)
UP-0464	CN103	5408024	1	ACN2 RDCD-37SE-LNA Receptacle Female
UP-0464	C001-C002	4315367	2	FLC1 ECQ-V 1H 334JZ3 (0.33uF)
UP-0464	C003-C004	4312503	2	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0464	C005-C006	4315304	2	FLC1 ECQ-V 1H 104JZ3 (0.1uF)
UP-0464	C007-C009	4312503	3	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0464	C101-C116	4315242	16	FLC1 ECQ-V 1H 333JZ3 (0.033uF)
UP-0464	C201-C216	4315242	16	FLC1 ECQ-V 1H 333JZ3 (0.033uF)
UP-0464	C301-C311	4315242	11	FLC1 ECQ-V 1H 333JZ3 (0.033uF)
UP-0464	C401-C406	4315162	6	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0464	C411-C416	4315162	6	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0464	C421-C426	4315162	6	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0464	C431-C436	4315162	6	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0464	C441-C446	4315162	6	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0464	C451-C456	4315162	6	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0464	C461-C466	4315162	6	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0464	C471-C476	4315162	6	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0464	C481-C482	4315162	2	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0464	C701	4317525	1	CEC1 TP D55Y5V1H 104Z 5-W
UP-0464	C702	3820928	1	FLC1 ECQP1H102JZ 1000pF
UP-0464	C703	4317525	1	CEC1 TP D55Y5V1H 104Z 5-W

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-0464	C704	4312503	1	TC04	ECSZ35HS6R8B 6.8uF/35V
UP-0464	C705-C707	4317525	3	CEC1	TP D55Y5V1H 104Z 5-W
UP-0464	C708-C709	4312503	2	TC04	ECSZ35HS6R8B 6.8uF/35V
UP-0464	C801-C860	4317525	60	CEC1	TP D55Y5V1H 104Z 5-W
UP-0464	DA101	0800608	1	D	Diode Array DAN 803
UP-0464	DA102	0800591	1	D	Diode Array DAP 803
UP-0464	DA103	0800608	1	D	Diode Array DAN 803
UP-0464	DA104	0800591	1	D	Diode Array DAP 803
UP-0464	DA201	0800608	1	D	Diode Array DAN 803
UP-0464	DA202	0800591	1	D	Diode Array DAP 803
UP-0464	DA203	0800608	1	D	Diode Array DAN 803
UP-0464	DA204	0800591	1	D	Diode Array DAP 803
UP-0464	DA301	0800608	1	D	Diode Array DAN 803
UP-0464	DA302	0800591	1	D	Diode Array DAP 803
UP-0464	D201-D202	4322528	2	D	1S2076ARE
UP-0464	D301-D306	4322528	6	D	1S2076ARE
UP-0464	D401-D406	4322519	6	D	1SS104,TPB2
UP-0464	D411-D416	4322519	6	D	1SS104,TPB2
UP-0464	D421-D426	4322519	6	D	1SS104,TPB2
UP-0464	D431-D436	4322519	6	D	1SS104,TPB2
UP-0464	D441-D446	4322519	6	D	1SS104,TPB2
UP-0464	D451-D456	4322519	6	D	1SS104,TPB2
UP-0464	D461-D466	4322519	6	D	1SS104,TPB2
UP-0464	D471-D476	4322519	6	D	1SS104,TPB2
UP-0464	D481-D482	4322519	2	D	1SS104,TPB2
UP-0464	IC201-IC204	1253831	4	OPIC	uPC458C
UP-0464	IC301-IC303	1253831	3	OPIC	uPC458C
UP-0464	IC401-IC463	1253715	63	OPIC	uPC812C(LF412CN)2FET
UP-0464	IC501-IC502	1303769	2	MIC	uPD74HCT240C
UP-0464	IC503-IC504	1303822	2	MIC	uPD74HCT640C
UP-0464	IC505-IC506	1303742	2	MIC	HD74HCT138P
UP-0464	IC507	1303564	1	MIC	HD74HC164P(uPD74HC164C)
UP-0464	IC508	1303555	1	MIC	HD74HC10(uPD74HC10C)
UP-0464	IC509	1302975	1	MIC	HD74HC32P(uPD74HC32C)
UP-0464	IC510	1202628	1	TIC	SN74LS01
UP-0464	IC511	1302939	1	MIC	HD74HC04P(uPD74HC04C)
UP-0464	IC601-IC602	1303537	2	MIC	HD74HC390P (uPD74HC390C)
UP-0464	IC603	1303074	1	MIC	uPD74HC4040C(HD74HC4040P)
UP-0464	IC604	1303386	1	MIC	uPD74HC175C(HD74HC175P)
UP-0464	IC605	1302948	1	MIC	uPD74HC08C(HD74HC08P)
UP-0464	IC606	1302975	1	MIC	HD74HC32P(uPD74HC32C)
UP-0464	IC607	1303092	1	MIC	HD74HC74P(uPD74HC74C)
UP-0464	IC608	1302939	1	MIC	HD74HC04P(uPD74HC04C)

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-0464	IC609	1301263	1	MIC	MC14504BCP
UP-0464	IC610	1303092	1	MIC	HD74HC74P(uPD74HC74C)
UP-0464	IC621-IC628	1303698	8	MIC	MC14051BCP(JLC1133P)
UP-0464	IC701	1301263	1	MIC	MC14504BCP
UP-0464	IC702-IC704	1300611	3	MIC	HD14051BP(MC14051BCP)
UP-0464	IC705	1301263	1	MIC	MC14504BCP
UP-0464	IC706-IC709	1300611	4	MIC	HD14051BP(MC14051BCP)
UP-0464	IC710	1301263	1	MIC	MC14504BCP
UP-0464	IC711	1302993	1	MIC	HD74HC139P(uPD74HC139C)
UP-0464	IC712	1253715	1	OPIC	uPC812C(LF412CN)2FET
UP-0464	IC713	1253386	1	AIC	uPC649C
UP-0464	IC714	1350414	1	ADIC	HI1-574AJD (AD574JD)
UP-0464	IC715	1253831	1	OPIC	uPC458C
UP-0464	IC801-IC802	1207285	2	CPU	MB8421-12LP
UP-0464	IC803	1303056	1	MIC	HD74HC244P(uPD74HC244C)
UP-0464	IC804	1303243	1	MIC	HD74HC374P(uPD74HC374C)
UP-0464	IC901	1251584	1	REG	uPC78L15J (NJM78L15A)
UP-0464	IC902	1251878	1	REG	uPC79L15J (NJM79L15A)
UP-0464	RA101	4093436	1	RM	EXB-F9E-104
UP-0464	RA102-RA103	4093196	2	RM	EXB-F8V 103J 10K
UP-0464	RA104	4093436	1	RM	EXB-F9E-104
UP-0464	RA105-RA106	4093196	2	RM	EXB-F8V 103J 10K
UP-0464	RA201	4093436	1	RM	EXB-F9E-104
UP-0464	RA202-RA203	4093196	2	RM	EXB-F8V 103J 10K
UP-0464	RA204	4093436	1	RM	EXB-F9E-104
UP-0464	RA205-RA206	4093196	2	RM	EXB-F8V 103J 10K
UP-0464	RA301	4093436	1	RM	EXB-F9E-104
UP-0464	RA302-RA303	4093196	2	RM	EXB-F8V 103J 10K
UP-0464	RA501-RA504	4093436	4	RM	EXB-F9E-104
UP-0464	RA506-RA508	4093436	3	RM	EXB-F9E-104
UP-0464	SKT714	5422846	1	SOKT	IC SOCKET DL-2-28A (01)
UP-0464	VR701	4160596	1	TPOT	GF06P 1KOHM
UP-0464	VR702	4160792	1	TPOT	GF06P 200 OHM
UP-0464	VR703	4160613	1	TPOT	GF06P 10KOHM
UP-0464	VR704	4160658	1	TPOT	GF06P 500 OHM

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-0481 Operation board, main					
UP-0481	CN101	5429251	1	PCN	HIF3BAG-30PA-2.54DSA
UP-0481	CN102	5427663	1	PCN	M60-12-30-114P Straight
UP-0481	CN104	5427645	1	PCN	M60-06-30-114P Straight
UP-0481	CN201	5429429	1	PCN	FFC-26BSM1#02
UP-0481	C101	4315242	1	FLC1	ECQ-V 1H 333JZ3 (0.033uF)
UP-0481	C106	4312503	1	TCO4	ECSZ35HS6R8B 6.8uF/35V
UP-0481	C107-C109	4317525	3	CEC1	TP D55Y5V1H 104Z 5-W
UP-0481	C110	4315385	1	FLC1	ECQ-V 1H 474JZ3 (0.47uF)
UP-0481	C201-C203	4315242	3	FLC1	ECQ-V 1H 333JZ3 (0.033uF)
UP-0481	DA101-DA102	0800608	2	D	Diode Array DAN 803
UP-0481	D101-D108	4320031	8	D	1S2076ATE
UP-0481	IC101	1203975	1	TR	TD62004P
UP-0481	IC102	1203333	1	TIC	SN74LS174
UP-0481	IC103	1203093	1	TIC	SN74LS125
UP-0481	IC104	1302957	1	MIC	HD74HC14P(uPD74HC14C)
UP-0481	IC105	1300504	1	MIC	HD14040BP (MC14040BCP)
UP-0481	IC106	1303092	1	MIC	HD74HC74P(uPD74HC74C)
UP-0481	IC201-IC202	1302957	2	MIC	HD74HC14P(uPD74HC14C)
UP-0481	IC203-IC204	1206348	2	TIC	74F534
UP-0481	IC205	1203333	1	TIC	SN74LS174
UP-0481	IC206	1206544	1	TIC	74F138PC(N74F138N)
UP-0481	IC207-IC208	1203173	2	TIC	SN74LS148
UP-0481	LED101-LED108	1102611	8	LED	HLMP-2500 green
UP-0481	LED109-LED112	1101407	4	LED	LT9002D
UP-0481	LED201-LED202	1101701	2	LED	LD101YY
UP-0481	LED203-LED204	1101407	2	LED	LT9002D
UP-0481	LED205	1101416	1	LED	LT9002H
UP-0481	RA101	4093454	1	RM	EXB-F9E-271
UP-0481	RA102-RA103	4093436	2	RM	EXB-F9E-104
UP-0481	RA104	4093454	1	RM	EXB-F9E-271
UP-0481	RA105	4093828	1	RM	EXB-F9E-151
UP-0481	SW101-SW108	3211231	8	SW	SKHCAC(KHC-10903)
UP-0481	SW201-SW208	3211231	8	SW	SKHCAC(KHC-10903)
UP-0481	SW301-SW307	3211231	7	SW	SKHCAC(KHC-10903)
UP-0481	SW309	3211231	1	SW	SKHCAC(KHC-10903)

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-0482 Operation board, VR				
UP-0482	CN001	5427645	1	PCN M60-06-30-114P Straight
UP-0482	CN002	5427636	1	PCN M60-03-30-114P Straight
UP-0482	VR001	4150446	1	TVR1 EVJ-2KA 50Kohm L=10
UP-0482	VR002-VR003	4150259	2	TVR1 EVJ-2KA 500ohm L=10
UP-0483 Operation board, left				
UP-0483	CN203	5425567	1	PCN HKP-26ML-13BT
UP-0483	CN204	5422249	1	PCN HKP-6ML-3BT
UP-0483	LED101-LED108	1102611	8	LED HLMP-2500 green
UP-0483	LED109-LED112	1101407	4	LED LT9002D
UP-0483	LED113	1101461	1	LED LT9002N
UP-0483	LED114	1101416	1	LED LT9002H
UP-0483	RA101	4093454	1	RM EXB-F9E-271J
UP-0483	RA102	4093828	1	RM EXB-F9E-151J
UP-0483	SW101-SW109	3211231	9	SW SKHCAC(KHC-10903)
UP-0507 WS/IO board (QI-809P)				
UP-0507	CN101	5427939	1	PCN PCN10EA-90P-2.54DS(05)
UP-0507	CN102	5427895	1	PCN PCN10EA-32P-2.54DS(05)
UP-0507	CN103	5424229	1	PCN HIF3BA-30PA-2.54DS
UP-0507	CN104	5429242	1	PCN HIF3BD-10PA-2.54DS
UP-0507	CN105	5408024	1	ACN2 RDCD-37SE-LNA Receptacle Female
UP-0507	C001-C007	4312503	7	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0507	C008-C022	4317525	15	CEC1 TP D55Y5V1H 104Z 5-W
UP-0507	C023-C024	4315367	2	FLC1 ECQ-V 1H 334JZ3 (0.33uF)
UP-0507	C030-C039	4317525	10	CEC1 TP D55Y5V1H 104Z 5-W
UP-0507	C202-C203	4317614	2	CEC2 DD05-989B 221K500 (220pF)
UP-0507	D001-D002	4320031	2	D 1S2076ATE
UP-0507	D500-D524	4320049	25	D 1SS237(1)-T1
UP-0507	IC101-IC103	1303769	3	MIC uPD74HCT240C
UP-0507	IC104	1303778	1	MIC uPD74HCT244C
UP-0507	IC105-IC106	1303822	2	MIC uPD74HCT640C

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-0507	IC107-IC108	1302984	2	MIC	uPD74HC138C(HD74HC138P)
UP-0507	IC109	1206179	1	TIC	74F20
UP-0507	IC110	1302975	1	MIC	HD74HC32P(uPD74HC32C)
UP-0507	IC111	1202512	1	TIC	SN74LS30N
UP-0507	IC112	1205108	1	TIC	74F04PC
UP-0507	IC113	1302984	1	MIC	uPD74HC138C(HD74HC138P)
UP-0507	IC201	1205786	1	CPU	uPD71055C(82C55A-2)
UP-0507	IC202-IC204	1203779	3	TIC	SN74LS367
UP-0507	IC205	1203075	1	TIC	SN74LS123
UP-0507	IC212-IC215	1206473	4	CPU	MB84256-10LP-G
UP-0507	IC301	1207365	1	CPU	uPD72001C
UP-0507	IC303	1205206	1	TIC	SN75188N
UP-0507	IC304	1205198	1	TIC	SN75189AN
UP-0507	IC305	1303136	1	MIC	HD74HC393P(uPD74HC393C)
UP-0507	IC306	1205117	1	TIC	74F08PC
UP-0507	IC307	1205153	1	TIC	74F164PC
UP-0507	IC308	1302939	1	MIC	HD74HC04P(uPD74HC04C)
UP-0507	IC309	1205536	1	TIC	74F10PC 3INPUT NAND
UP-0507	IC310	1202798	1	TIC	SN74LS38
UP-0507	IC312	1206179	1	TIC	74F20
UP-0507	IC401	1207285	1	CPU	MB8421-12LP
UP-0507	IC402-IC404	1203966	3	TIC	SN74LS244
UP-0507	IC405	1204992	1	TIC	SN74LS641
UP-0507	IC406	1202423	1	TIC	SN74LS04N
UP-0507	IC501	1251361	1	REG	uPC78L12J (NJM78L12A)
UP-0507	IC502	1251379	1	REG	uPC79L12J (NJM79L12A)
UP-0507	RA101-RA108	4093436	8	RM	EXB-F9E-104
UP-0507	RA109-RA110	4093124	2	RM	EXB-F9E 472J 4.7KOHM
UP-0507	SKT210-SKT211	5422846	2	SOKT	IC SOCKET DL-2-28A (01)
UP-0507	SW201	3280325	1	SW	B-4A-T

UP-0511 REC CNTL board

UP-0511	CN101	5427939	1	PCN	PCN10EA-90P-2.54DS(05)
UP-0511	CN102	5427895	1	PCN	PCN10EA-32P-2.54DS(05)
UP-0511	CN103	5422623	1	PCN	HIF3BA-20PA-2.54DS
UP-0511	CN104	5408033	1	ACN2	RDBD-25SE-LNA Receptacle Female
UP-0511	CN105	5408051	1	ACN2	RDED-9SE-LNA Receptacle Female
UP-0511	C201	4315046	1	FLC1	ECQ-B 1H 102JZ3 0.001uF

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-0511	C501	4312503	1	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0511	C502	4315304	1	FLC1 ECQ-V 1H 104JZ3 (0.1uF)
UP-0511	C801-C803	4317525	3	CEC1 TP D55Y5V1H 104Z 5-W
UP-0511	C804-C807	4312503	4	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0511	C808-C833	4317525	26	CEC1 TP D55Y5V1H 104Z 5-W
UP-0511	C834-C836	4312503	3	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0511	C837-C839	4317525	3	CEC1 TP D55Y5V1H 104Z 5-W
UP-0511	D501-D502	4320031	2	D 1S2076ATE
UP-0511	IC101-IC102	1303769	2	MIC uPD74HCT240C
UP-0511	IC103	1303822	1	MIC uPD74HCT640C
UP-0511	IC104-IC105	1303742	2	MIC HD74HCT138P
UP-0511	IC106	1303564	1	MIC HD74HC164P(uPD74HC164C)
UP-0511	IC107	1205536	1	TIC 74F10PC 3INPUT NAND
UP-0511	IC108	1202628	1	TIC SN74LS01
UP-0511	IC109	1302975	1	MIC HD74HC32P(uPD74HC32C)
UP-0511	IC110	1302939	1	MIC HD74HC04P(uPD74HC04C)
UP-0511	IC201	1207365	1	CPU uPD72001C
UP-0511	IC202	1206758	1	TIC SN75174N LINE DRIVER
UP-0511	IC203	1252957	1	DIC AM26LS33PC QUAD L.REC.AMD
UP-0511	IC204	1202423	1	TIC SN74LS04N
UP-0511	IC205	1202762	1	TIC SN74LS32
UP-0511	IC206	1206758	1	TIC SN75174N LINE DRIVER
UP-0511	IC207-IC208	1202887	2	TIC SN74LS74AN
UP-0511	IC209	1202566	1	TIC SN74LS157N
UP-0511	IC210	1303778	1	MIC uPD74HCT244C
UP-0511	IC211	1303127	1	MIC HD74HC273P(uPD74HC273C)
UP-0511	IC301	1206027	1	CPU MSM80C85A-2RS
UP-0511	IC302	1302984	1	MIC uPD74HC138C(HD74HC138P)
UP-0511	IC303	1303083	1	MIC uPD74HC373C(HD74HC373P)
UP-0511	IC305	1206473	1	CPU MB84256-10LP-G
UP-0511	IC306	1302975	1	MIC HD74HC32P(uPD74HC32C)
UP-0511	IC307-IC308	1303092	2	MIC HD74HC74P(uPD74HC74C)
UP-0511	IC309	1302912	1	MIC HD74HC00P(uPD74HC00C)
UP-0511	IC310	1303626	1	MIC HD74HC11P(uPD74HC11C)
UP-0511	IC401	1303092	1	MIC HD74HC74P(uPD74HC74C)
UP-0511	IC402	1303029	1	MIC uPD74HC161C(HD74HC161P)
UP-0511	IC403	1303136	1	MIC HD74HC393P(uPD74HC393C)
UP-0511	IC404	1303092	1	MIC HD74HC74P(uPD74HC74C)
UP-0511	IC405	1302948	1	MIC uPD74HC08C(HD74HC08P)
UP-0511	IC406	1303564	1	MIC HD74HC164P(uPD74HC164C)
UP-0511	IC407	1302939	1	MIC HD74HC04P(uPD74HC04C)
UP-0511	IC501	1302921	1	MIC uPD74HC02C(HD74HC02P)
UP-0511	IC502	1302886	1	ADIC M58990P-1 8-8-AD

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-0511	IC601	1303136	1	MIC	HD74HC393P(uPD74HC393C)
UP-0511	IC602-IC605	1303002	4	MIC	uPD74HC157C(HD74HC157P)
UP-0511	IC606	1204902	1	CPU	HM6264LP-15(uPD4364C-15L
UP-0511	IC607	1303065	1	MIC	HD74HC245P(uPD74HC245C)
UP-0511	IC608	1303288	1	MIC	HD74HC597P(uPD74HC597C)
UP-0511	IC609	1303555	1	MIC	HD74HC10(uPD74HC10C)
UP-0511	IC610	1303243	1	MIC	HD74HC374P(uPD74HC374C)
UP-0511	IC611	1303092	1	MIC	HD74HC74P(uPD74HC74C)
UP-0511	IC701	1206455	1	CPU	uPD71054C
UP-0511	IC702	1303127	1	MIC	HD74HC273P(uPD74HC273C)
UP-0511	IC703	1303778	1	MIC	uPD74HCT244C
UP-0511	IC704	1206455	1	CPU	uPD71054C
UP-0511	IC705	1302975	1	MIC	HD74HC32P(uPD74HC32C)
UP-0511	IC706	1303395	1	MIC	uPD74HC109C(HD74HC109P)
UP-0511	IC707	1207285	1	CPU	MB8421-12LP
UP-0511	IC708	1302939	1	MIC	HD74HC04P(uPD74HC04C)
UP-0511	IC709	1302975	1	MIC	HD74HC32P(uPD74HC32C)
UP-0511	IC801	1253537	1	OPIC	LM361N High-speed Comparator
UP-0511	IC802	1205108	1	TIC	74F04PC
UP-0511	SKT301	5422605	1	SOKT	IC SOCKET DL-2-40A (01)
UP-0511	SKT304	5422846	1	SOKT	IC SOCKET DL-2-28A (01)
UP-0511	SW101	3352088	1	SW	SKHCAD (KHC10904)

UP-0512 REC DRV board

UP-0512		5492333	2	CHEM	Heat Sink Seat TC30-AG TO-3P
UP-0512	CN101	5429367	1	PCN	FFC-14BSM1#02
UP-0512	CN102	5429394	1	PCN	FFC-20BSM1#02
UP-0512	CN103	5422766	1	PCN	HIF3BA-20PA-2.54DSA
UP-0512	CN104	5413883	1	NCN	172036-1 A,M,P
UP-0512	CN105	5429322	1	PCN	FFC-6BSM1#02
UP-0512	CN106	5429198	1	PCN	TCS7587-01-401
UP-0512	C101	4315304	1	FLC1	ECQ-V 1H 104JZ3 (0.1uF)
UP-0512	C103-C104	4315385	2	FLC1	ECQ-V 1H 474JZ3 (0.47uF)
UP-0512	C105-C106	4315162	2	FLC1	ECQ-B 1H 103JZ3 0.01uF
UP-0512	C107	4315189	1	FLC1	ECQ-B 1H 153JZ3 0.015uF
UP-0512	C201-C202	4315385	2	FLC1	ECQ-V 1H 474JZ3 (0.47uF)
UP-0512	C204-C205	4310176	2	ECO4	ECEA1VU 100B (10uF/35V)
UP-0512	C301	4315304	1	FLC1	ECQ-V 1H 104JZ3 (0.1uF)
UP-0512	C304	4315206	1	FLC1	ECQ-B 1H 223JZ3 0.022uF

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-0512	C305	4315304	1	FLC1 ECQ-V 1H 104JZ3 (0.1uF)
UP-0512	C306	4312503	1	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0512	C401-C402	3802128	2	EC04 ECOS1VG472Q 4700uF/35V
UP-0512	C403	4315162	1	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-0512	C404	3802101	1	EC04 ECOS1EG472E 4700uF/25V
UP-0512	C405	4315385	1	FLC1 ECQ-V 1H 474JZ3 (0.47uF)
UP-0512	C406	4310176	1	EC04 ECEA1VU 100B (10uF/35V)
UP-0512	C407	4315304	1	FLC1 ECQ-V 1H 104JZ3 (0.1uF)
UP-0512	C408	4310176	1	EC04 ECEA1VU 100B (10uF/35V)
UP-0512	C421-C423	4312503	3	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-0512	C431-C432	3802119	2	EC04 ECOS1EG153T 15000uF/25V
UP-0512	C501-C509	4317525	9	CEC1 TP D55Y5V1H 104Z 5-W
UP-0512	D101	4325089	1	ZD2 HZ5C1TE (4.9-5.1V)
UP-0512	D102	4320031	1	D 1S2076ATE
UP-0512	D201	4320031	1	D 1S2076ATE
UP-0512	D302	4320031	1	D 1S2076ATE
UP-0512	D401	0910561	1	DP S10SC4M 10A40V
UP-0512	IC101	1301601	1	MIC HD14538BP (MC14538BCP)
UP-0512	IC102	1302912	1	MIC HD74HC00P(uPD74HC00C)
UP-0512	IC103	1301601	1	MIC HD14538BP (MC14538BCP)
UP-0512	IC104	1204894	1	AIC HA17901P Comparator
UP-0512	IC105	1302912	1	MIC HD74HC00P(uPD74HC00C)
UP-0512	IC106	1302957	1	MIC HD74HC14P(uPD74HC14C)
UP-0512	IC201	1252868	1	DIC TD62307P
UP-0512	IC303	1201041	1	TIC SN7438N
UP-0512	IC304	1251165	1	OPIC uPC1458C
UP-0512	IC305	1253297	1	REG uPC 7805H
UP-0512	IC401	1601893	1	MD SWC-01
UP-0512	L401	3788838	1	L SKP-5-50
UP-0512	L402	3780864	1	L HP-054SZ
UP-0512	Q201	0101196	1	TRA 2SA1015
UP-0512	Q204-Q205	4335051	2	TRC 2SC1345KDTZ
UP-0512	Q206	0200302	1	TRA 2SA985 (2SB512P) with AC
UP-0512	Q402	0101294	1	TRA 2SA1012-Y
UP-0512	VR101	4160961	1	TPOT GF-06S(ET-6S) 5KOHM
UP-0512	VR102	4160925	1	TPOT GF-06S(ET-6S) 20KOHM
UP-0512	VR402	4160961	1	TPOT GF-06S(ET-6S) 5KOHM

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-0539 Mother board				
UP-0539	CN101-CN106	5427948	6	PCN PCN10EA-90S-2.54DSA(05)
UP-0539	CN107-CN110	5427903	4	PCN PCN10EA-32S-2.54DSA(05)
UP-0539	CN111	5427886	1	PCN PCN10EA-20S-2.54DSA(05)
UP-0539	CN112	5427868	1	PCN HIF3BA-30PA-2.54DSA
UP-0539	CN113	5427636	1	PCN M60-03-30-114P Straight
UP-0539	CN114	5427903	1	PCN PCN10EA-32S-2.54DSA(05)
UP-0539	CN115	5427645	1	PCN M60-06-30-114P Straight
UP-0539	CN116	5415239	1	NCN 171363-1 17pin Receptacle Male
UP-0539	CN117	5413713	1	NCN 350209-1 2P Pin Header ASSY
UP-0539	CN118	5424764	1	PCN HNC2-2.5P-3DS 3P
UP-0539	CN119	5413883	1	NCN 172036-1 A,M,P
UP-0539	C101-C102	3853367	2	C EECF5R5U105 1F/5.5V
UP-0539	C103	4317525	1	CEC1 TP D55Y5V1H 104Z 5-W
UP-0564 Operation board, bottom				
UP-0564	CN401	5427663	1	PCN M60-12-30-114P Straight
UP-0564	DA401	0800608	1	D Diode Array DAN 803
UP-0564	SW401-SW406	3352088	6	SW SKHCAD (KHC10904)
UP-02602 CPU board				
UP-02602	BAT101	5650555	1	CR17335SE-P
UP-02602	CN101	5427939	1	PCN PCN10EA-90P-2.54DS(05)
UP-02602	CN102	5427895	1	PCN PCN10EA-32P-2.54DS(05)
UP-02602	CN103	5408033	1	ACN2 RDBD-25SE-LNA Receptacle Female
UP-02602	C101	4312575	1	TC04 204M2002 226MB(22uF/20V)
UP-02602	C102	4317525	1	CEC1 TP D55Y5V1H 104Z 5-W
UP-02602	C103	4312557	1	TC04 204M2002 106MB(10uF/20V)
UP-02602	C104	4315304	1	FLC1 ECQ-V 1H 104JZ3 (0.1uF)
UP-02602	C105	4315162	1	FLC1 ECQ-B 1H 103JZ3 0.01uF
UP-02602	C106	4312503	1	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-02602	C107	4317552	1	CEC2 DD05-989SL 220K500 (22pF)
UP-02602	C109	4312503	1	TC04 ECSZ35HS6R8B 6.8uF/35V

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-02602	C110-C117	4317525	8	CEC1 TP D55Y5V1H 104Z 5-W
UP-02602	C118-C124	4312503	7	TC04 ECSZ35HS6R8B 6.8uF/35V
UP-02602	C125-C131	4317525	7	CEC1 TP D55Y5V1H 104Z 5-W
UP-02602	D101	4320013	1	D 1SS104,TP3
UP-02602	D102	4320022	1	D 1SS106TE
UP-02602	D103	4325071	1	ZD1 HZ3C3TE (3.3-3.5V)
UP-02602	D104	0800635	1	D HP5082-2835
UP-02602	D105-D106	4320031	2	D 1S2076ATE
UP-02602	D107-D108	4320013	2	D 1SS104,TP3
UP-02602	IC101	1206508	1	CPU HD68HC000Y8
UP-02602	IC102	1205135	1	TIC 74F74PC
UP-02602	IC103	1206366	1	TIC 74F112
UP-02602	IC104	1203271	1	TIC SN74LS164
UP-02602	IC105	1203895	1	TIC SN74LS393
UP-02602	IC106	1202405	1	TIC SN74LS00N
UP-02602	IC107-IC108	1202762	2	TIC SN74LS32
UP-02602	IC109	1202664	1	TIC SN74LS09
UP-02602	IC110	1203797	1	TIC SN74LS373
UP-02602	IC111-IC112	1206544	2	TIC 74F138PC(N74F138N)
UP-02602	IC113	1303751	1	MIC HD74HCT238P
UP-02602	IC114	1303742	1	MIC HD74HCT138P
UP-02602	IC115	1202503	1	TIC SN74LS27N
UP-02602	IC116	1253207	1	AIC TL7705CP Voltage Detector
UP-02602	IC117	1303528	1	MIC uPD74HC123C(HD74HC123P)
UP-02602	IC118	1303092	1	MIC HD74HC74P(uPD74HC74C)
UP-02602	IC119	1302948	1	MIC uPD74HC08C(HD74HC08P)
UP-02602	IC120	1302957	1	MIC HD74HC14P(uPD74HC14C)
UP-02602	IC121	1303706	1	MIC HD74HC01P
UP-02602	IC122	1202726	1	TIC SN74LS21
UP-02602	IC123	1303742	1	MIC HD74HCT138P
UP-02602	IC124	1302948	1	MIC uPD74HC08C(HD74HC08P)
UP-02602	IC125-IC126	1303092	2	MIC HD74HC74P(uPD74HC74C)
UP-02602	IC127	1303715	1	MIC uPD74HC148C
UP-02602	IC128	1302948	1	MIC uPD74HC08C(HD74HC08P)
UP-02602	IC129	1303092	1	MIC HD74HC74P(uPD74HC74C)
UP-02602	IC130	1303813	1	MIC HD74HCT534P
UP-02602	IC131	1303715	1	MIC uPD74HC148C
UP-02602	IC132	1303769	1	MIC uPD74HCT240C
UP-02602	IC133	1303742	1	MIC HD74HCT138P
UP-02602	IC134-IC135	1302948	2	MIC uPD74HC08C(HD74HC08P)
UP-02602	IC136-IC139	1303092	4	MIC HD74HC74P(uPD74HC74C)
UP-02602	IC140	1303804	1	MIC uPD74HCT374C
UP-02602	IC141	1303715	1	MIC uPD74HC148C

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-02602	IC142	1303769	1	MIC	uPD74HCT240C
UP-02602	IC143	1303742	1	MIC	HD74HCT138P
UP-02602	IC144-IC147	1206491	4	CPU	MBM27C512-20CZ-G
UP-02602	IC152-IC167	1206473	16	CPU	MB84256-10LP-G
UP-02602	IC168	1303234	1	MIC	uPD74HC132C(HD74HC132P)
UP-02602	IC169	1303662	1	CPU	MSM6242 RS
UP-02602	IC170	1207213	1	CPU	X2816BP 2K*8 EEPROM
UP-02602	IC172	1206446	1	CPU	uPD71051C
UP-02602	IC173	1206455	1	CPU	uPD71054C
UP-02602	IC174	1205206	1	TIC	SN75188N
UP-02602	IC175	1205198	1	TIC	SN75189AN
UP-02602	IC176	1302859	1	CPU	uPD8279C-2
UP-02602	IC177	1202762	1	TIC	SN74LS32
UP-02602	IC178	1204867	1	AIC	HA17903PS Comparator
UP-02602	IC179-IC180	1303769	2	MIC	uPD74HCT240C
UP-02602	IC181	1303813	1	MIC	HD74HCT534P
UP-02602	IC182-IC184	1206589	3	TIC	74F533PC(N74F533N)
UP-02602	IC185-IC186	1204983	2	TIC	SN74LS640
UP-02602	IC187-IC188	1303769	2	MIC	uPD74HCT240C
UP-02602	IC189	1251361	1	REG	uPC78L12J (NJM78L12A)
UP-02602	IC190	1251379	1	REG	uPC79L12J (NJM79L12A)
UP-02602	IC191	1205108	1	TIC	74F04PC
UP-02602	IC192-IC193	1205135	2	TIC	74F74PC
UP-02602	IC194-IC195	1302912	2	MIC	HD74HC00P(uPD74HC00C)
UP-02602	LED101-LED110	1102246	10	LED	GL-3AR2 Red
UP-02602	Q101	0302362	1	TRC	2SC1213A-C
UP-02602	RA101-RA106	4093436	6	RM	EXB-F9E-104
UP-02602	RA107	4093124	1	RM	EXB-F9E 472J 4.7KOHM
UP-02602	RA109-RA112	4093124	4	RM	EXB-F9E 472J 4.7KOHM
UP-02602	RA114	4093427	1	RM	EXB-F9E-102
UP-02602	RA115-RA116	4093124	2	RM	EXB-F9E 472J 4.7KOHM
UP-02602	SK101	5601341	1	SOKT	PIC01-10A068-391A
UP-02602	SK144-SK151	5422846	8	SOKT	IC SOCKET DL-2-28A (01)
UP-02602	SK160-SK167	5422846	8	SOKT	IC SOCKET DL-2-28A (01)
UP-02602	SW101	3352088	1	SW	SKHCAD (KHC10904)
UP-02602	SW102	3280325	1	SW	B-4A-T
UP-02602	SW103	3352435	1	SW	D1P SW B-8A
UP-02602	VC101	3890469	1	VC	TZ03R 300ER 5.2-30pF
UP-02602	X101	1705781	1	XTAL	TD308C (XCO-B)16M
UP-02602	X102	1702597	1	XTAL	KF38G 32.768KHZ

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
YS-009P0 CNS-JJS connection able (standard accessory)				
YS-009P0		5401085	2	ACN1 CDC-37P Housing Male
YS-009P0		5401111	74	ACN1 CD-PC-121 Contact Male
YS-009P0		5401361	2	ACN1 HDC-CTH1
YS-009P1 CNS-JJW connection cable (standard accessory)				
YS-009P1		5401094	2	ACN1 CDB-25P Housing Male
YS-009P1		5401111	40	ACN1 CD-PC-121 Contact Male
YS-009P1		5401352	2	ACN1 HDB-CTH1

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
SC-001RA Transformer unit (MU-820RA)				
SC-001RA	CN001	5415337	8	NCN Receptacle 170458-1
SC-001RA	CN001	5415373	1	NCN Housing 172024-1
SC-001RA	F001	5620062	1	FUSE SAU-4A
SC-001RA	F001	5625396	1	FH FEU 031.1681 Body
SC-001RA	F001	5625404	1	FH FEK 031.1661 Cap
SC-001RA	F002	5620062	1	FUSE SAU-4A
SC-001RA	F002	5625396	1	FH FEU 031.1681 Body
SC-001RA	F002	5625404	1	FH FEK 031.1661 Cap
SC-001RA	LF001	1706022	1	TH SUP-E3G-E-2 Line Filter
SC-001RA	SW001	3250367	1	SW JPZ2120-0101
SC-001RA	T001	3714802	1	PT T-3714802 117V MU800RA

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
SC-001RJ Transformer unit (MU-820RJ)					
SC-001RJ	CN001	5415337	8	NCN	Receptacle 170458-1
SC-001RJ	CN001	5415373	1	NCN	Housing 172024-1
SC-001RJ	F001	5620062	1	FUSE	SAU-4A
SC-001RJ	F001	5625396	1	FH	FEU 031.1681 Body
SC-001RJ	F001	5625404	1	FH	FEK 031.1661 Cap
SC-001RJ	F002	5620062	1	FUSE	SAU-4A
SC-001RJ	F002	5625396	1	FH	FEU 031.1681 Body
SC-001RJ	F002	5625404	1	FH	FEK 031.1661 Cap
SC-001RJ	LF001	1706022	1	TH	SUP-E3G-E-2 Line Filter
SC-001RJ	SW001	3250367	1	SW	JPZ2120-0101
SC-001RJ	T001	3714856	1	PT	T-3714856 100V MU800RJ
SC-001RK Transformer unit (MU-820RK)					
SC-001RK	CN001	5415337	8	NCN	Receptacle 170458-1
SC-001RK	CN001	5415373	1	NCN	Housing 172024-1
SC-001RK	F001	5620044	1	FUSE	GDL-2
SC-001RK	F001	5625396	1	FH	FEU 031.1681 Body
SC-001RK	F001	5625404	1	FH	FEK 031.1661 Cap
SC-001RK	F002	5620044	1	FUSE	GDL-2
SC-001RK	F002	5625396	1	FH	FEU 031.1681 Body
SC-001RK	F002	5625404	1	FH	FEK 031.1661 Cap
SC-001RK	LF001	1706022	1	TH	SUP-E3G-E-2 Line Filter
SC-001RK	SW001	3250367	1	SW	JPZ2120-0101
SC-001RK	T001	3714847	1	PT	T-3714847 200V MU800RK

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
UP-0372 CRT PWB board					
UP-0372		7401143	1		OSH-1625-SP
UP-0372	CN201	5428225	1	PCN	M60-02-30-114P
UP-0372	CN202	7400732	1		B4B-XH-A
UP-0372	CN203	7400741	1		RTB-1.5-4
UP-0372	CN204	7401277	1		B3B-XH-A
UP-0372	CN205	7400759	1		RT-01T-1.0B
UP-0372	C201	7402151	1		CEUSM1E470
UP-0372	C202	7402204	1		CEUSM2A470
UP-0372	C203	7401892	1		DEP-50V-103K
UP-0372	C204	7405914	1		DM10C271J3
UP-0372	C205	7401927	1		DEP-200V-104K
UP-0372	C206	7401116	1		DE1710BN222K2K
UP-0372	C207	7401963	1		DTW223K630V
UP-0372	C208	7405923	1		DM10C470J3
UP-0372	C209	7402196	1		CEUSM2A4R7
UP-0372	D201-D204	7400723	4		1S1585
UP-0372	D205	7400973	1		1S1555
UP-0372	GP201-GP204	7400607	4		GD626-150V
UP-0372	L201	7400777	1		EL0607SKI-101K
UP-0372	L203	7400786	1		EL0606SKI-1R0K
UP-0372	L204	7400795	1		EL0606SKI-2R2K
UP-0372	L205	7405959	1		EL0606SKI-R68M
UP-0372	SW201	7400536	1		A3A-5113-04
UP-0372	TP201-TP202	7401134	2		UP101
UP-0372	TR201	7400545	1		2SA1164-Y
UP-0372	TR202	7400554	1		2SC3597-C
UP-0372	TR203	7400572	1		2SC3595-C
UP-0372	TR204	7400581	1		2SC3601-C
UP-0372	TR205	7400599	1		2SA1407-C
UP-03731 CRT MAIN PWB board					
UP-03731	CN001	5428234	1	PCN	M60-04-30-114P
UP-03731	CN002	5413999	1	NCN	350209-1 2P
UP-03731	CN007	7400759	1		RT-01T-1.0B
UP-03731	C001	7401856	1		DEP-50V-102K
UP-03731	C002	7401018	1		DM10C121J3

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-03731	C003	7405968	1	CEUSM1H010
UP-03731	C004	7402169	1	CEUSM1H100
UP-03731	C005	7401036	1	DM15C391J3
UP-03731	C006	7405977	1	DEP-50V-152K
UP-03731	C007	7405968	1	CEUSM1H010
UP-03731	C008	7401865	1	DEP-50V-472K
UP-03731	C009	7401107	1	CQ09S1H751J
UP-03731	C011	7402169	1	CEUSM1H100
UP-03731	C012	7401874	1	DEP-50V-182K
UP-03731	C013	7401883	1	DEP-50V-224K
UP-03731	C014	7402267	1	CSO4E1D4R7M
UP-03731	C016	7402267	1	CSO4E1D4R7M
UP-03731	C017	7402178	1	CEUSM1H470
UP-03731	C018	7402213	1	CEUSM2A101
UP-03731	C019	7401099	1	2MFT-D104
UP-03731	C020	7402178	1	CEUSM1H470
UP-03731	C021	7401152	1	AWS-100V-683J
UP-03731	C022	7401161	1	AWS-100V-104J
UP-03731	C023	7402222	1	CEUSM2C470
UP-03731	C025	7405986	1	DM10C620J3
UP-03731	C026	7401954	1	DTW104K400V
UP-03731	C027	7401856	1	DEP-50V-102K
UP-03731	C028	7401072	1	DM15C391J5
UP-03731	C029	7401081	1	DM15C471J5
UP-03731	C030	7402249	1	CEUSM2D2R2
UP-03731	C031	7401856	1	DEP-50V-102K
UP-03731	C032	7401945	1	DTW474K200V
UP-03731	C033	7401936	1	DTW224K200V
UP-03731	C034	7405995	1	DTB222K1250V
UP-03731	C035	7401972	1	DTB152K1250V
UP-03731	C037	7401999	1	DKB104K1250V
UP-03731	C038	7402204	1	CEUSM2A470
UP-03731	C039	7402222	1	CEUSM2C470
UP-03731	C040	7402231	1	CEUSM2C100
UP-03731	C041	7401936	1	DTW224K200V
UP-03731	C042	7402222	1	CEUSM2C470
UP-03731	C043	7401054	1	DM15C681J3
UP-03731	C046	7406004	1	DEP-200V-223K
UP-03731	C047	7401918	1	DEP-200V-222K
UP-03731	C048	7402151	1	CEUSM1E470
UP-03731	C050	7401027	1	DM10C331J3
UP-03731	D001	7400973	1	1S1555
UP-03731	D002	7400982	1	2S5277B

ASSY	CKT NO.	PART NO.	Q'TY	DESCRIPTION
UP-03731	D003-D004	7400973	2	1S1555
UP-03731	D005	7400982	1	2S5277B
UP-03731	D006	7401241	1	CTU-G2DR
UP-03731	D007	7401205	1	GU-3C
UP-03731	D009	7401214	1	RG4
UP-03731	D010-D012	7401223	3	RF1
UP-03731	D013	7401232	1	RU2B
UP-03731	FH001	7401259	1	F-60A
UP-03731	F001	7401321	1	GGS1
UP-03731	IC001	7401268	1	TA7609P
UP-03731	L002	7411364	1	SL3523B63
UP-03731	TR001	7400643	1	2SC1815-Y
UP-03731	TR002	7400652	1	2SC752(G)TM-Y
UP-03731	TR003	7400661	1	2SC2229-Y
UP-03731	TR004	7400679	1	2SC3676
UP-03731	TR005	7400688	1	2SD1148-O
UP-03731	TR006	7400697	1	2SB863-O
UP-03731	TR007	7400705	1	2SC3620
UP-03731	TR008	7400714	1	2SC3688
UP-03731	T001	7401357	1	ST4064A83
UP-03731	T002	7406067	1	ST4120A94
UP-03731	VR001	4160613	1	TPOT GF06P 10KOHM
UP-03731	VR002	4160694	1	TPOT GF06P 200KOHM
UP-03731	VR003	4160667	1	TPOT GF06P 20KOHM
UP-03731	VR004	7401295	1	H0621A-22K-J
UP-03731	VR005	7400634	1	H1621C-2,2M-B
UP-03731	VR007	4160596	1	TPOT GF06P 1KOHM

VM-003P CRT unit

VM-003P		7400839	4	SLF-41T-1.3
VM-003P		7400884	2	SMF-01T-1.0
VM-003P		7400964	18	SIN-01T-1.8
VM-003P		7411346	3	SIN-01T-1.2
VM-003P	CN003	7400893	1	XHP-4
VM-003P	CN003-CN004	7400901	4	SXH-001T-0.6
VM-003P	CN004	7400937	1	XHP-3
VM-003P	CN005	7400919	1	P-SVF
VM-003P	CN005	7400928	4	SVF-01T-1.5A
VM-003P	CN006	7400821	1	MLP-06

ASSY	CKT NO.	PART NO.	Q'TY		DESCRIPTION
VM-003P	CN006	7400839	4		SLF-41T-1.3
VM-003P	CN008	7400857	1		MLR-06
VM-003P	CN008	7400866	4		SLM-41T-1.3
VM-003P	CN009	5416202	1	NCN	MLR-03
VM-003P	CN009	5416211	3	NCN	SLM-01T-1.3
VM-003P	CN206	7400875	1		1P-SMF
VM-003P	CN206	7400884	1		SMF-01T-1.0
VM-003P	CN207	7400875	1		1P-SMF
VM-003P	CN207	7400884	1		SMF-01T-1.0
VM-003P	CRT201	7401713	1		E2809B31-SDHT
VM-003P	L201	7400848	1		SL3517A55
VM-003P	SK201	7400955	1		S8-502B-40

Section 12

12. Part location guide

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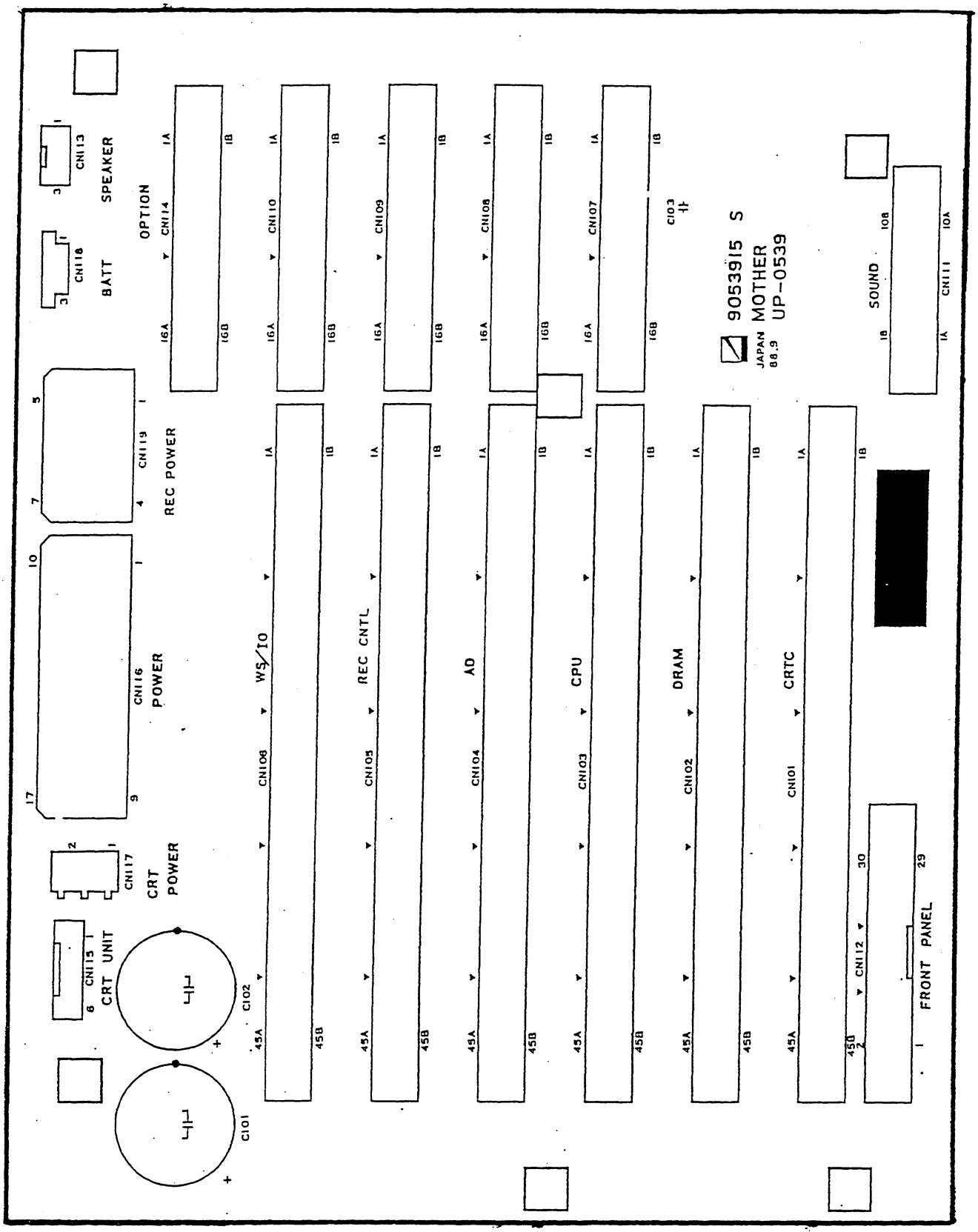
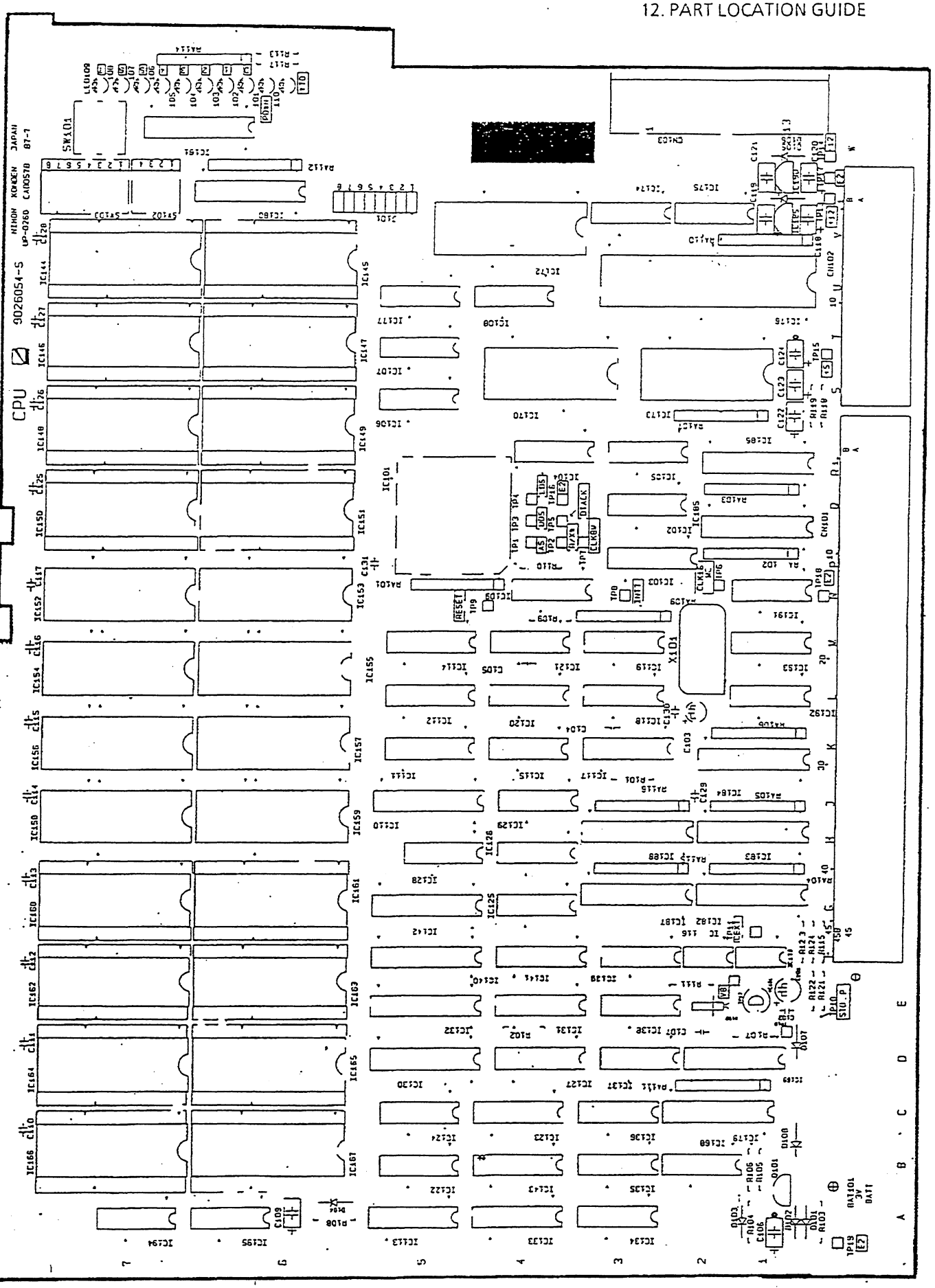
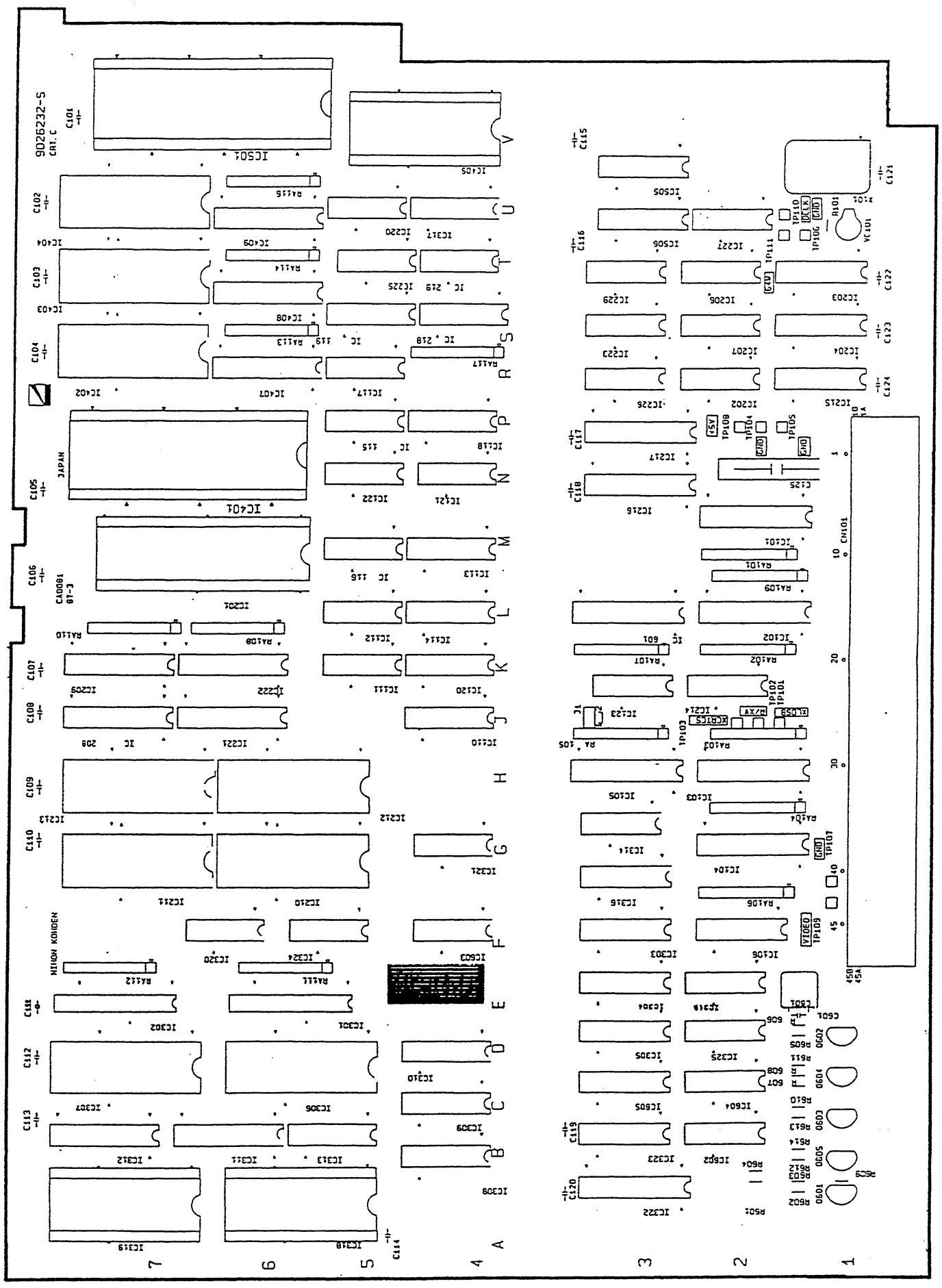


UP-0539
Mother board



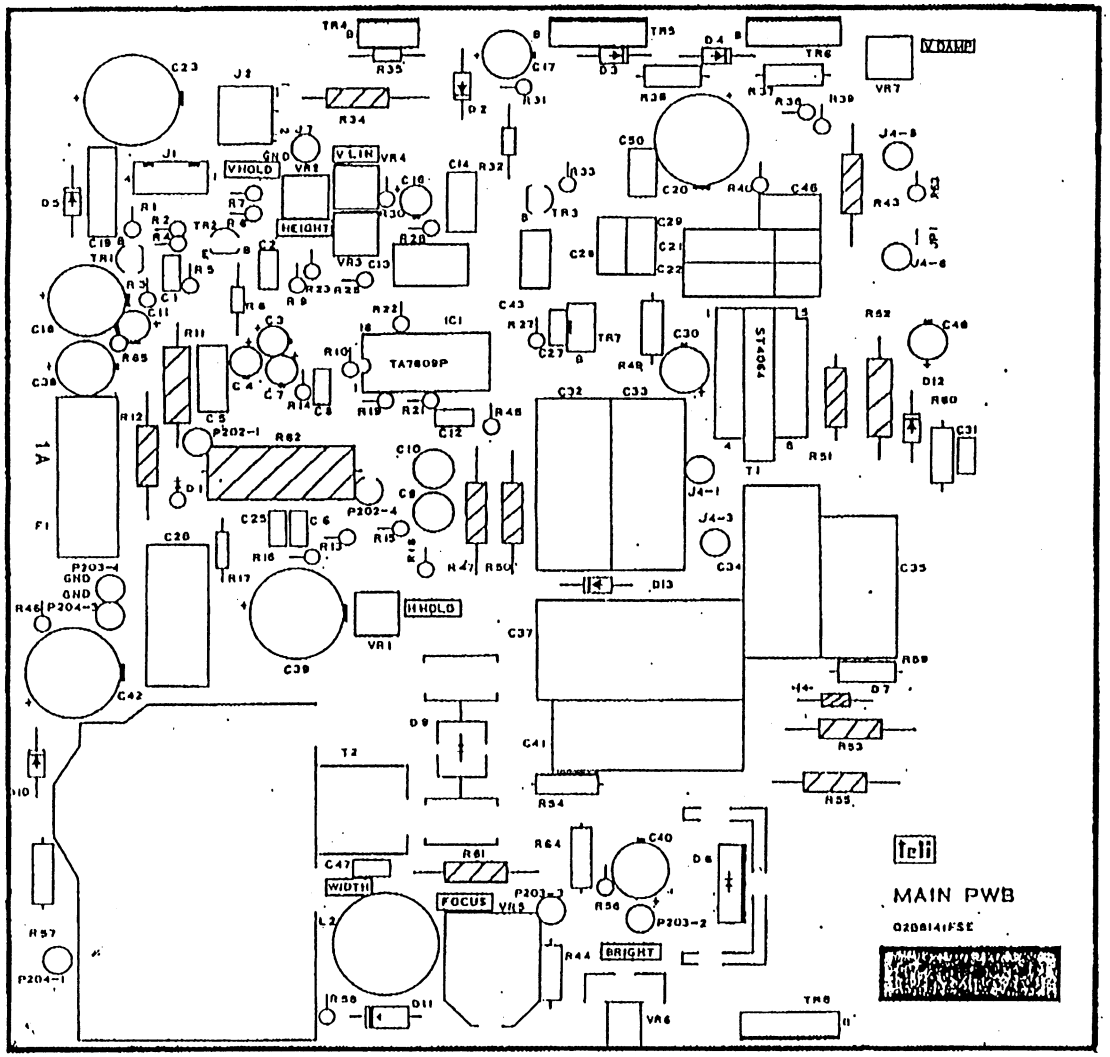
UP-02602 CPU board



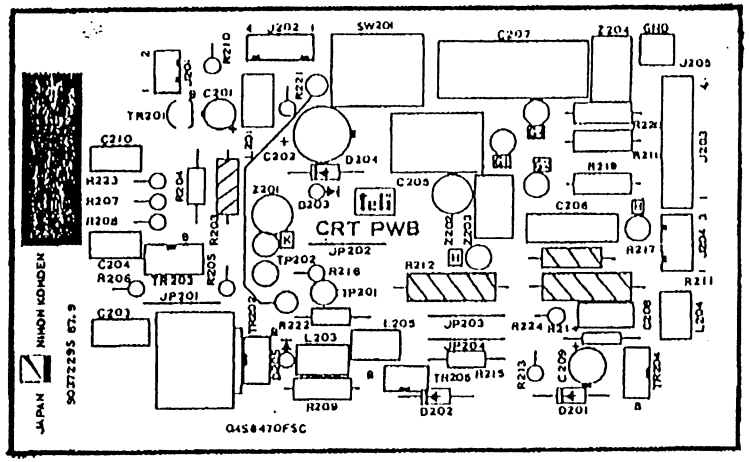
UP-0262 CRTC board

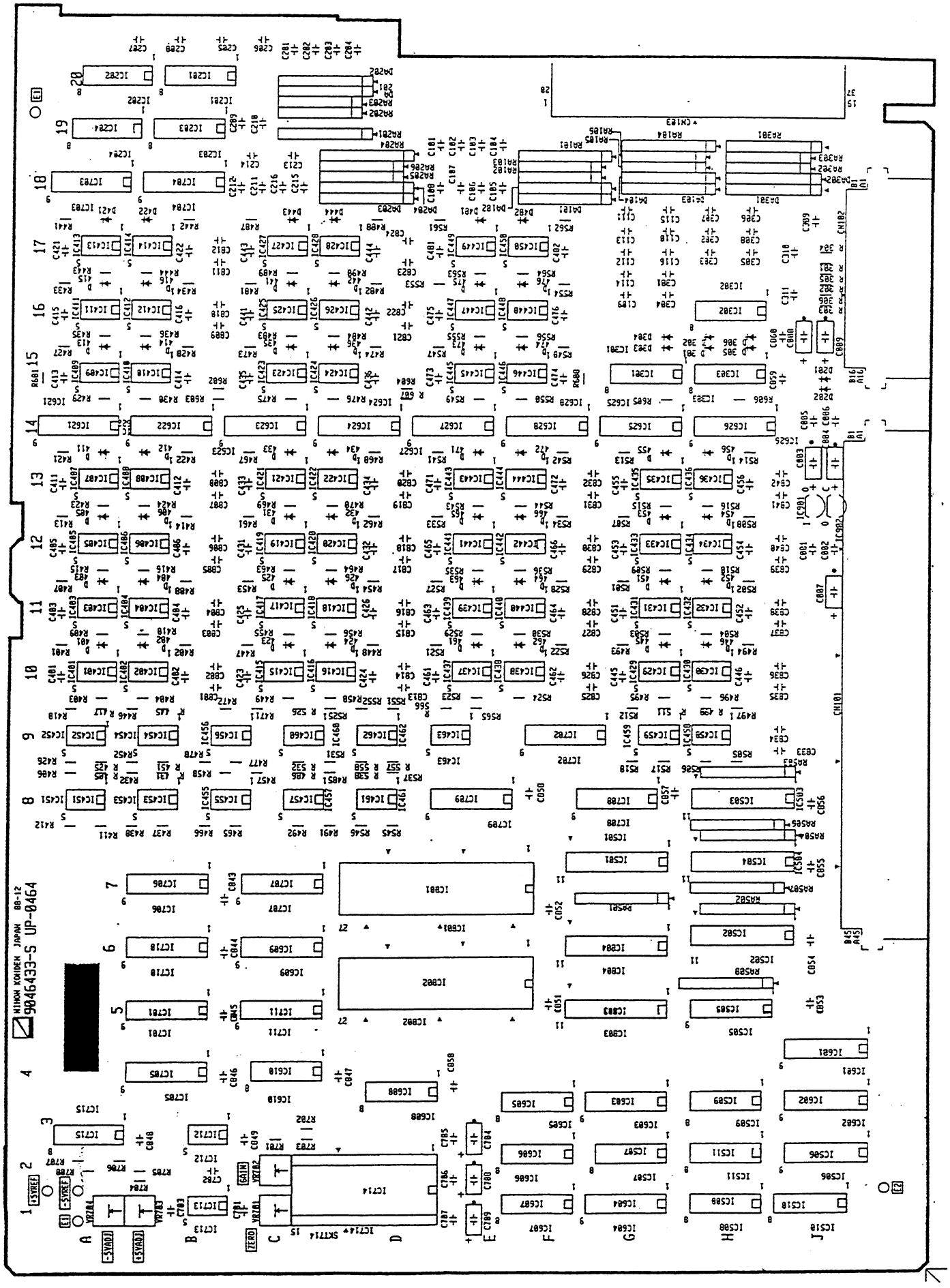
VM-003P CRT unit

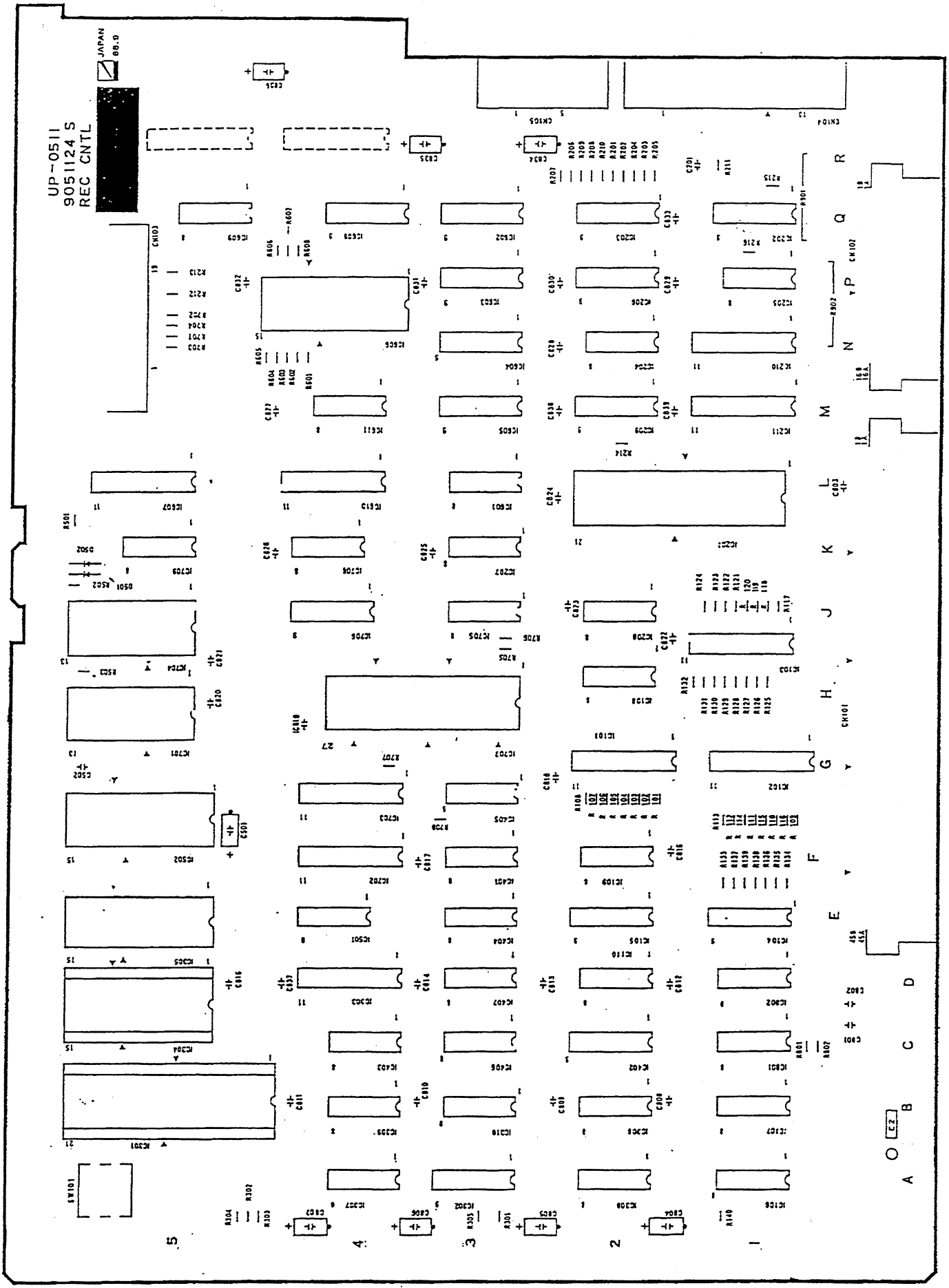
UP-03731 CRT MAIN PWB board



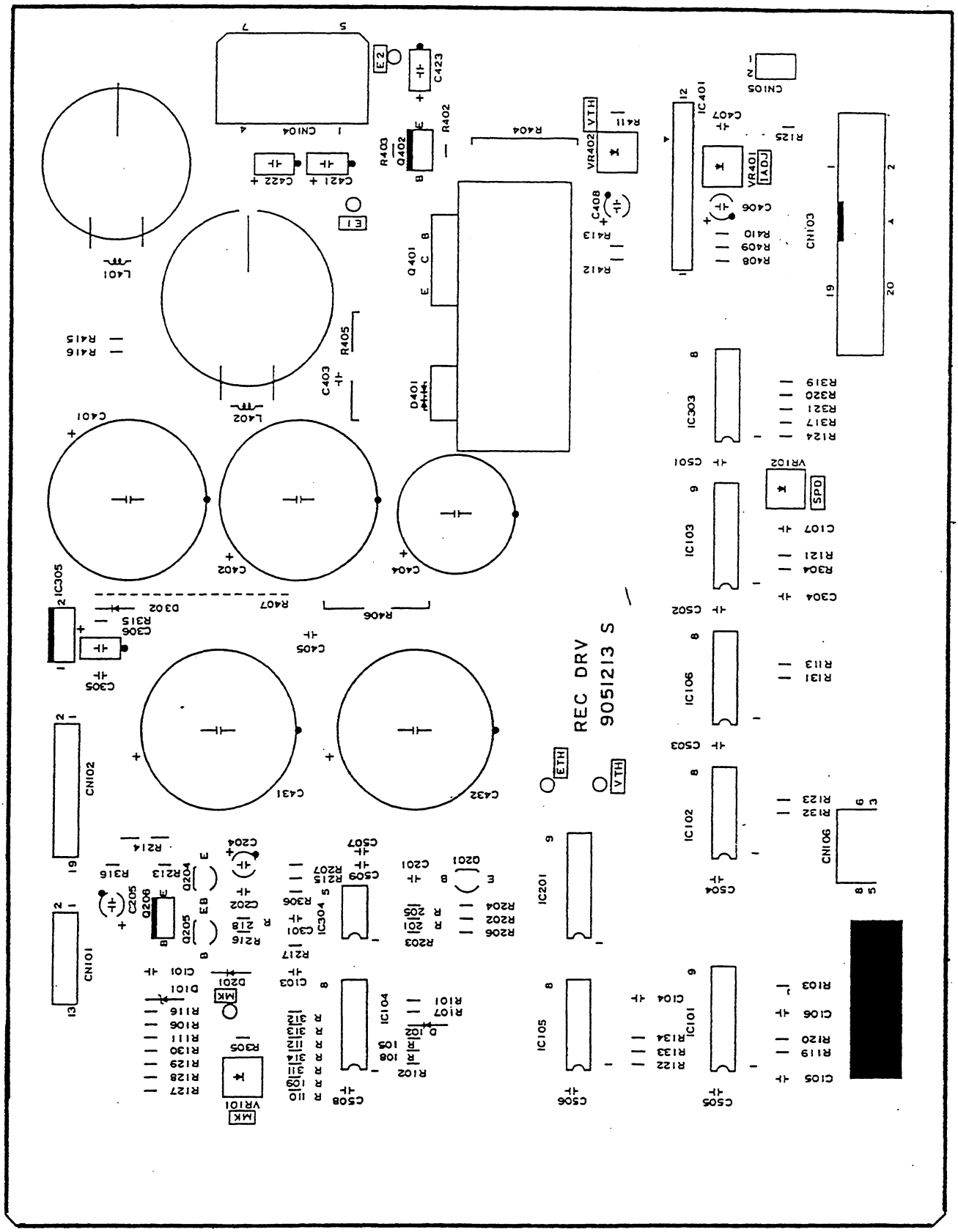
UP-0372 CRT PWB board



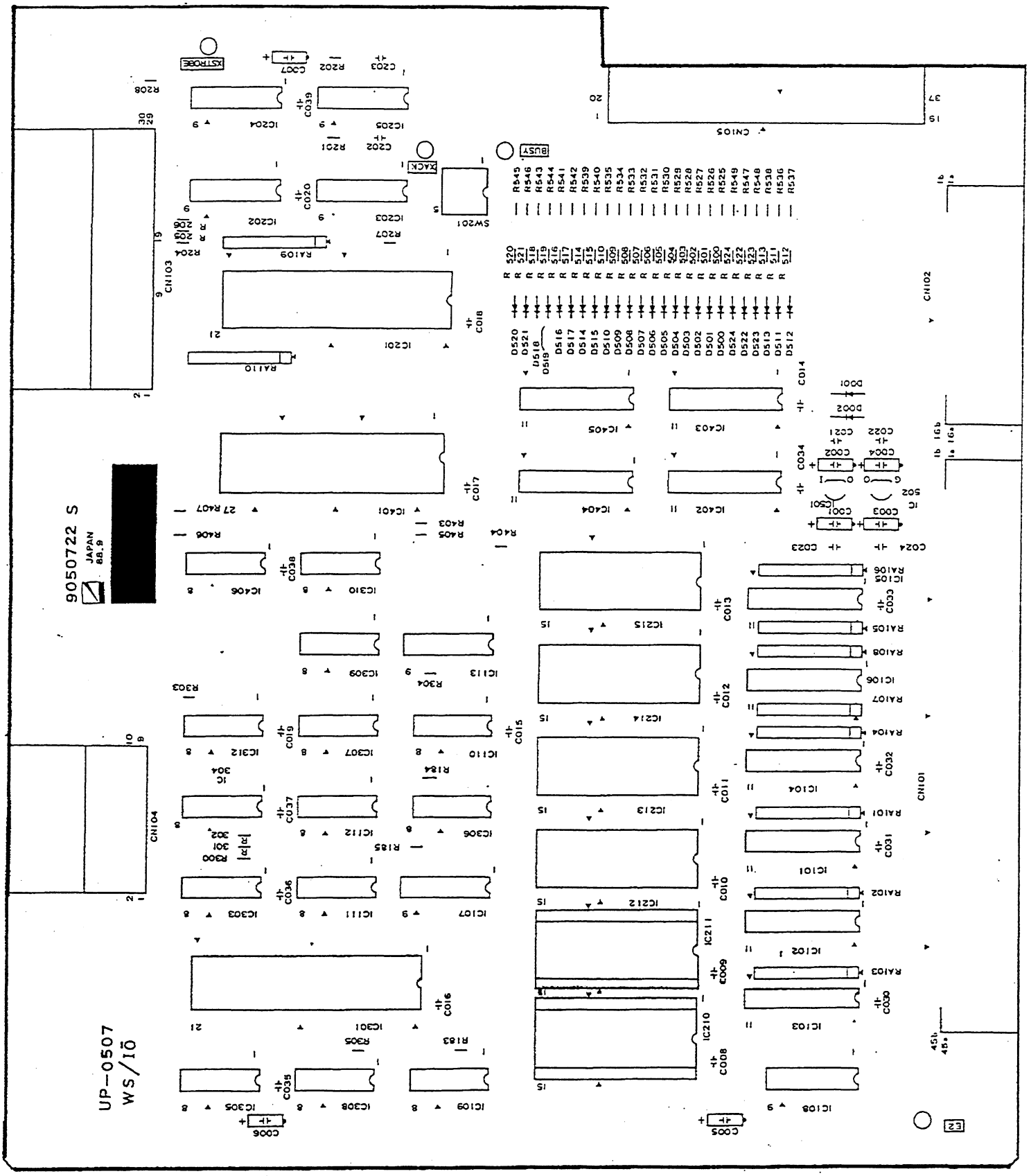

UP-0464 AD board
NIHON KOHDEN JAPAN 88-12
9046433-S UP-0464



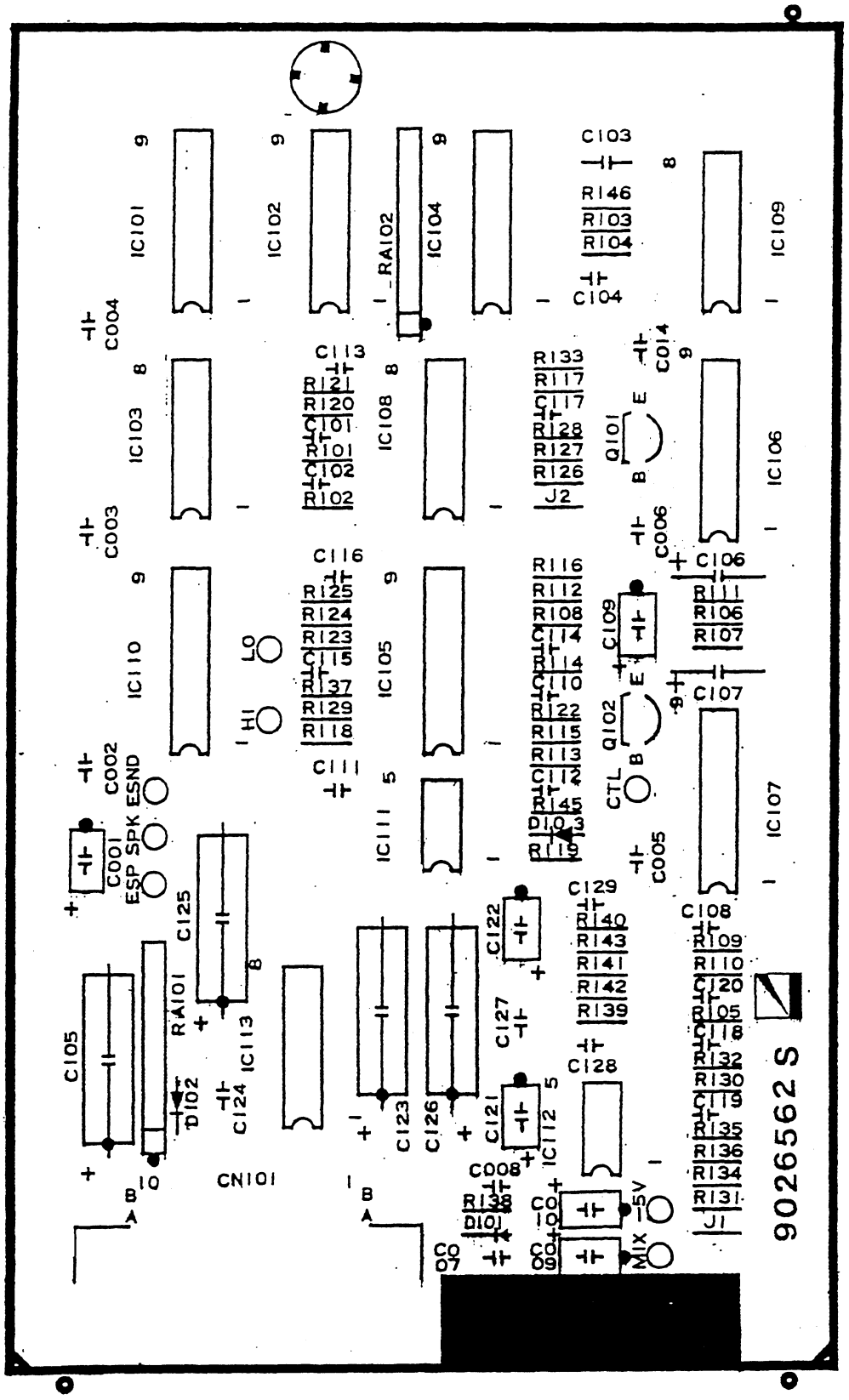
UP-0511 REC CNTL board



UP-0512
REC DRV board

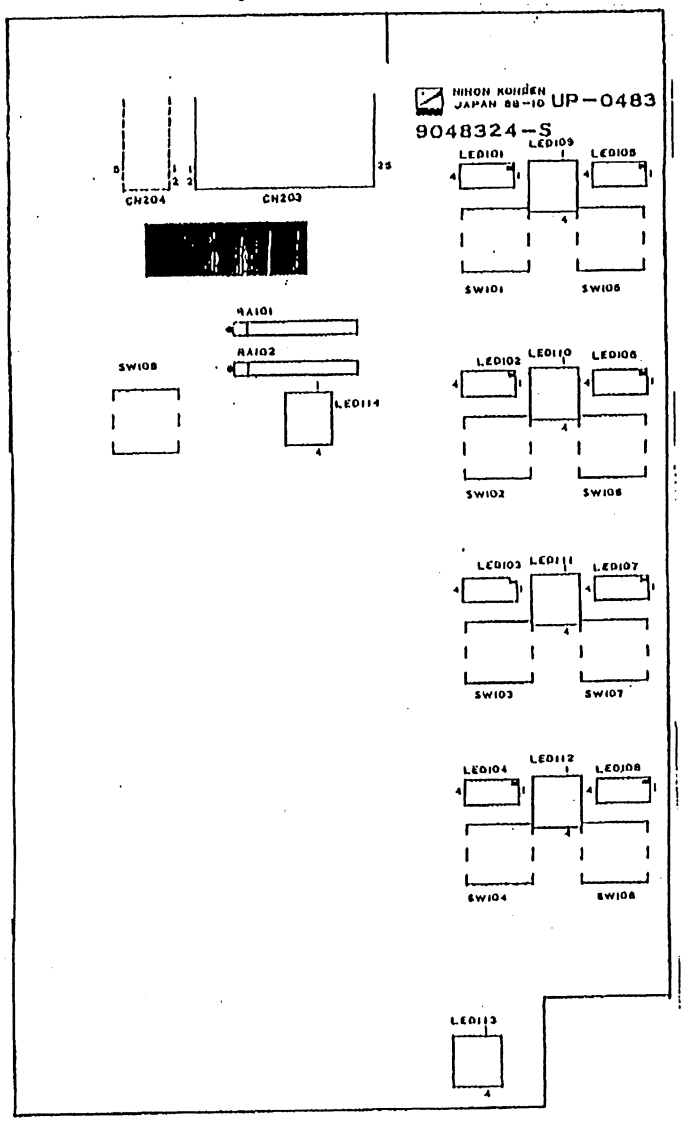


UP-0507
WS/IO board

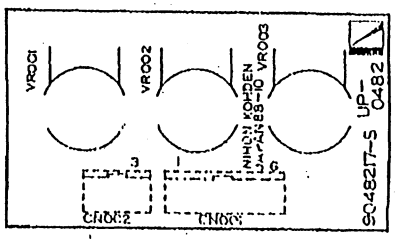


UP-0265 Sound control board

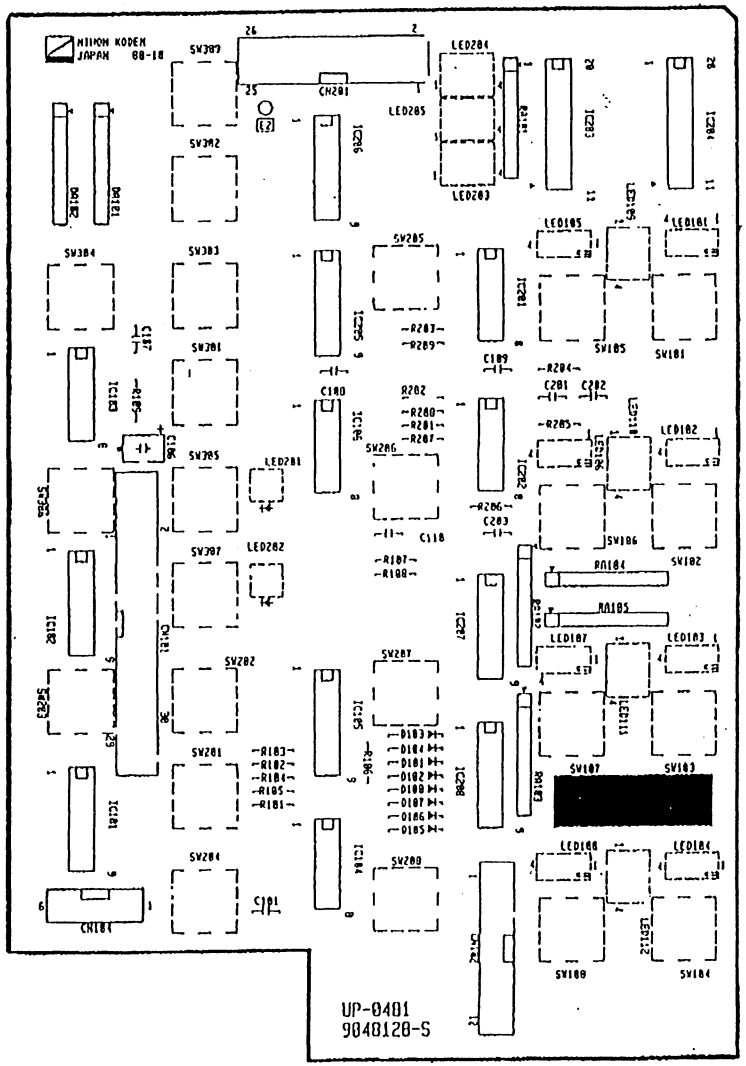
UP-0483 Operation board, left



UP-0482 Operation board, VR

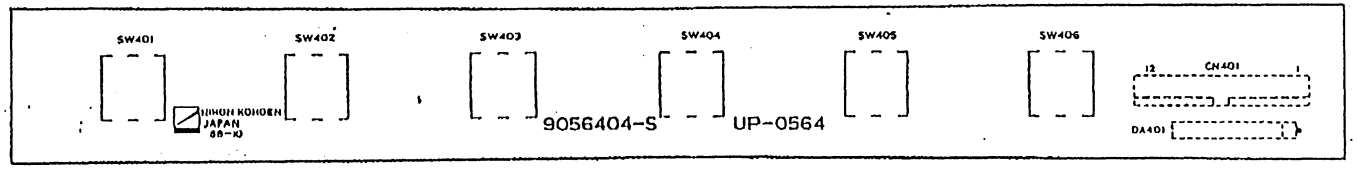


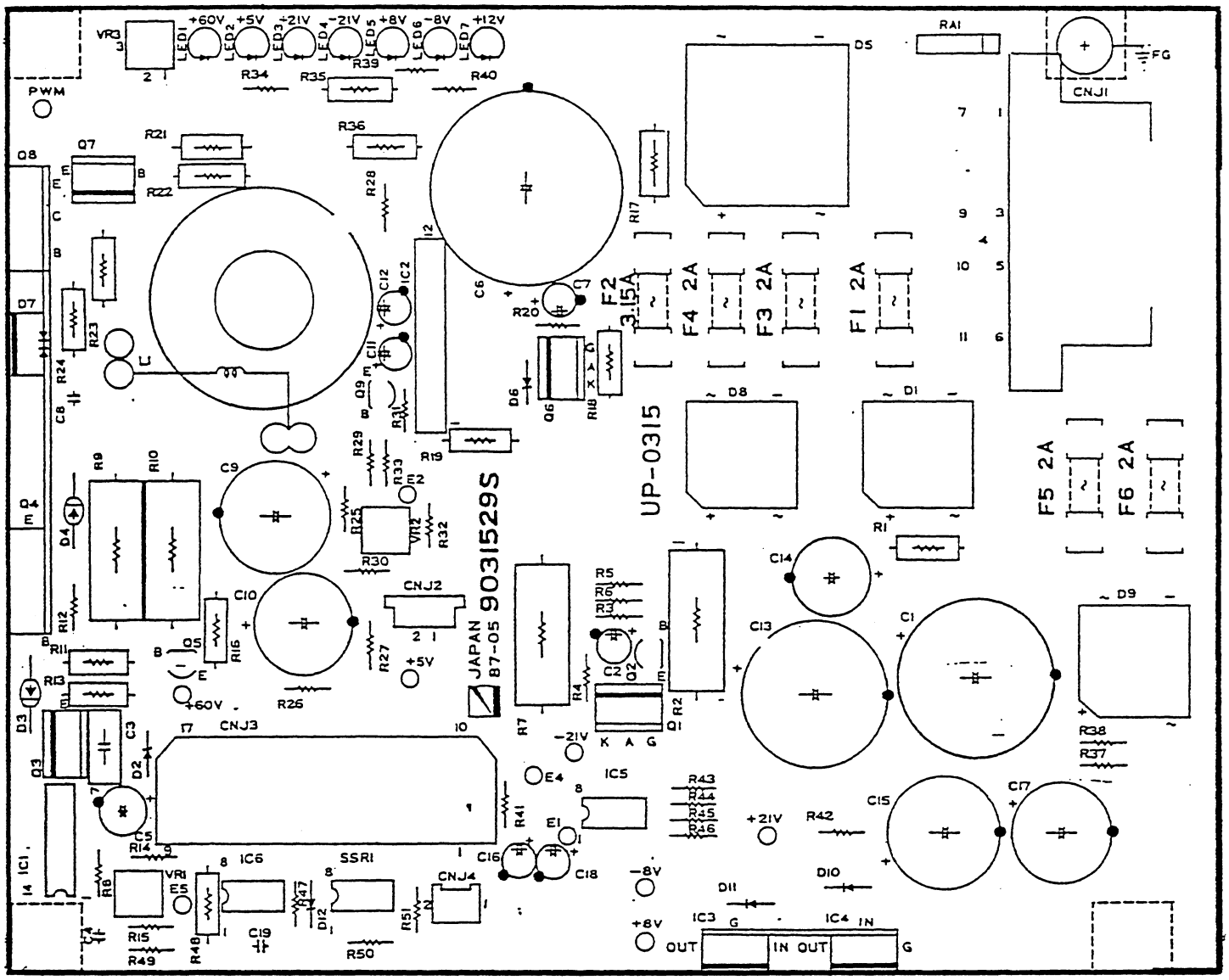
UP-0481 Operation board, main



NOTE: Switches are mounted on the opposite side.

UP-0564 Operation board, bottom





UP-0315
Regulator unit

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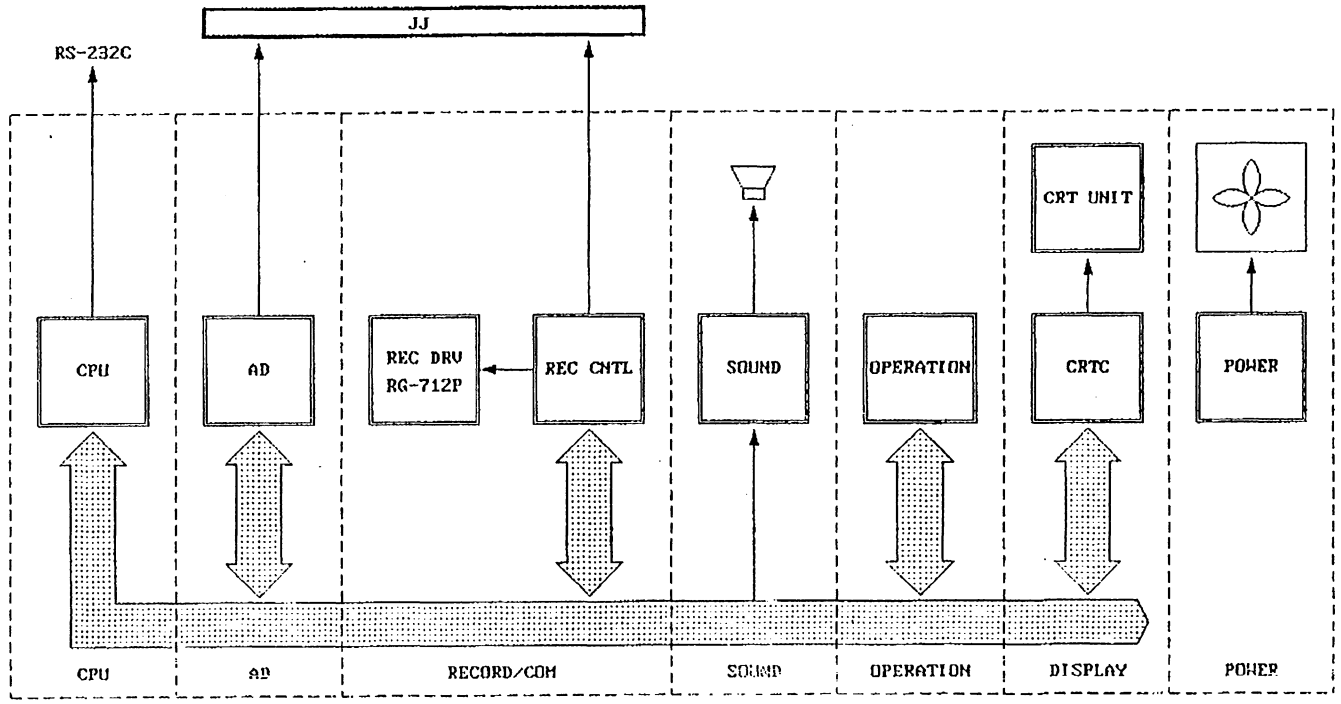
CNS SYSTEM BLOCK



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△X		– –		検図2 CHK 2		型式 MODEL	MU-820R
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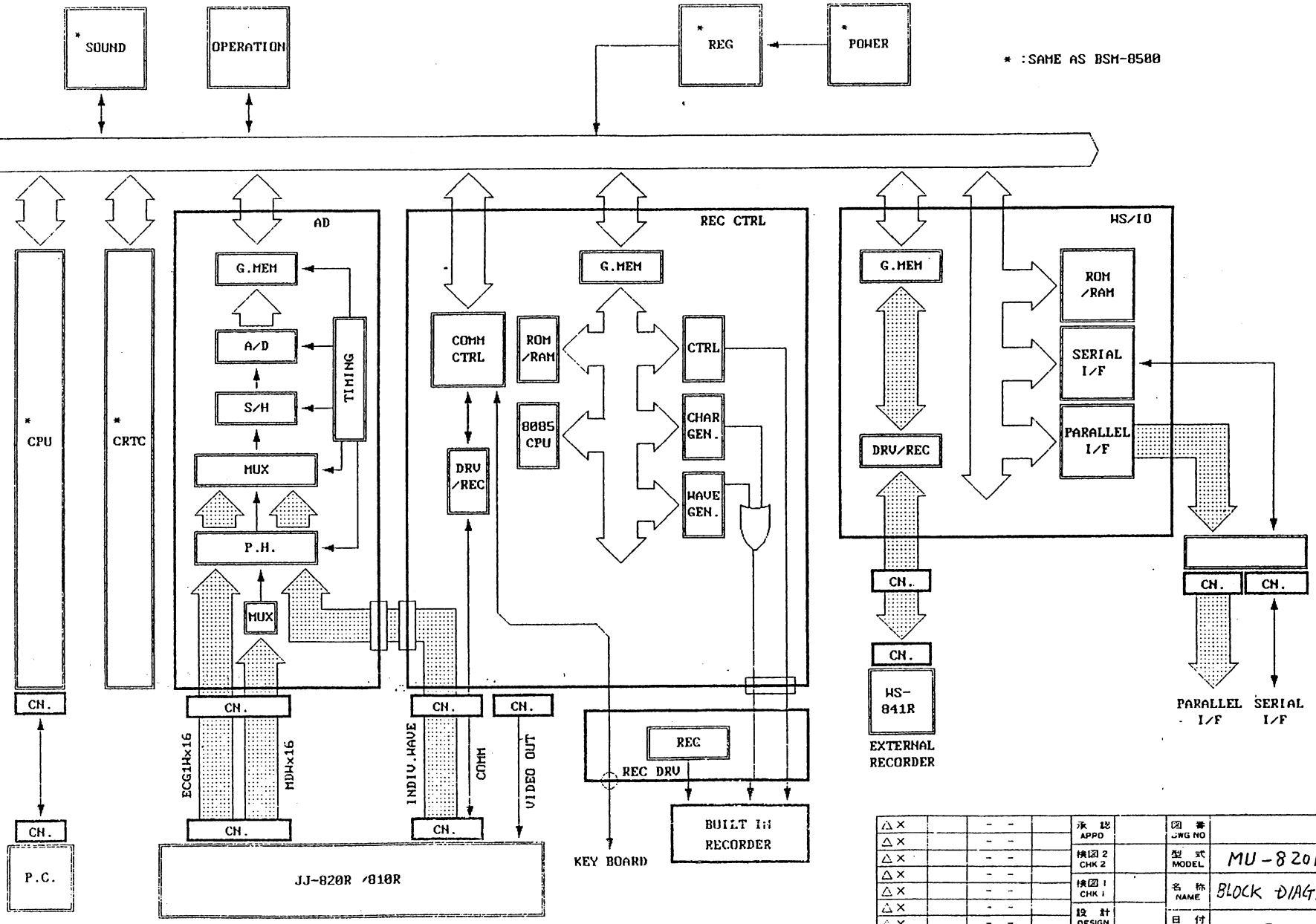
△X		– –		設計 DESIGN		日付 DATE	– –
△X		– –					
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE			日本光電

MU-820R FUNCTIONAL BLOCK DIAGRAM



変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	承認 APPD	図番 DWG NO	
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△×		- -		検図1 CHK 1	名称 NAME	BLOCK DIAGRAM
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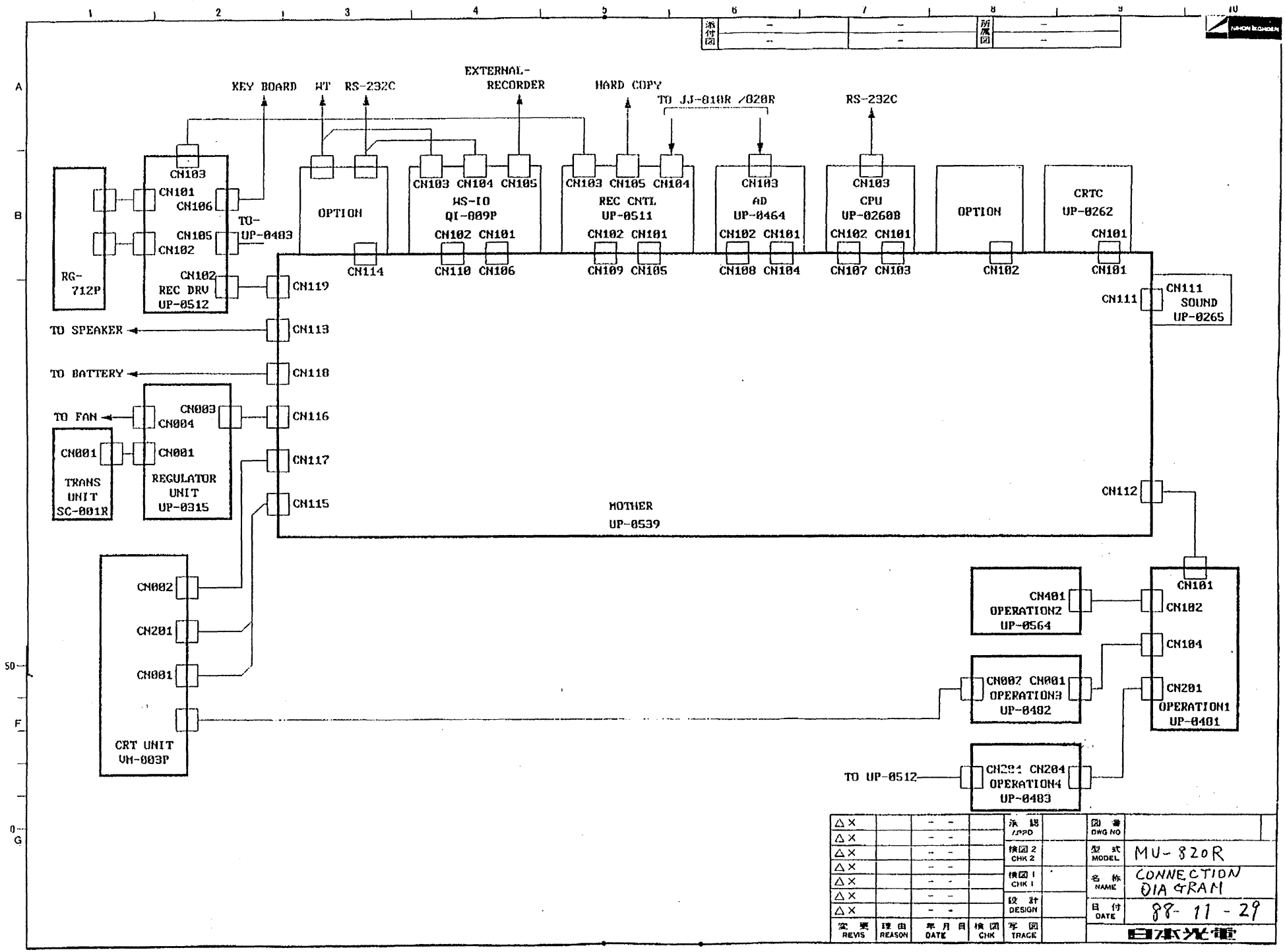
△×		- -		写図 TRACE		

日本光電



添付図	–	–	所属図	–
	–	–		–

変更 REVIS	理由 REASON	年月日 DATE	検図 CHK
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△×		– –	
△×		– –	
△×		– –	
△×		– –	
△×		– –	
△×		– –	

承認 APPD	
検図2 CHK 2	
検図1 CHK 1	
設計 DESIGN	
写図 TRACE	

図番 DWG NO	
型式 MODEL	MU-820R
名称 NAME	CONNECTION DIAGRAM
日付 DATE	88-11-29

日本光電

添付図	–	–	所属図	–
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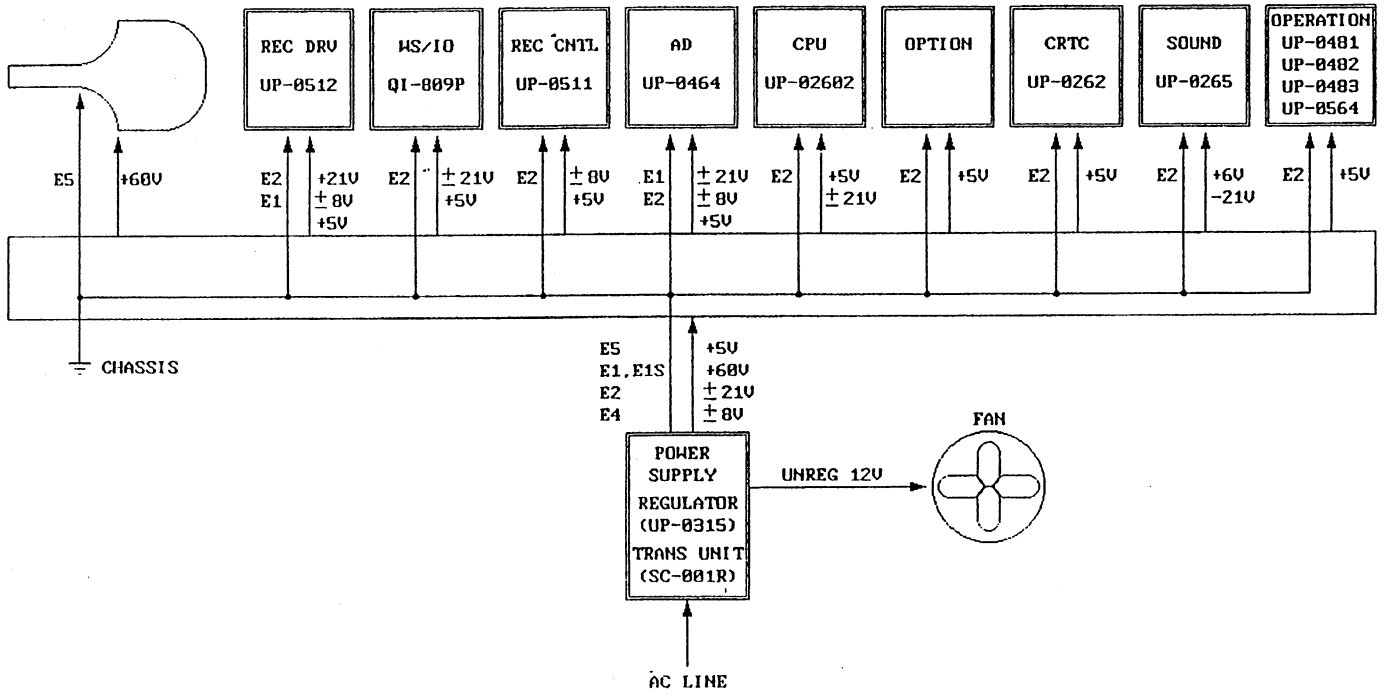

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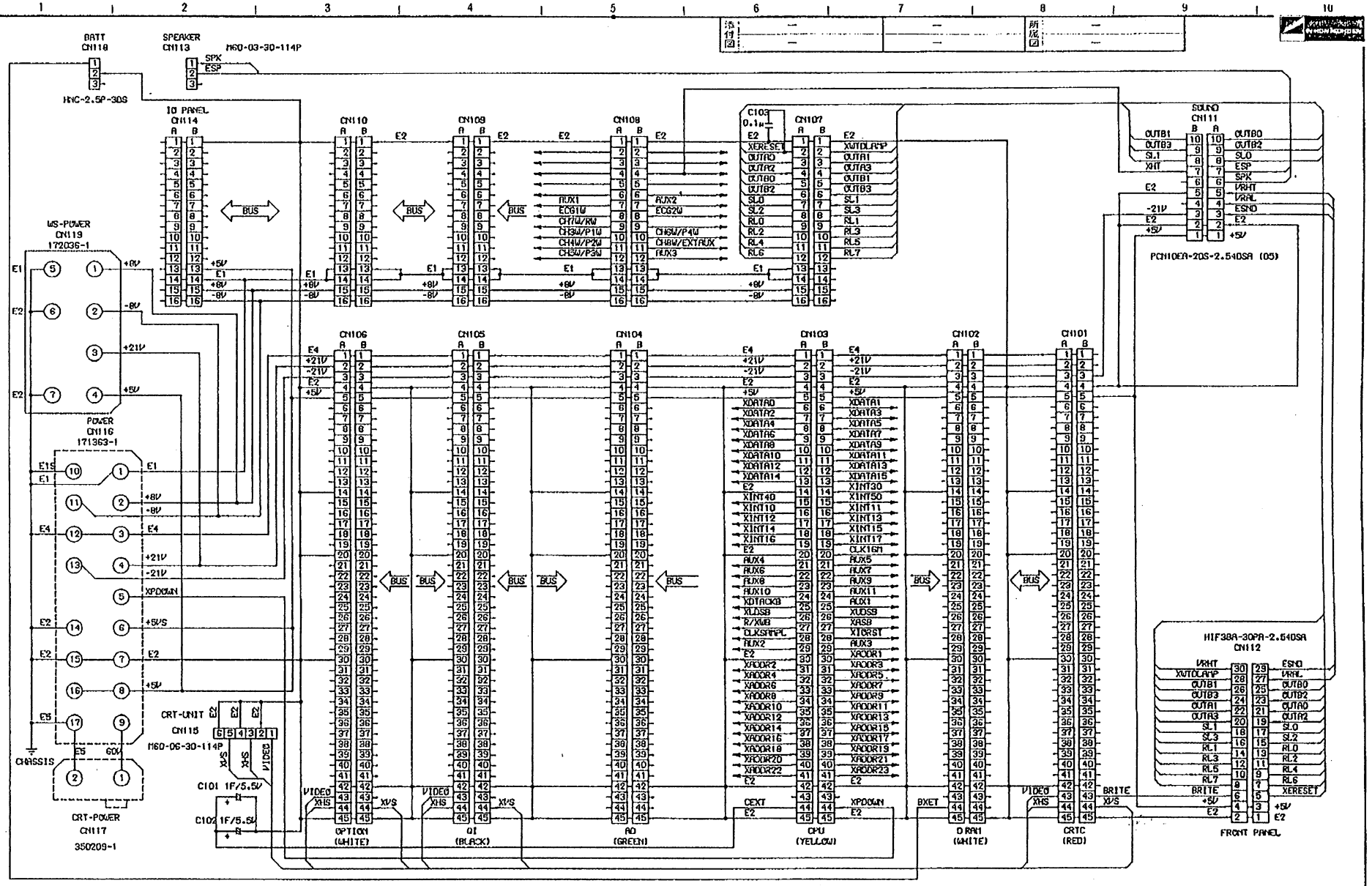
△×		– –		検図1 CHK 1		名称 NAME	POWER SUPPLY FLOW
△×		– –		設計 DESIGN		日付 DATE	– –
△×		– –					
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE			日本光電



※ CN101~CN106 : PCN10EA-90S-2.54DSA (05)
CN107~CN110 : PCN10EA-32S-2.54DSA (05)
CN114

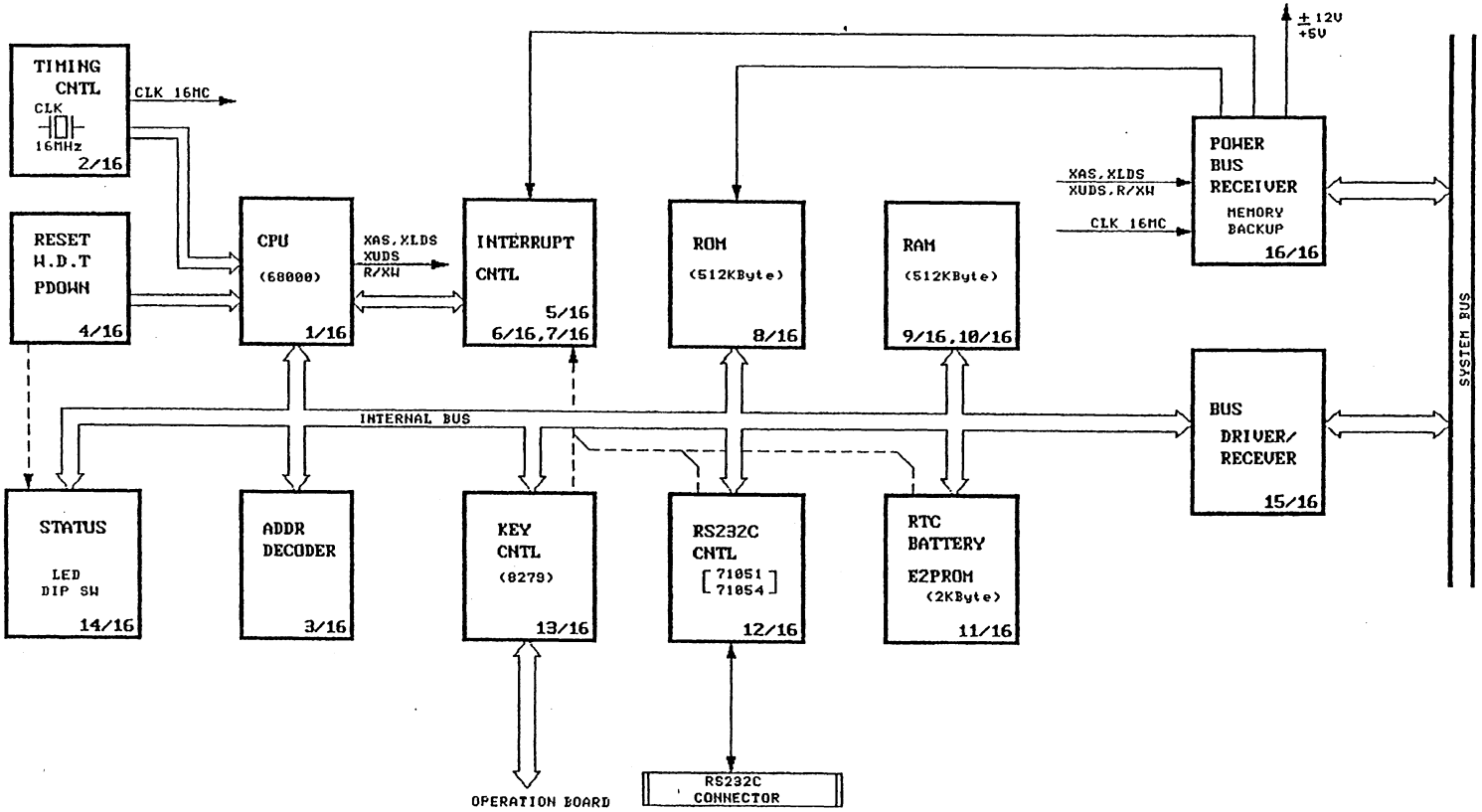
※ CN101~CN106 : 6~41 A,B BUS CONNECT
※ CN108~CN110,CN114 : 2~12 A,B BUS CONNECT

REVIS	REASON	DATE	CHK
△×		- -	
△×		- -	
△×		- -	
△×		- -	
△×		- -	
△×		- -	
△×		- -	

承認 APPD	
検図2 CHK 2	荒金
検図1 CHK 1	木下
設計 DESIGN	緑川
製図 TRACE	山田

図番 DWG NO	106267
型式 MODEL	UP-0539
名称 NAME	CNS-MOTHER
日付 DATE	88 - 11 - 22

日本光電

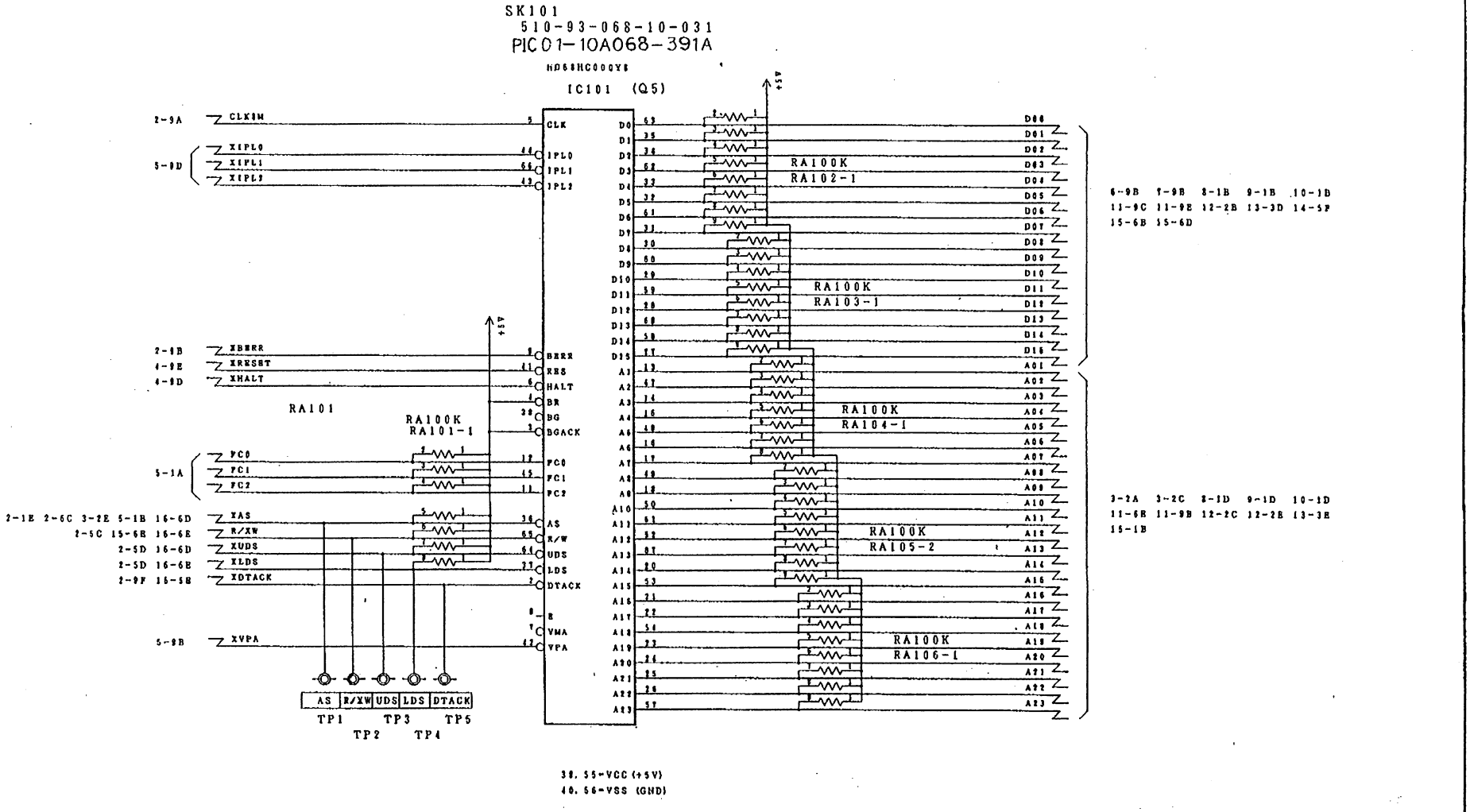


添付図			所属図	
—	—	—	—	—

変更 REVIS	理由 REASON	年月日 DATE	検図 CHK
△×		- -	
△×		- -	
△×		- -	
△×		- -	
△×		- -	
△×		- -	
△×		- -	

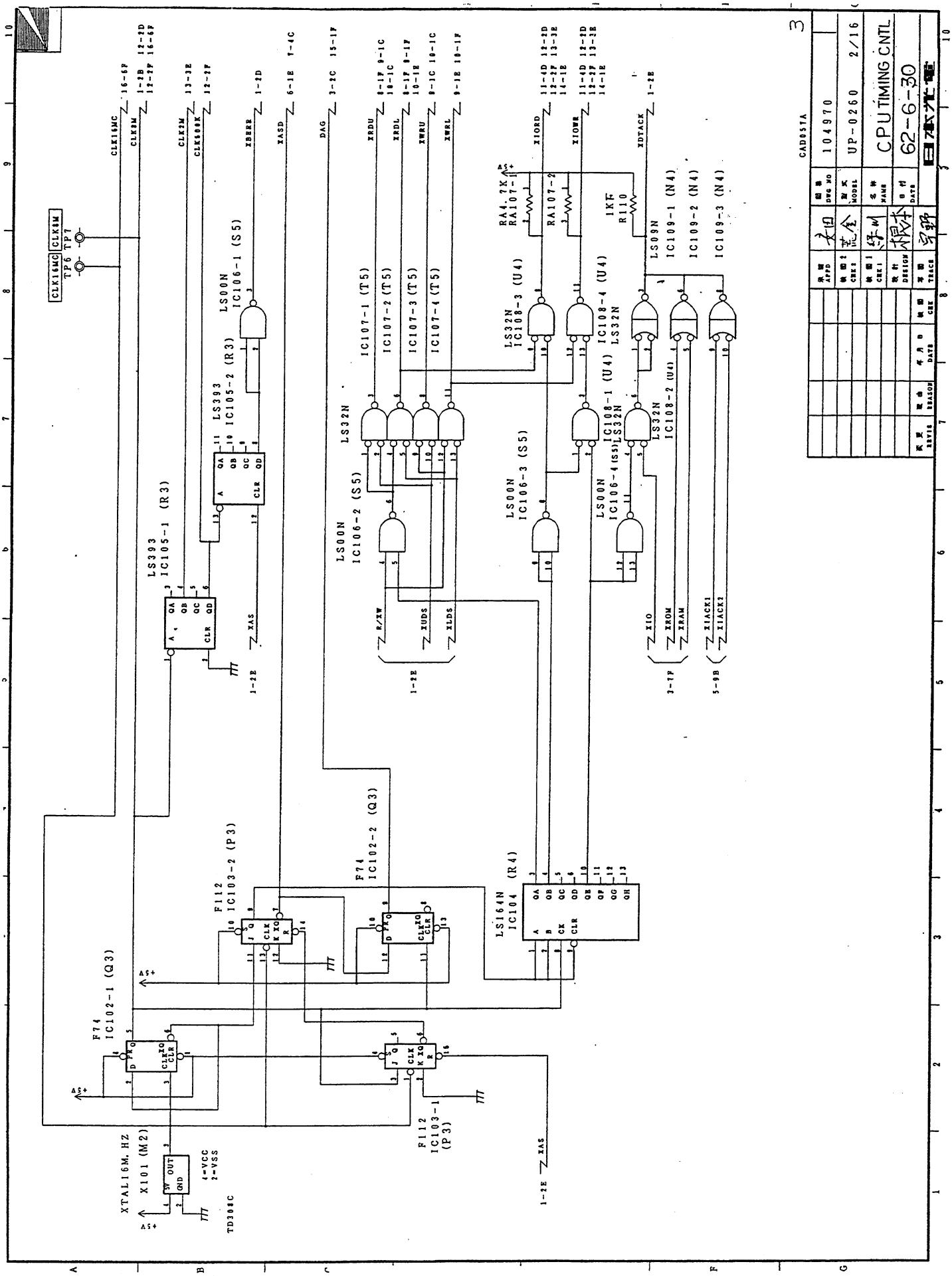
承認 APPD	吉田	図番 DWG NO	105422
検図2 CHK 2	荒金	型式 MODEL	UP-0260
検図1 CHK 1	緑川	名称 NAME	CPU BLOCK DIAGRAM
設計 DESIGN	根本	日付 DATE	62- 7-14
写図 TRACE	斉藤	日本光電	

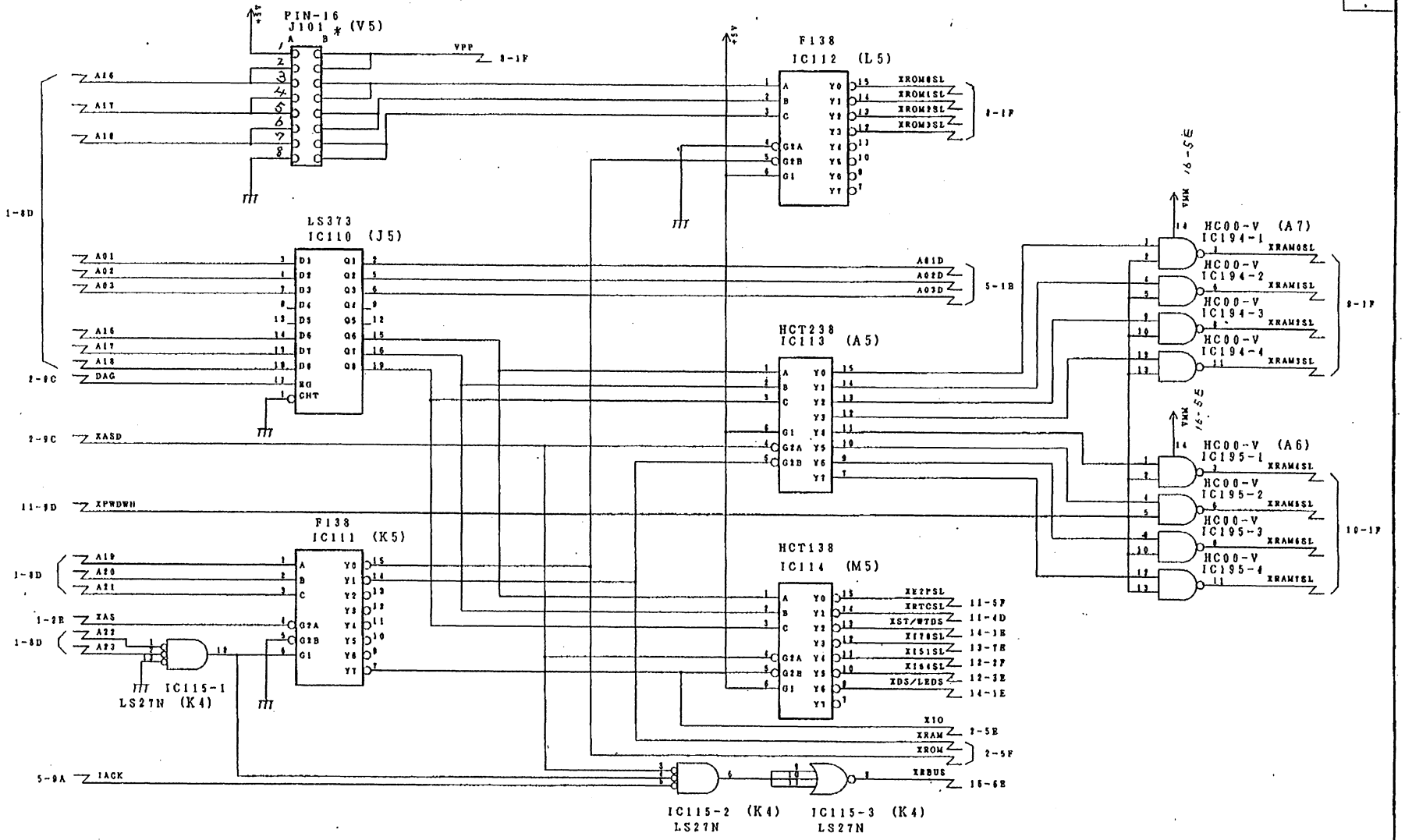
3



CAD051A 3

				承認 APPD	永田	図番 DRG NO	104969
				検図2 CHK 2	荒金	型式 MODEL	UP-0260 1/16
				検図1 CHK 1	緑川	名称 NAME	CPU CPU
				設計 DESIGN	根本	日付 DATE	62-6-30
改訂 REVIS	理由 REASON	年月日 DATE	検図 CHK	作図 TRACE	宇野	日本電気	


CPU TIMING CNTL
UP-0260
104970
62-6-30
2/16
CADDSTA
XTAL16M, HZ
X101 (M2)
TD303C
IC102-1 (Q3)
IC102-2 (Q3)
IC103-2 (P3)
IC103-1 (P3)
IC104 (R4)
IC105-1 (R3)
IC105-2 (R3)
IC106-1 (S5)
IC106-2 (S5)
IC106-3 (S5)
IC106-4 (S5)
IC107-1 (T5)
IC107-2 (T5)
IC107-3 (T5)
IC107-4 (T5)
IC108-1 (U4)
IC108-2 (U4)
IC108-3 (U4)
IC108-4 (U4)
IC109-1 (N4)
IC109-2 (N4)
IC109-3 (N4)
RA4.7K
RA107-1
RA107-2
1KF
R110
CLK16MC
CLK8M
CLK4M
CLK500K
XBERR
XASD
XAS
DAG
XRDU
XRDL
XWRU
XWRL
XIORD
XIOWR
XDTACK
XUDS
XLDS
R/XW
XIO
XROM
XRAM
XIACK1
XIACK2



* 27256 ROM:

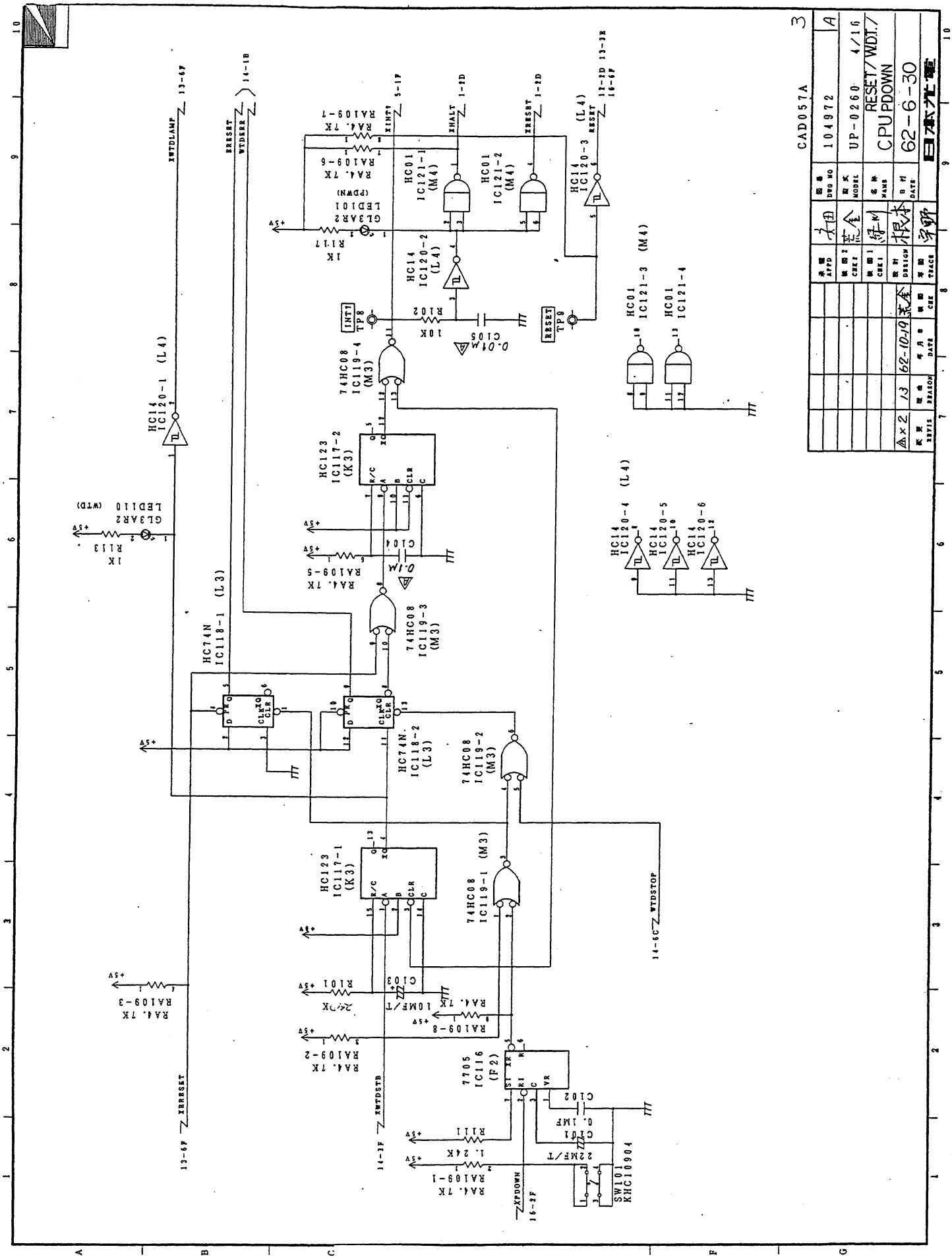
J101 1A-B, 3A-B, 5A-B, 7A-B : Shortened

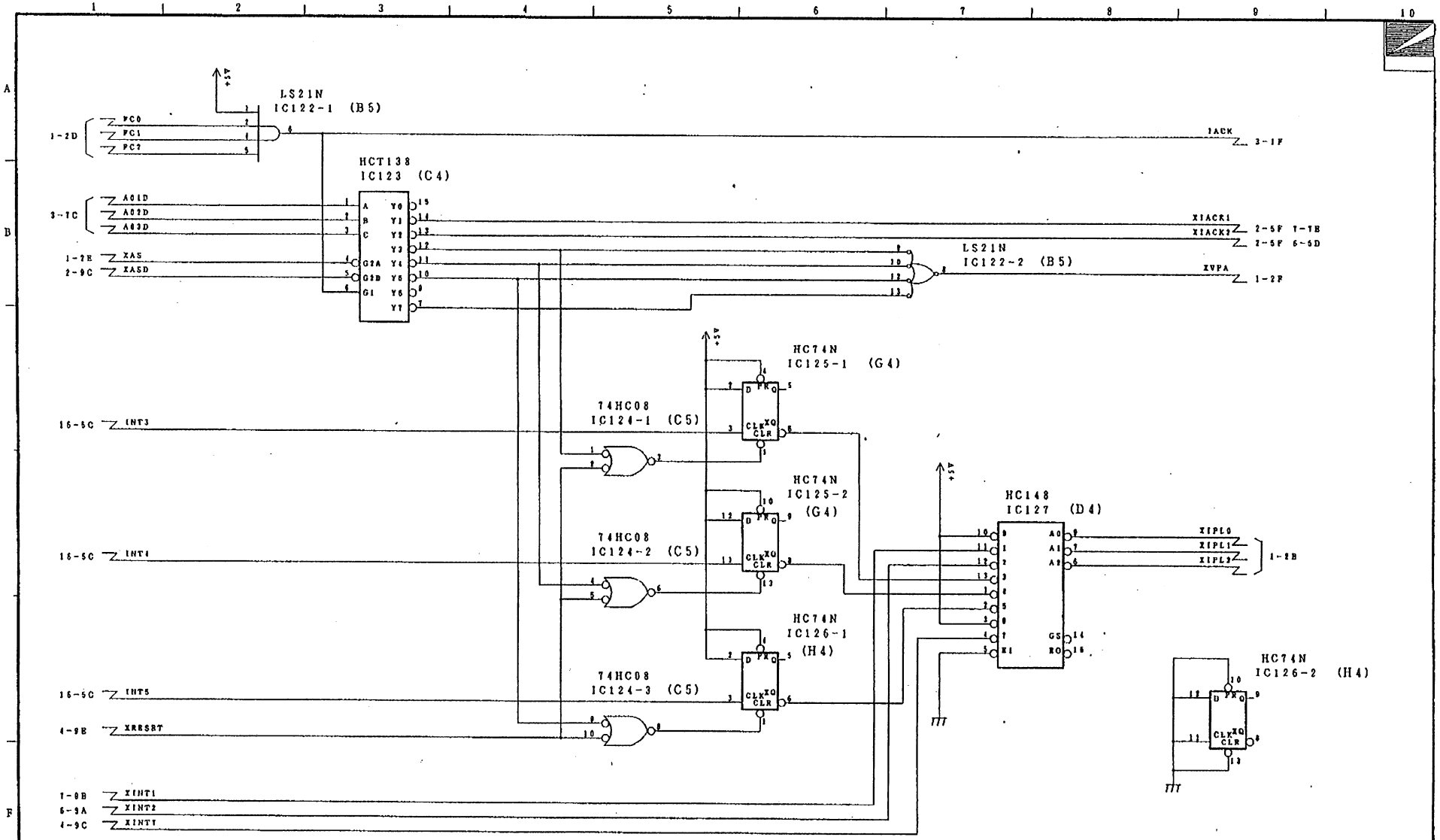
27512 ROM:

J101 2A-B, 4A-B, 6A-B, 8A-B : Shortened

				APPD	高田	DWG NO	104971
				CHK 2	荒金	MODEL	UP-0260 3/16
				CHK 1	緑川	NAME	CPU ADDR DECODER
				DESIGN	根本	DATE	62-6-30
REVIS	REASON	DATE	CHK	TRACE	宇野		日本光電

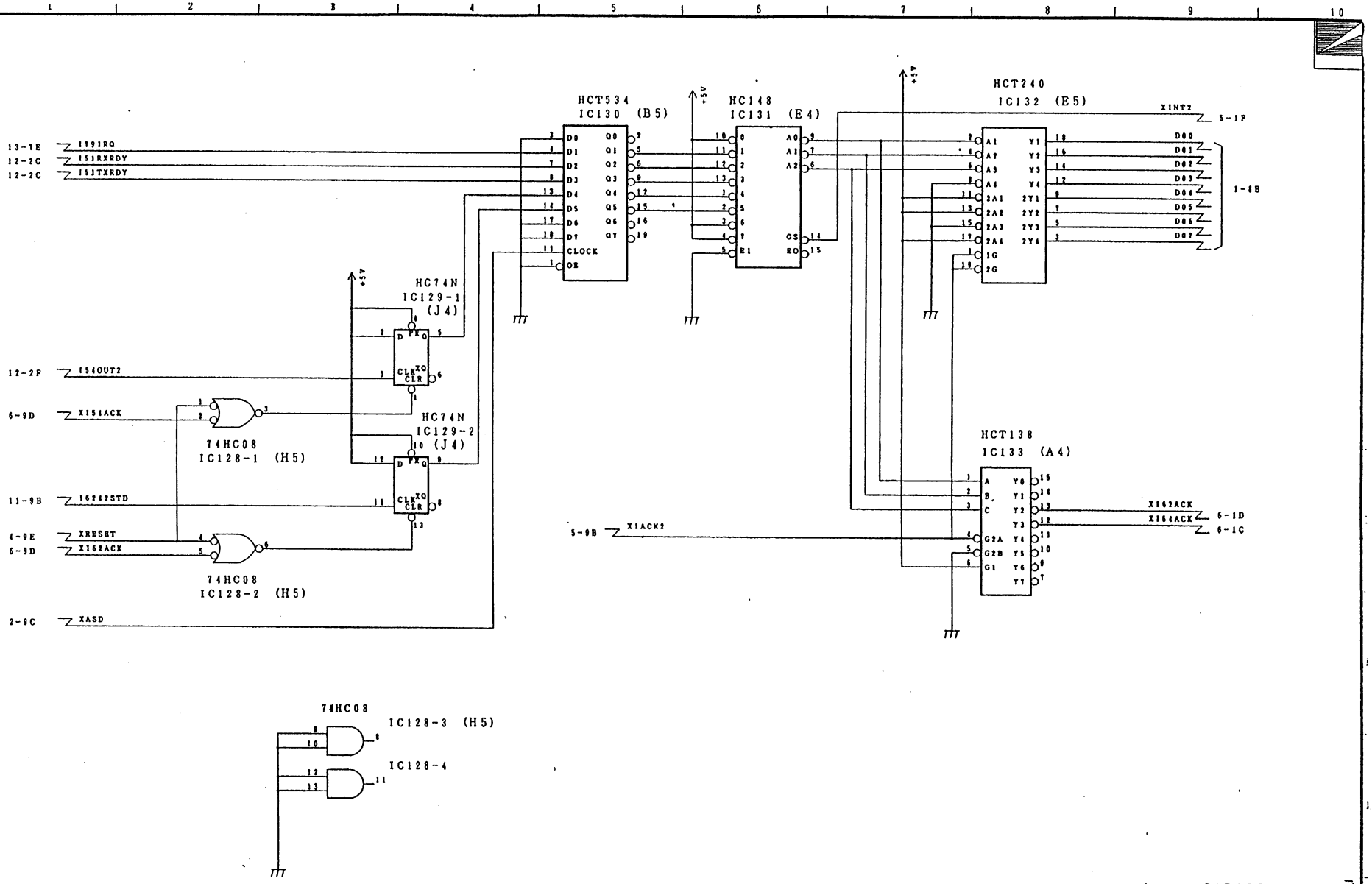
CAD05TA 3


CAD057A
104972
UP-0260
RESET/WDT./CPUPDOWN
62-6-30
日本光電
HC14 IC120-1 (L4)
HC14 IC120-2 (L4)
HC14 IC120-3 (L4)
HC14 IC120-4 (L4)
HC14 IC120-5
HC14 IC120-6
HC01 IC121-1 (M4)
HC01 IC121-2 (M4)
HC01 IC121-3 (M4)
HC01 IC121-4
74HC08 IC119-4 (M3)
74HC08 IC119-3 (M3)
74HC08 IC119-2 (M3)
74HC08 IC119-1 (M3)
HC74N IC118-1 (L3)
HC74N IC118-2 (L3)
HC123 IC117-2 (K3)
HC123 IC117-1 (K3)
7705 IC116 (F2)
RA4. 7K RA109-1
RA4. 7K RA109-2
RA4. 7K RA109-3
RA4. 7K RA109-5
RA4. 7K RA109-6
RA4. 7K RA109-7
RA4. 7K RA109-8
1K R113
1K R117
10K R102
24K R101
1.24K R111
0.01M C105
0.1M C104
10MF/T C103
22MF/T C101
0.1MF C102
LED110 GL3AR2 (WTD)
LED101 GL3AR2 (PDWN)
SW101 XHC10904
TP8 INT1
TP9 RESET
XWTDLAMP
XRRESET
XWTDSTB
XPDOWN
WTDSTOP
XINT1
XHALT
XRESET
+5V



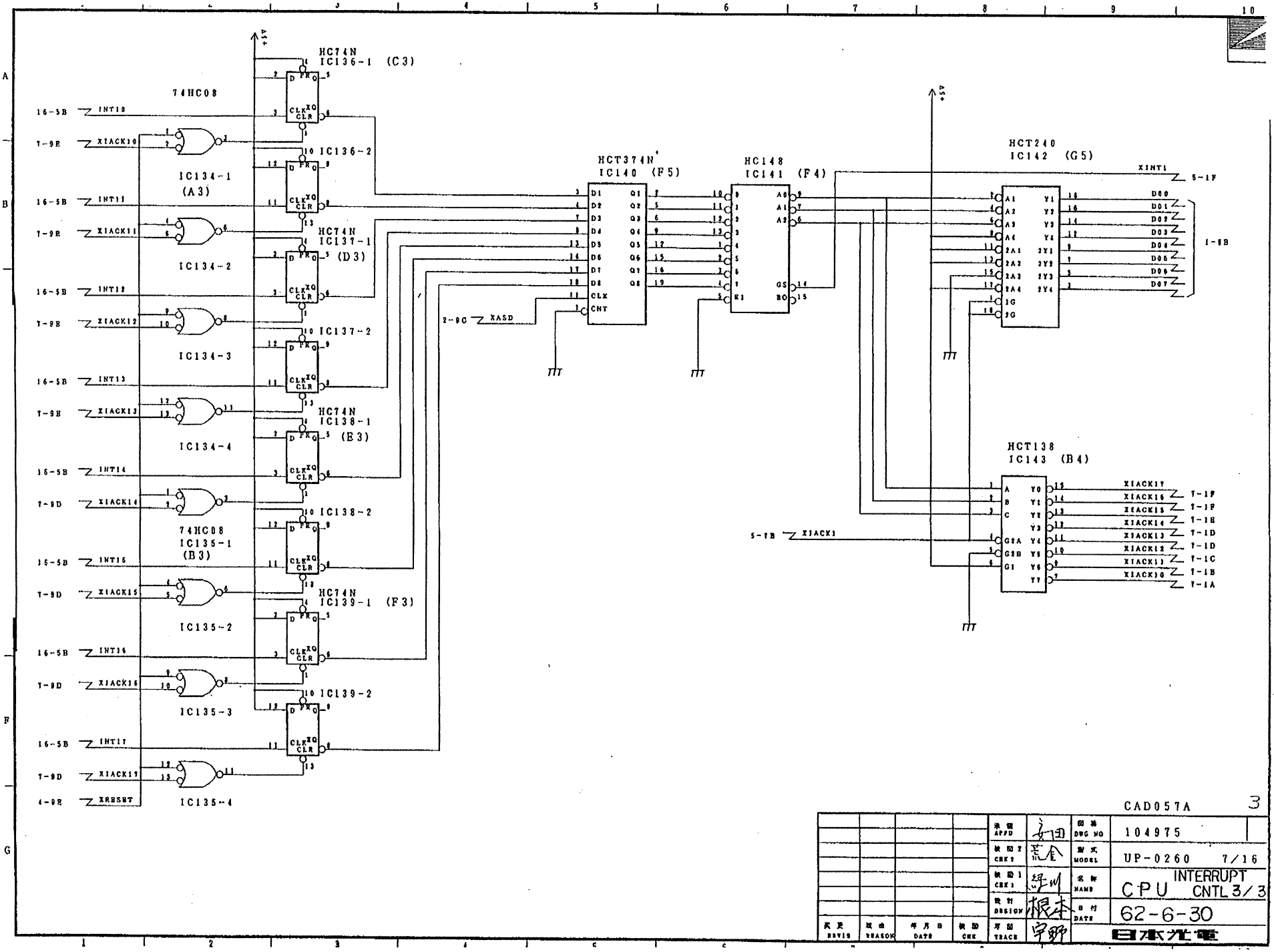
CAD057A

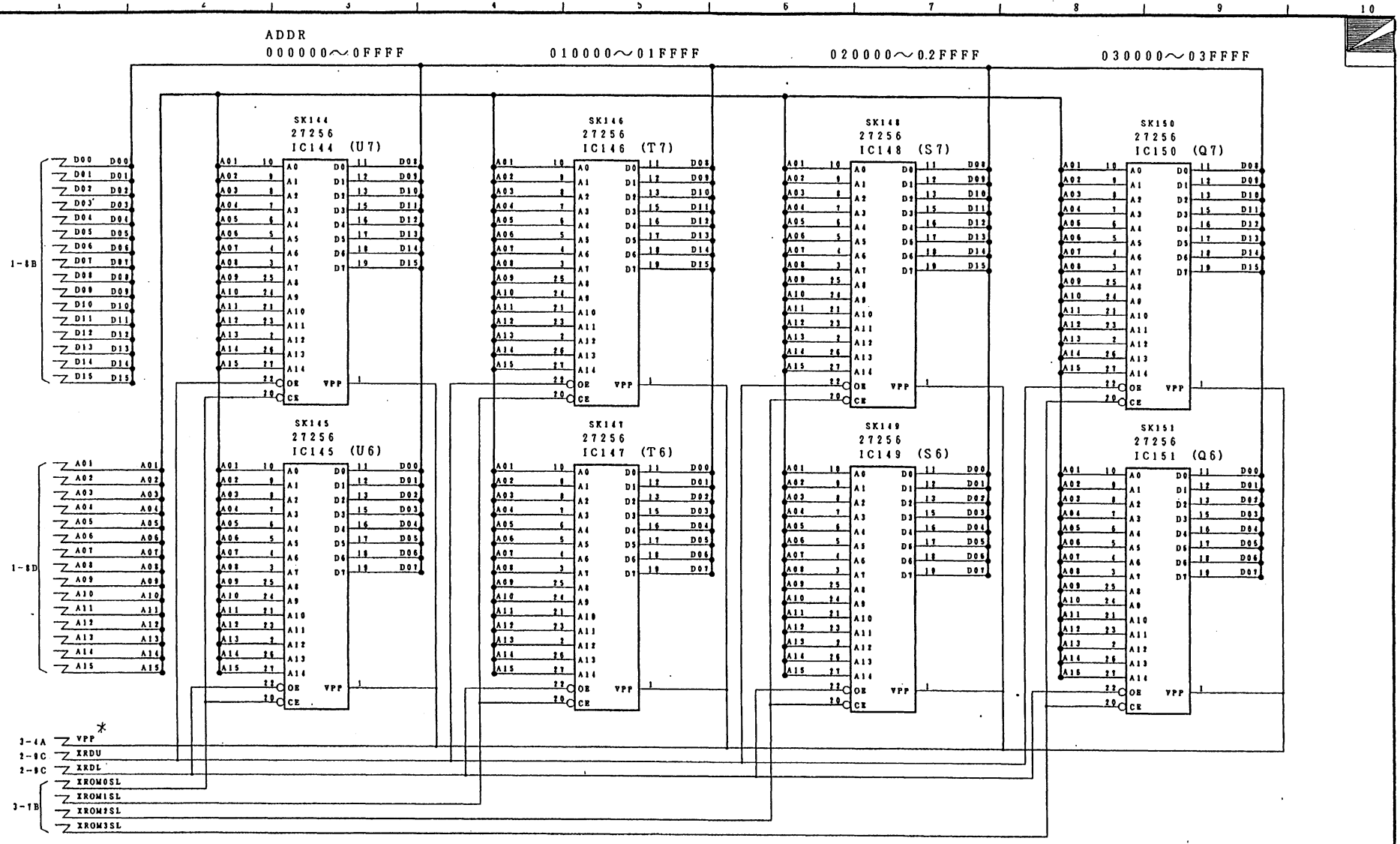
					承認 APPD	文田	図番 DWG NO	104973
					検図2 CHK 2	荒金	型式 MODEL	UP-0260 5/16
					検図1 CHK 1	鈴川	名称 NAME	INTERRUPT CPU CNTL 1/3
					設計 DESIGN	根本	日付 DATE	62-6-30
改定 REVIS	理由 REASON	年月日 DATE	検図 CHK		写図 TRACE	宇野	日本光電	



				承認 APPD	永田	図番 DWG NO	104985
				検図2 CHK 2	荒金	型式 MODEL	UP-0260 6/11
				検図1 CHK 1	緑川	名称 NAME	INTERRUPT CPU CNTL 2/3
				設計 DESIGN	根本	日付 DATE	62-6-30
改更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE	宇野	日本光電	

CAD057A


74HC08
IC134-1 (A3)
IC134-2
IC134-3
IC134-4
74HC08
IC135-1 (B3)
IC135-2
IC135-3
IC135-4
HC74N
IC136-1 (C3)
IC136-2
IC137-1 (D3)
IC137-2
IC138-1 (E3)
IC138-2
IC139-1 (F3)
IC139-2
HCT374N
IC140 (F5)
HC148
IC141 (F4)
HCT240
IC142 (G5)
HCT138
IC143 (B4)
INT10
INT11
INT12
INT13
INT14
INT15
INT16
INT17
XIACK10
XIACK11
XIACK12
XIACK13
XIACK14
XIACK15
XIACK16
XIACK17
XRESET
XASD
XINT1
XIACK1
CAD057A
3
104975
UP-0260 7/16
INTERRUPT CPU CNTL 3/3
62-6-30
日本光電



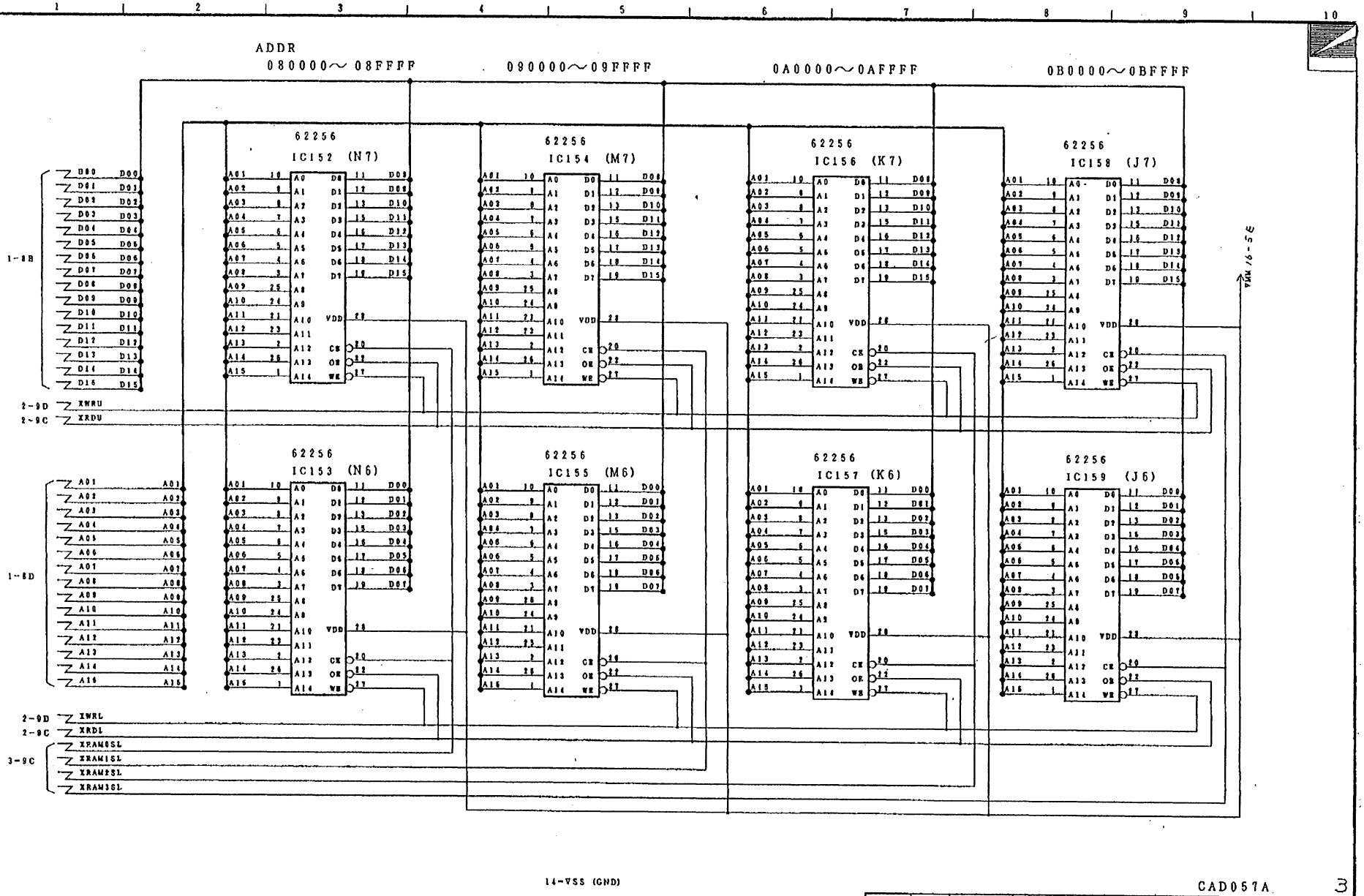
SK144～SK151: DL-2-28A

28-VCC (+5V)
14-VSS (GND)

If 27512 ROMs on IC144～IC151, $\overline{Vpp}$ is A16.

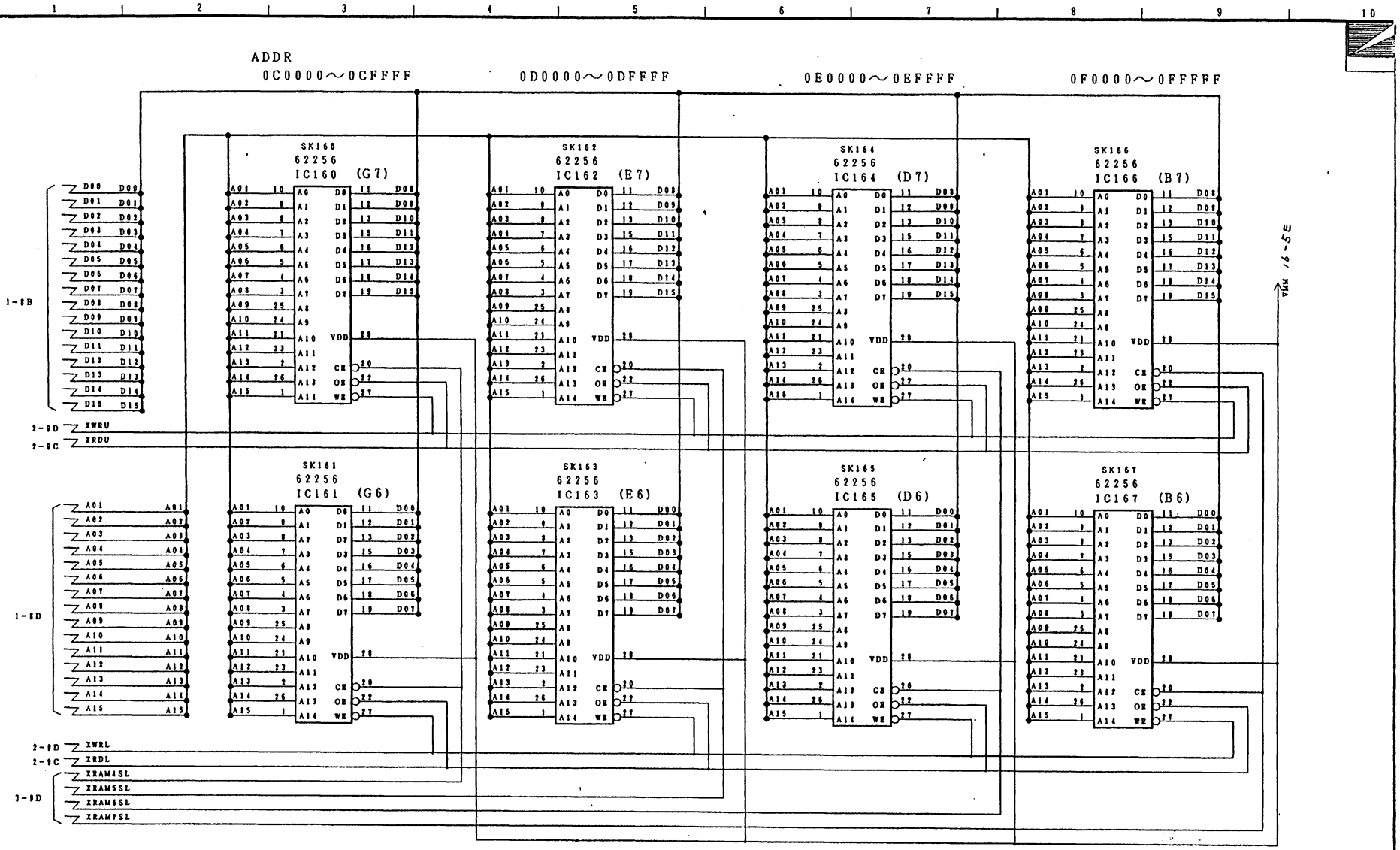
CAD057A 3

				承認 APPD	安田	図番 DWG NO	104976
				検図2 CHK 2	荒金	型式 MODEL	UP-0260 8/16
				検図1 CHK 1	近川	名称 NAME	CPU ROM
				設計 DESIGN	根本	日付 DATE	62-6-30
改版 REVIS	改由 REASON	年月日 DATE	検図 CHK	写図 TRACE	宇野	日本光電	



CAD057A 3

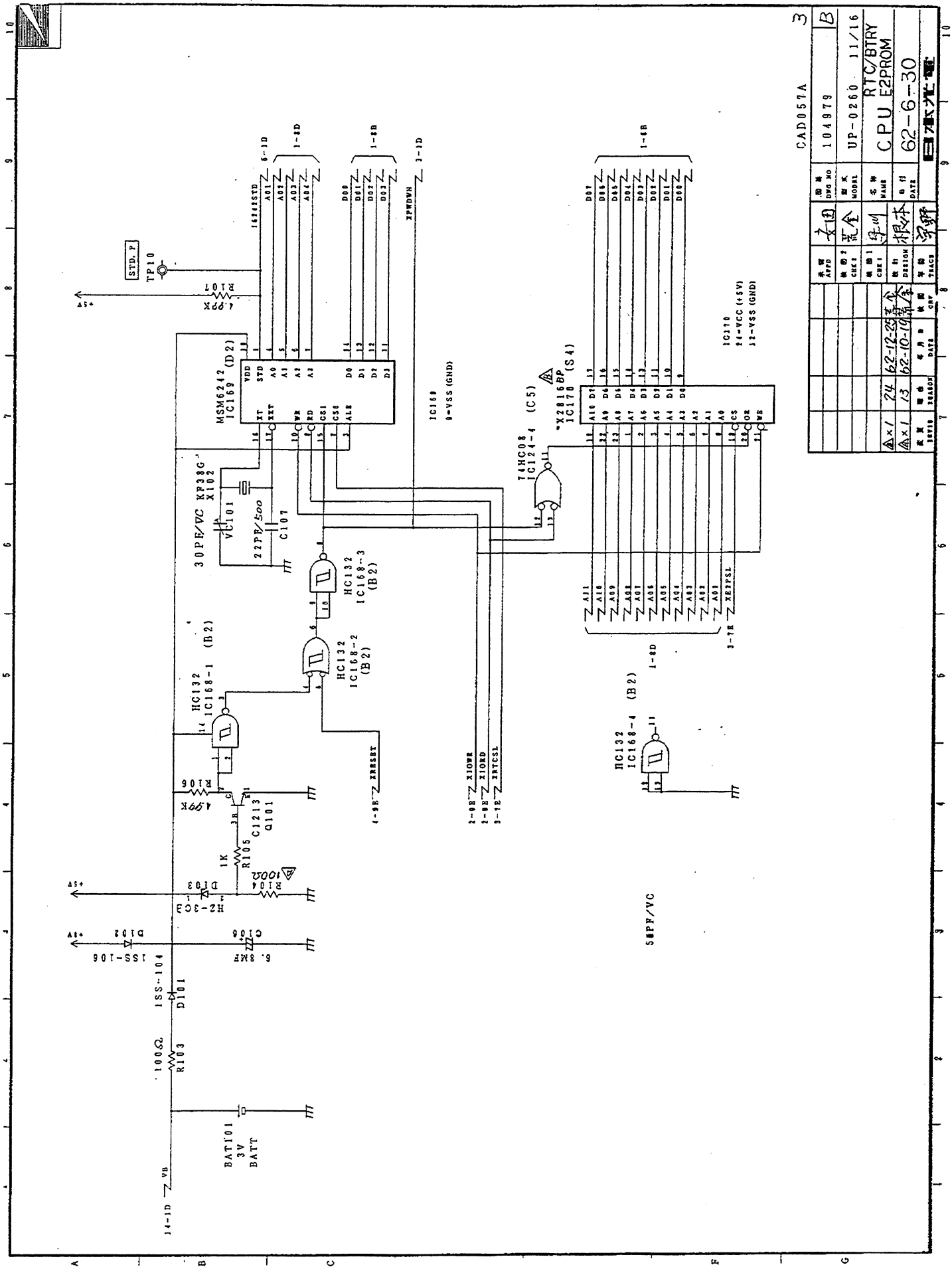
				承認 APPD	安田	図番 DWG NO	104977
				検図2 CHK 2	荒金	型式 MODEL	UP-0260 9/16
				検図1 CHK 1	坪川	名称 NAME	CPU RAM 1/2
				設計 DESIGN	根本	日付 DATE	62-6-30
改更 REVIS	改由 REASON	年月日 DATE	検図 CHK	写図 TRACE	宇野	日本電	

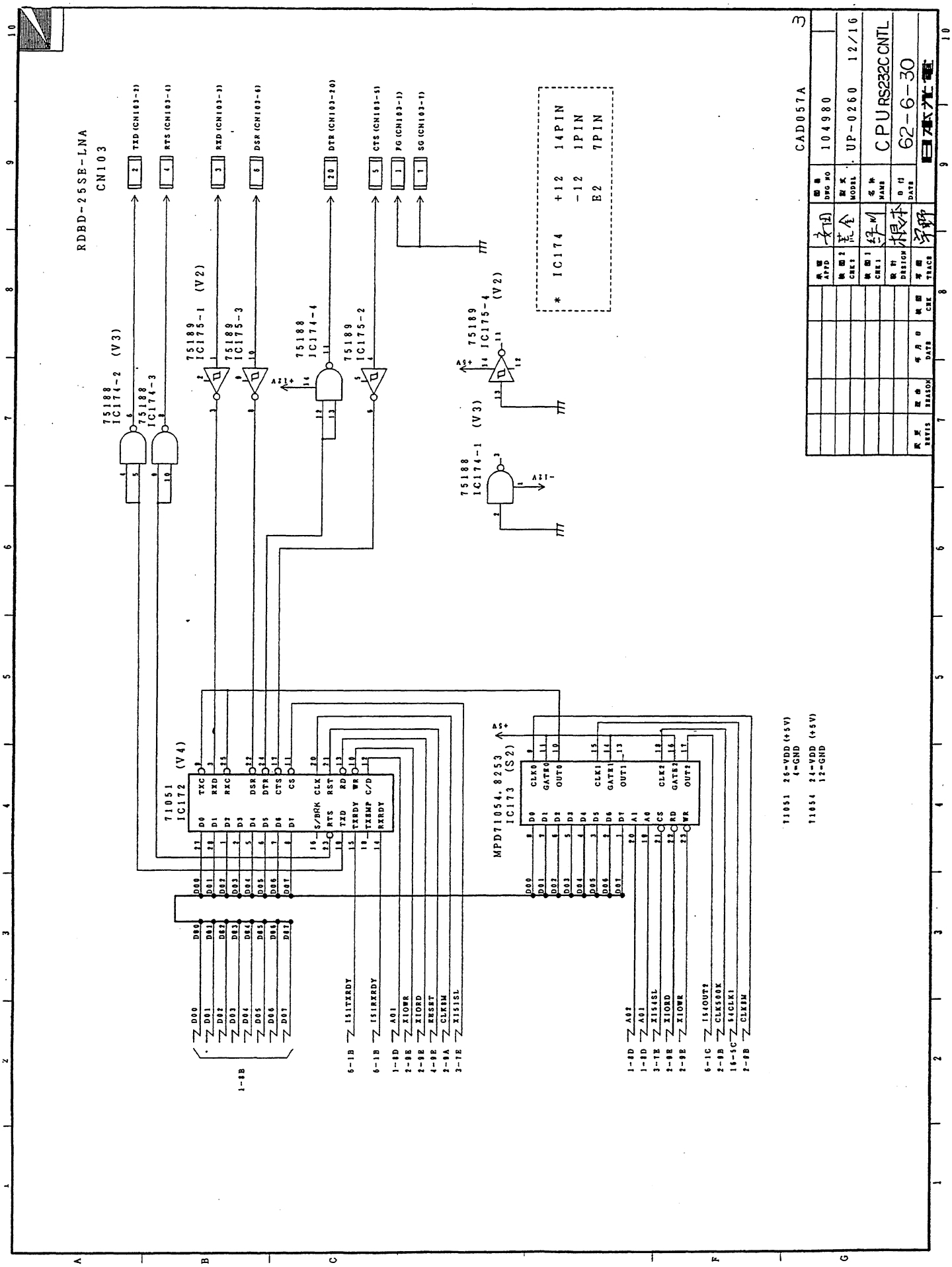


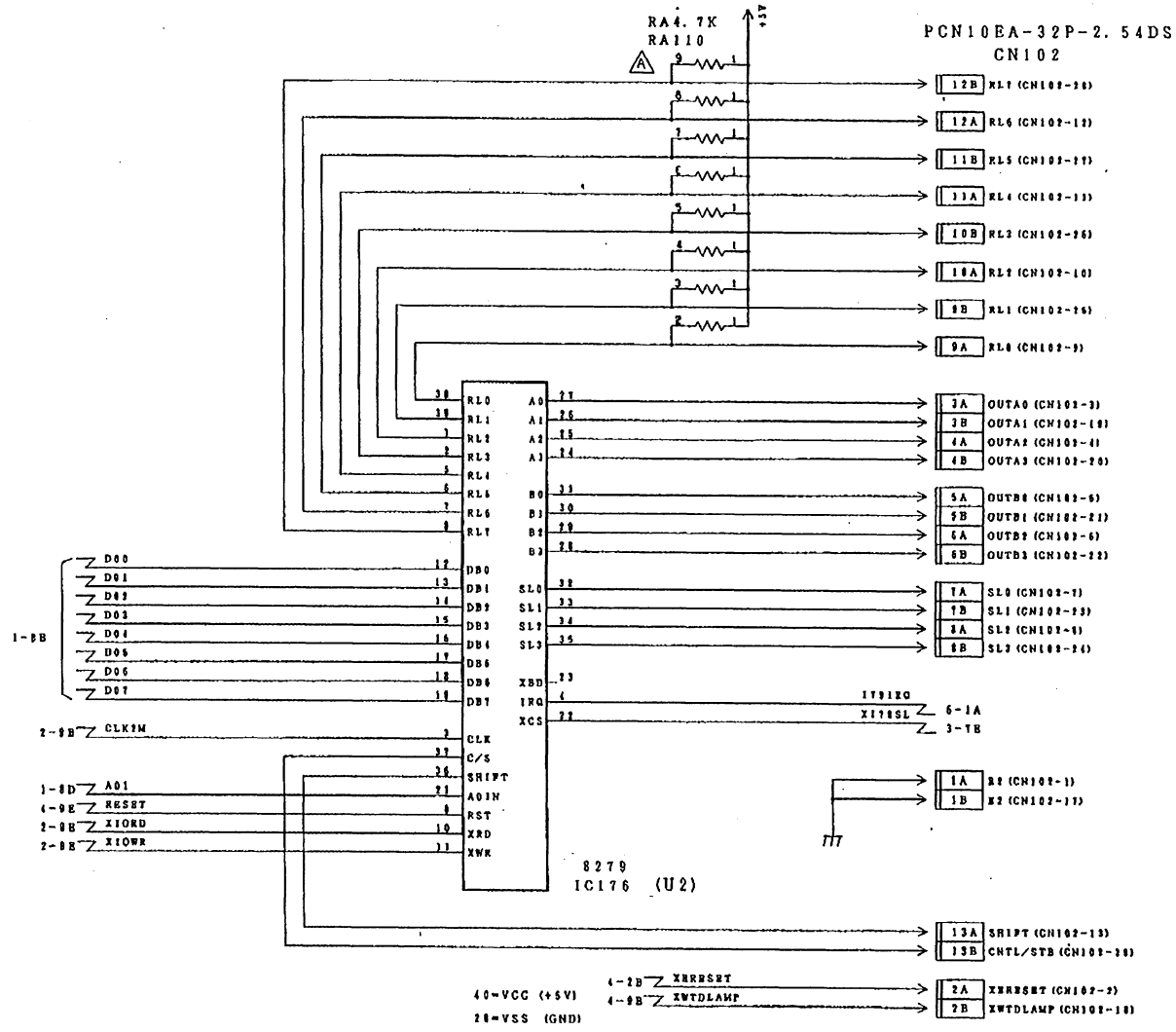
SK160～SK167 : DL-2-28A 14-VSS (GND)

CAD057A 3

承認 APPD	安田	図番 DWG NO	104978			
検図2 CHK2	荒金	型式 MODEL	UP-0260 10/16			
検図1 CHK1	早川	名称 NAME	CPU RAM 2/2			
設計 DESIGN	根本	日付 DATE	62-6-30			
製図 TRACE	宇野	日本光電				
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK			

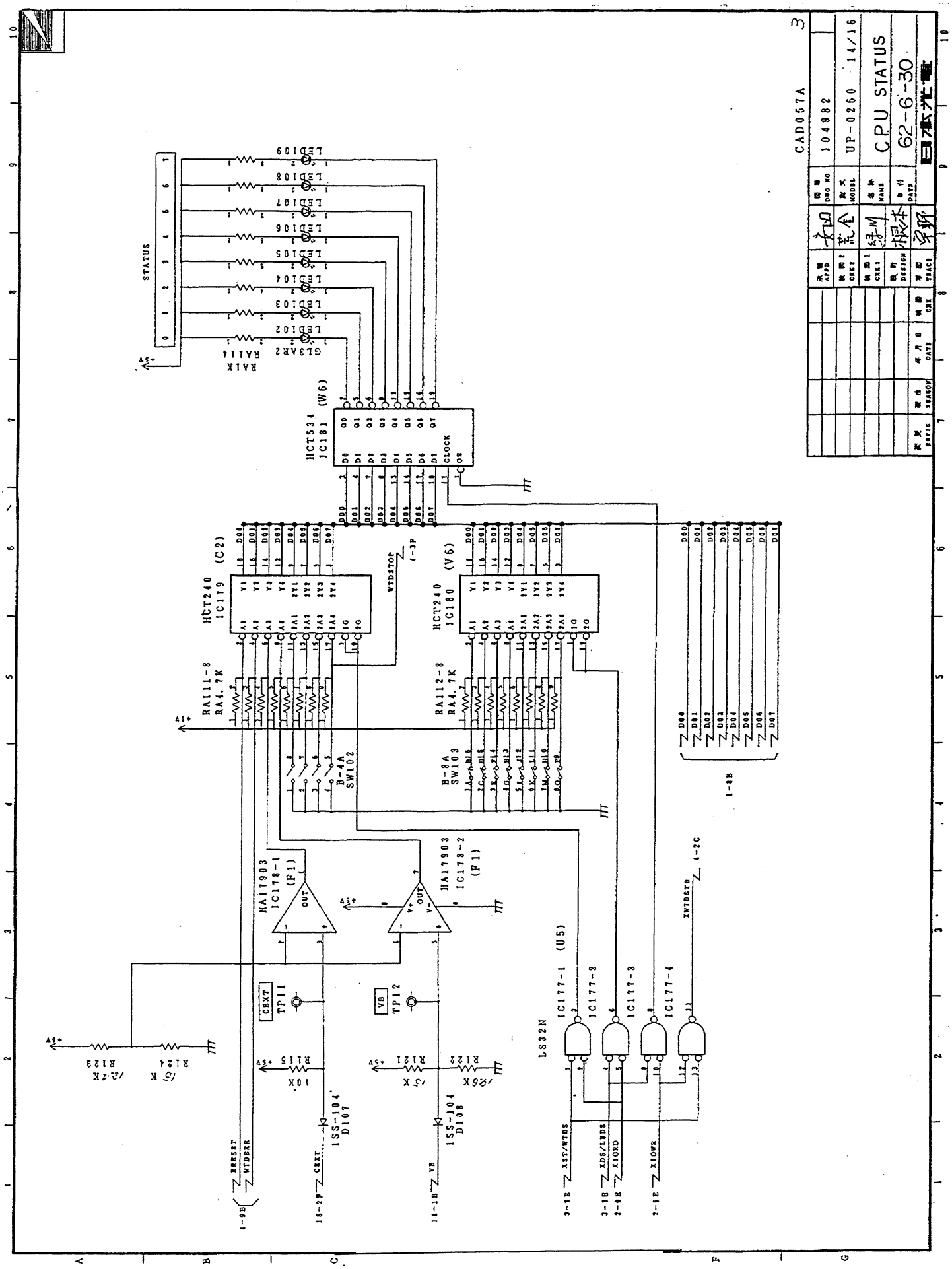

CAD057A
3
B
104979
UP-0260 11/16
CPU E2PROM
RTC/BTRY
62-6-30
MSM6242 IC169 (D2)
74HC08 IC124-4 (C5)
*X2816BP IC170 (S4)
IC110
HC132 IC168-1 (B2)
HC132 IC168-2 (B2)
HC132 IC168-3 (B2)
HC132 IC168-4 (B2)
30PF/VC KP38G X102
22PF/500 C107
5PF/VC
100Ω R103
1K R105
4.99K R106
4.99K R107
6.8MF C106
ISS-106 D102
ISS-104 D101
H2-3C3 D103
C1213 Q101
BAT101 3V BATT
STD. P TP10
XRESET
XIOWR
XIORD
XRTCSL
XEXPSL
XPWDWN

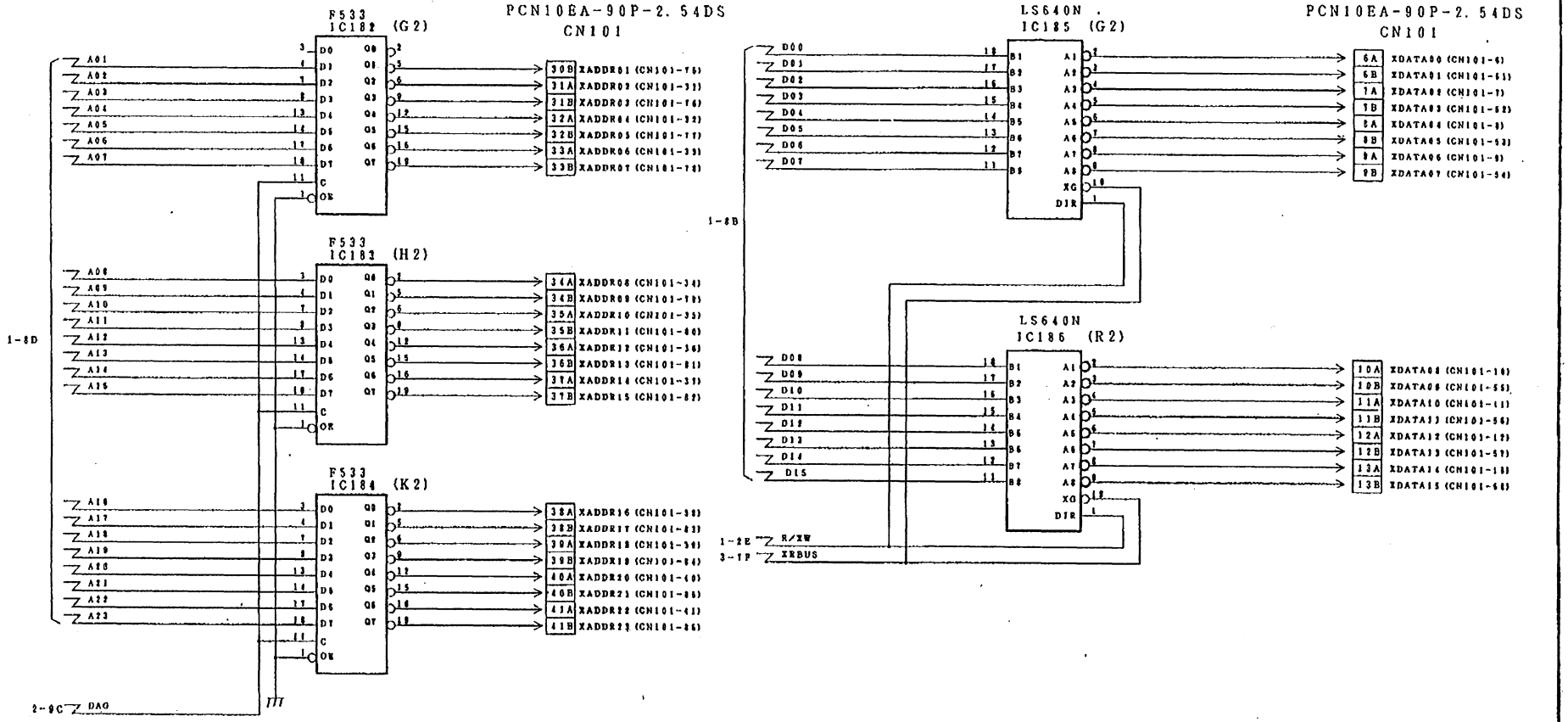

RDBD-25SE-LNA
CN103
TXD (CN103-2)
RTS (CN103-4)
RXD (CN103-3)
DSR (CN103-6)
DTR (CN103-20)
CTS (CN103-5)
FG (CN103-1)
SG (CN103-7)
75188 IC174-2 (V3)
75188 IC174-3
75189 IC175-1 (V2)
75189 IC175-3
75188 IC174-4
75189 IC175-2
75189 IC175-4 (V2)
75188 IC174-1 (V3)
* IC174 +12 14PIN
-12 1PIN
E2 7PIN
71051 IC172 (V4)
MPD71054.8253 IC173 (S2)
CAD057A
3
104980
UP-0260 12/16
CPU RS232C CNTL
62-6-30
日本光電



CAD057A 3

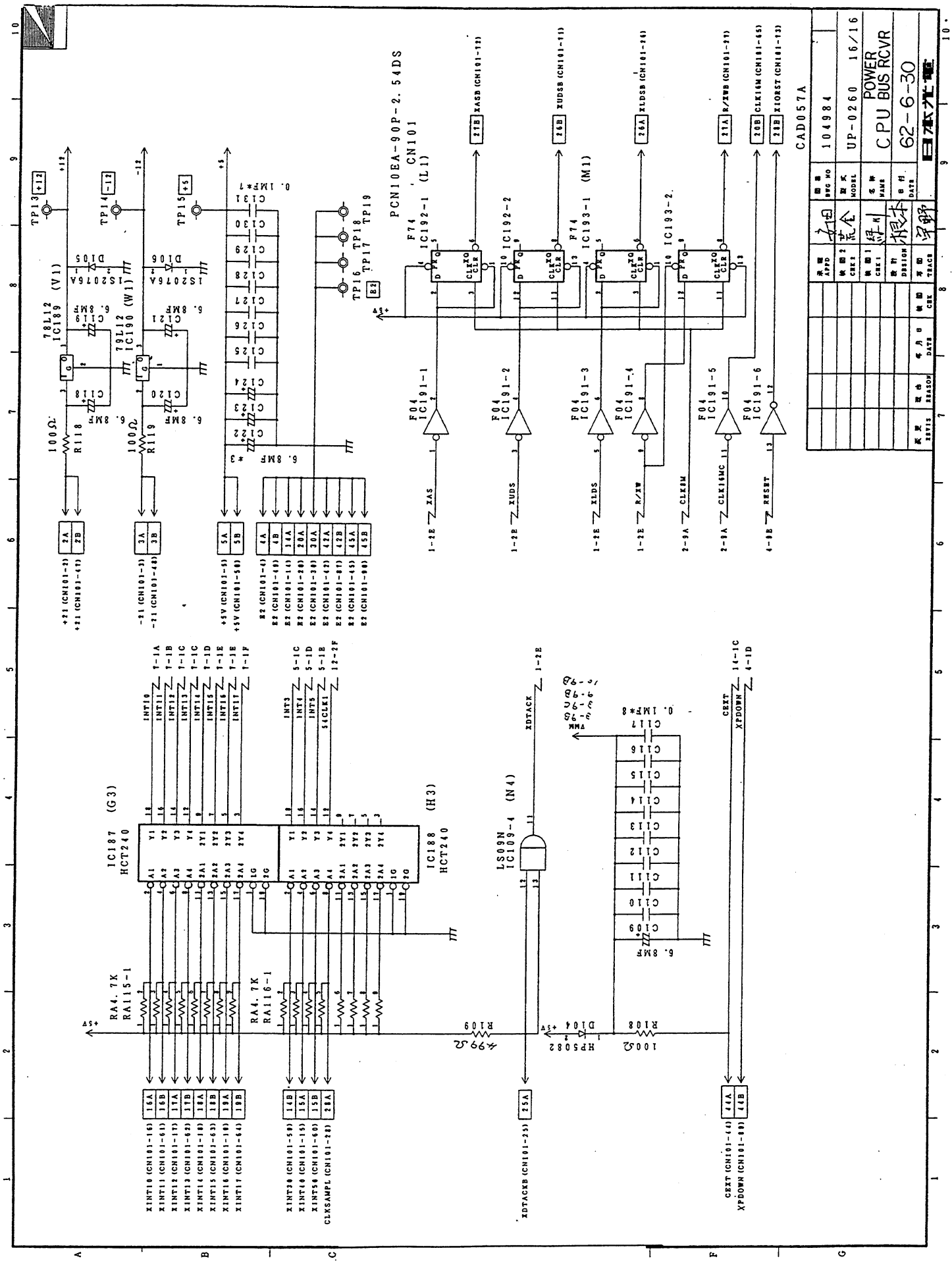
				承認 APPD	安田	図番 DWG NO	104981 A
				検図2 CHK2	荒金	型式 MODEL	UP-0260 13/16
				検図1 CHK1	深川	名称 NAME	CPU KEY CNTL
⚠×1	15	62-8-25	荒金	設計 DESIGN	根本	日付 DATE	62-6-30
改版 REVIS	改由 REASON	年月日 DATE	検図 CHK	作図 TRACE	宇野	日本電	

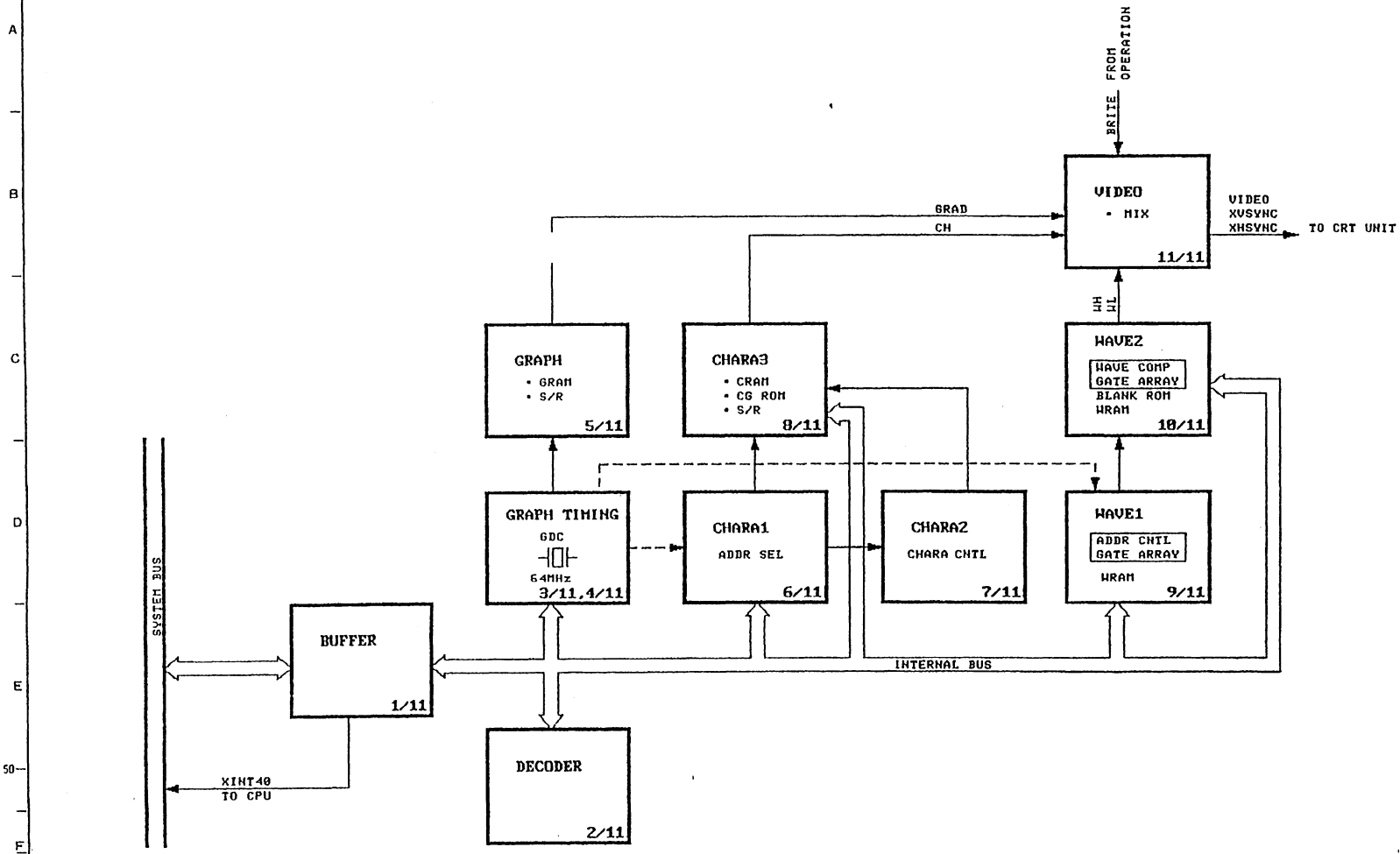

CAD057A
3
104982
UP-0260
14/16
CPU STATUS
62-6-30
日本光電
STATUS
LED109
LED108
LED107
LED106
LED105
LED104
LED103
LED102
RA1X
GL3AR2
RA114
HCT534
IC181 (W6)
HCT240
IC179 (C2)
HCT240
IC180 (V6)
WTDSTOP
RA111-8
RA4.7K
RA112-8
RA4.7K
B-4A
SW102
B-8A
SW103
HA17903
IC178-1 (F1)
HA17903
IC178-2 (F1)
CEXT
TP11
VB
TP12
R124
15K
R123
2.2K
R115
10K
R121
15K
R122
180K
ISS-104
D107
ISS-104
D108
LS32N
IC177-1 (U5)
IC177-2
IC177-3
IC177-4
XWTDSTB
XRESET
WTDERR
CEXT
VB
XST/WTDS
XDS/LEDS
XIORD
XIOWR



CAD057A 3

				承認 APPD	大田	図番 DWG NO	104983
				検図2 CHK 2	荒金	型式 MODEL	UP-0260 15/16
				検図1 CHK 1	緑川	名称 NAME	BUS CPU DRVR/RCVR
				設計 DESIGN	根本	日付 DATE	62-6-30
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	製図 TRACE	宇野	日本電	


PCN10EA-90P-2.54DS
CN101
CAD057A
104984
UP-0260 16/16
POWER
CPU BUS RCVR
62-6-30
日本ケンウッド
IC187 (G3)
HCT240
IC188 (H3)
HCT240
IC189 78L12 (V1)
IC190 79L12 (W1)
IC191-1 (L1)
IC192-1 (L1)
IC192-2
IC193-1 (M1)
IC193-2
IC109-4 (N4)
LS09N
RA4.7K RA115-1
RA4.7K RA116-1
RP5082
R108 100Ω
R109 499Ω
R118 100Ω
R119 100Ω
TP13 +12
TP14 -12
TP15 +5
TP16 TP17 TP18 TP19
XINT10 (CN101-16)
XINT11 (CN101-61)
XINT12 (CN101-17)
XINT13 (CN101-62)
XINT14 (CN101-18)
XINT15 (CN101-63)
XINT16 (CN101-19)
XINT17 (CN101-64)
XINT30 (CN101-59)
XINT40 (CN101-15)
XINT50 (CN101-60)
CLKSAMPL (CN101-20)
XDTACKB (CN101-25)
CEXT (CN101-44)
XPDOWN (CN101-89)
+21 (CN101-2)
+21 (CN101-47)
-21 (CN101-3)
-21 (CN101-48)
+5V (CN101-5)
+5V (CN101-50)
E2 (CN101-4)
E2 (CN101-49)
E2 (CN101-11)
E2 (CN101-56)
E2 (CN101-28)
E2 (CN101-73)
E2 (CN101-30)
E2 (CN101-75)
E2 (CN101-87)
E2 (CN101-45)
E2 (CN101-90)
XAS (CN101-72)
XUDSB (CN101-71)
XLDSB (CN101-24)
R/XWB (CN101-23)
CLKIOW (CN101-45)
XIORST (CN101-73)
XDTACK
XAS
XUDS
XLDS
R/XWB
CLKIOW
RESET
CLKSM
0.1MF*8
0.1MF*3
6.8MF

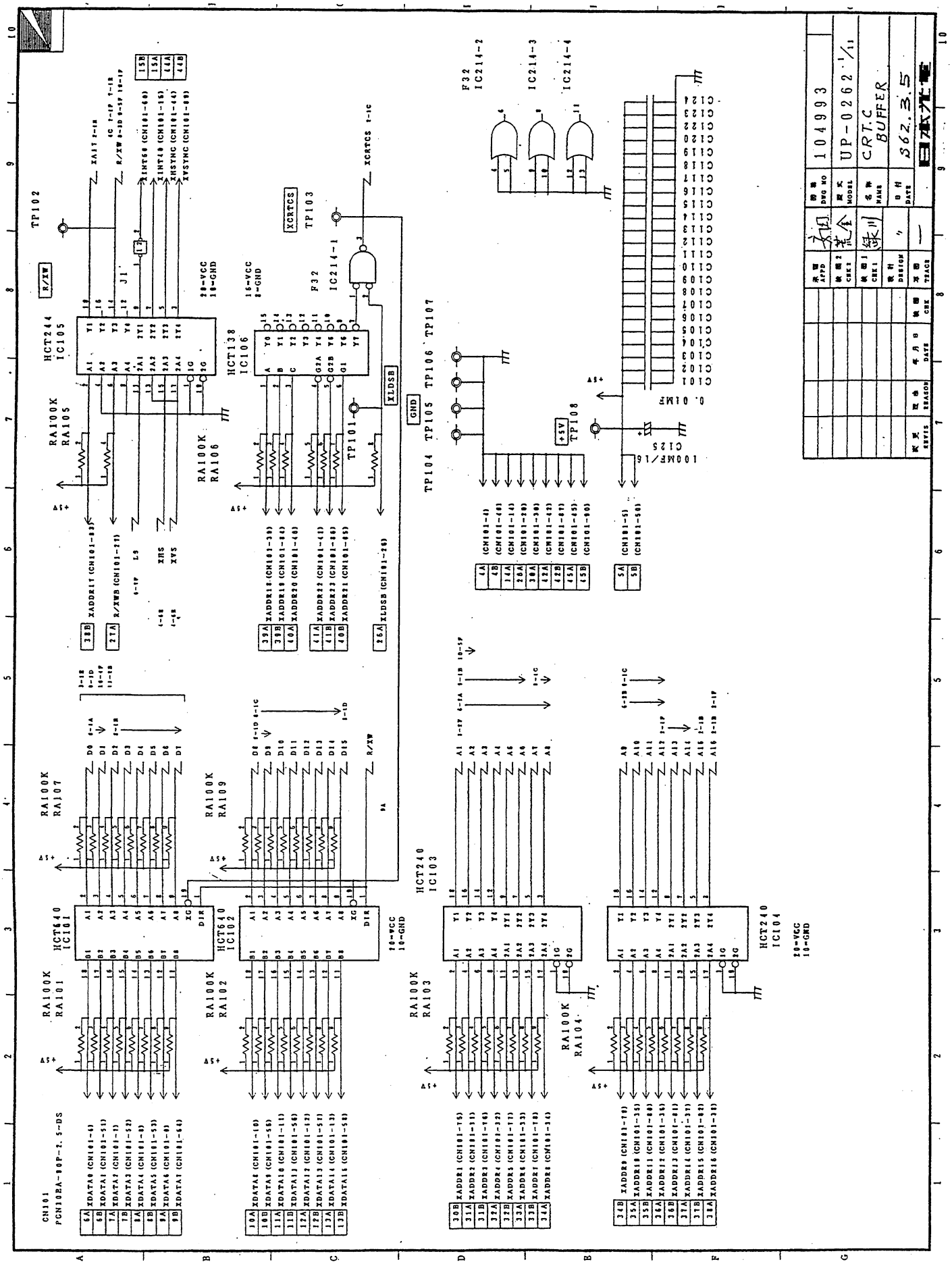


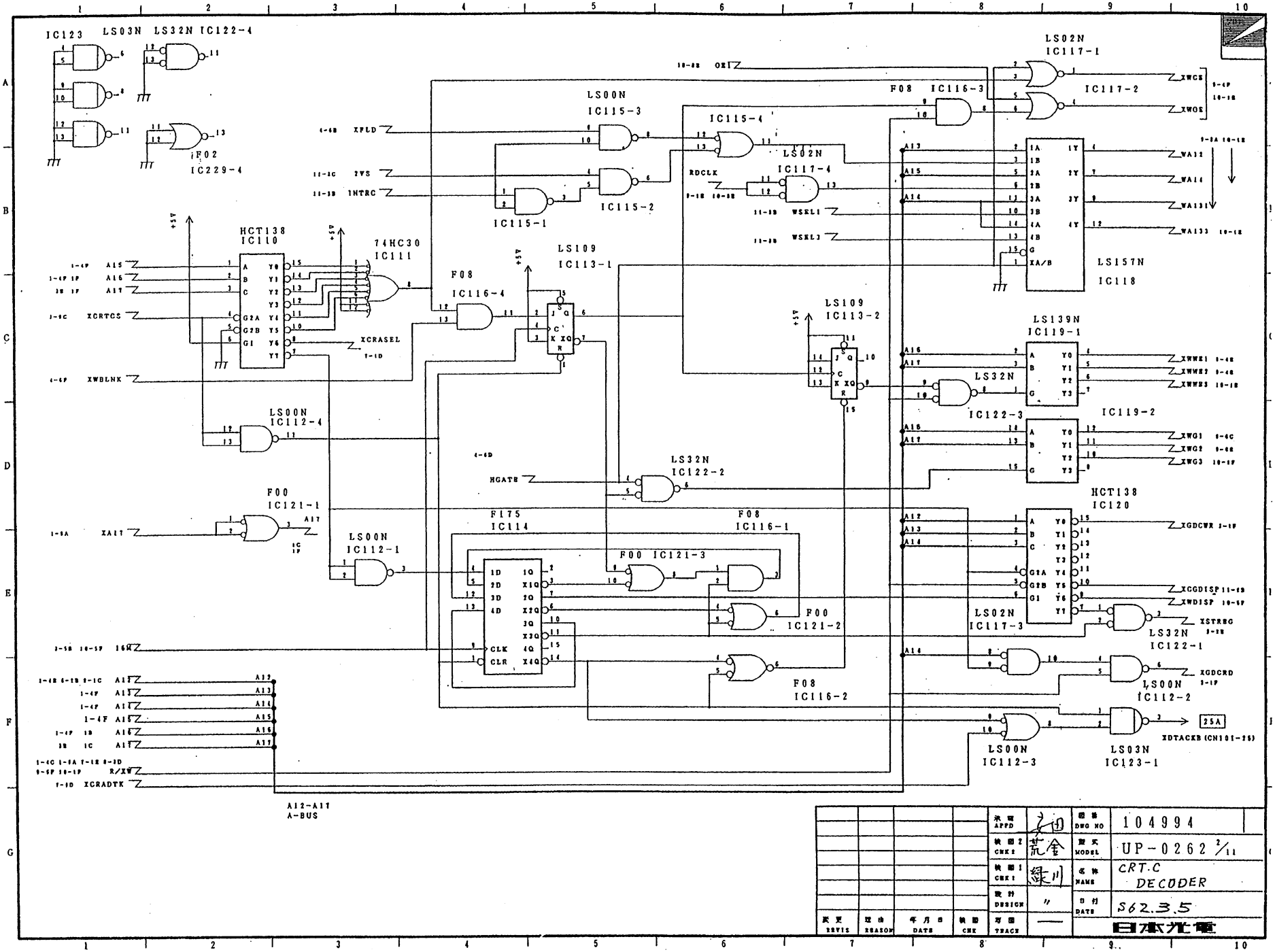
添付図	—	—	所蔵図	—
	—	—		—

変更 REVIS	理由 REASON	年月日 DATE	検図 CHK
△×		— —	
△×		— —	
△×		— —	
△×		— —	
△×		— —	
△×		— —	
△×		— —	

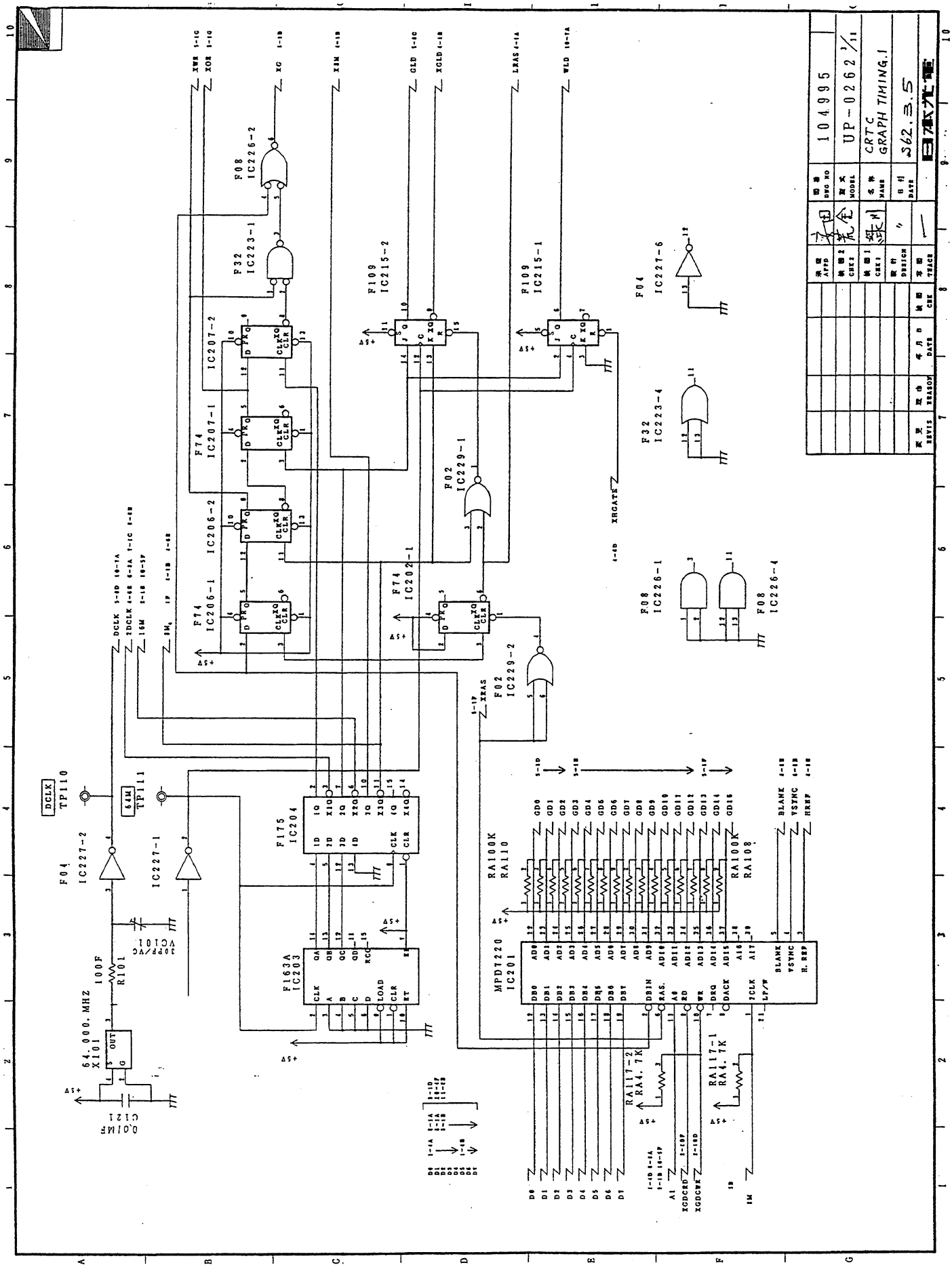
承認 APPD	安田	図番 DWG NO	105004
検図2 CHK 2	荒金	型式 MODEL	UP-0262
検図1 CHK 1	根本	名称 NAME	CRTC BLOCK DIAGRAM
設計 DESIGN	渡辺	日付 DATE	62-7-16
写図 TRACE	斉藤	日本光電	

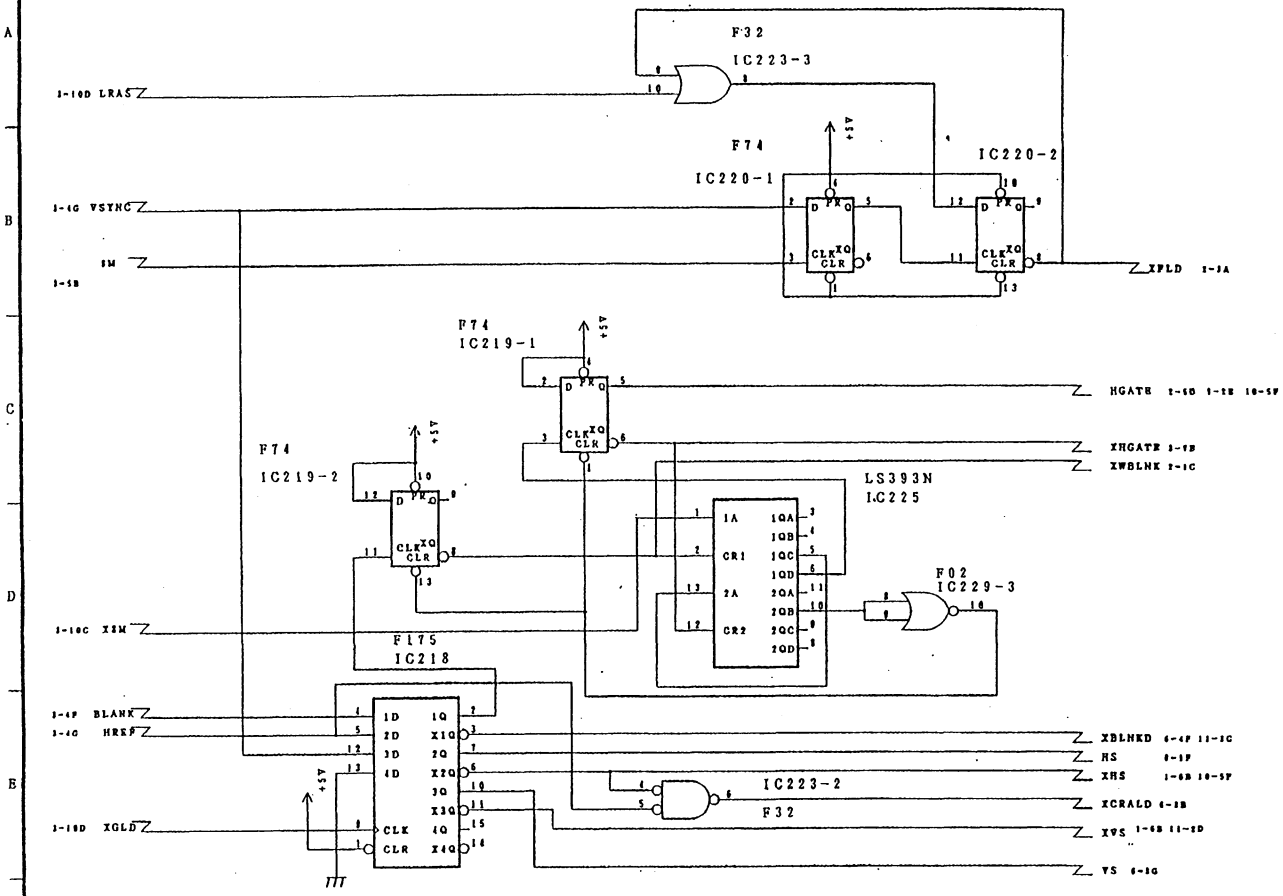
3


CN101
PCN10BA-80P-2.5-DS
HCT640 IC101
HCT640 IC102
HCT240 IC103
HCT240 IC104
HCT244 IC105
HCT138 IC106
RA100K RA101
RA100K RA102
RA100K RA103
RA100K RA104
RA100K RA105
RA100K RA106
RA100K RA107
RA100K RA109
TP102
TP103
TP104 TP105 TP106 TP107
TP101
TP108
R/XW
XCRTCS
XLDSB
GND
+5V
F32 IC214-2
IC214-3
IC214-4
IC214-1
100MF/16 C125
0.01MF
XDATA0 (CN101-4)
XDATA1 (CN101-51)
XDATA2 (CN101-1)
XDATA3 (CN101-52)
XDATA4 (CN101-3)
XDATA5 (CN101-53)
XDATA6 (CN101-9)
XDATA7 (CN101-54)
XADDR1 (CN101-75)
XADDR2 (CN101-31)
XADDR3 (CN101-76)
XADDR4 (CN101-32)
XADDR5 (CN101-77)
XADDR6 (CN101-33)
XADDR7 (CN101-78)
XADDR8 (CN101-34)
XADDR9 (CN101-79)
XADDR10 (CN101-35)
XADDR11 (CN101-80)
XADDR12 (CN101-36)
XADDR13 (CN101-81)
XADDR14 (CN101-37)
XADDR15 (CN101-82)
XADDR16 (CN101-38)
XADDR17 (CN101-83)
XADDR18 (CN101-39)
XADDR19 (CN101-84)
XADDR20 (CN101-40)
XADDR21 (CN101-85)
XADDR22 (CN101-41)
XADDR23 (CN101-86)
XADDR24 (CN101-42)
R/XWB (CN101-27)
XINTSB (CN101-60)
XINTSB (CN101-15)
XHSYNC (CN101-44)
XVSYNC (CN101-89)
XHS
XVS
20=VCC
10=GND
16=VCC
8=GND
104993
UP-0262-1/1
CRT.C
BUFFER
S62.3.5
日本ビクター

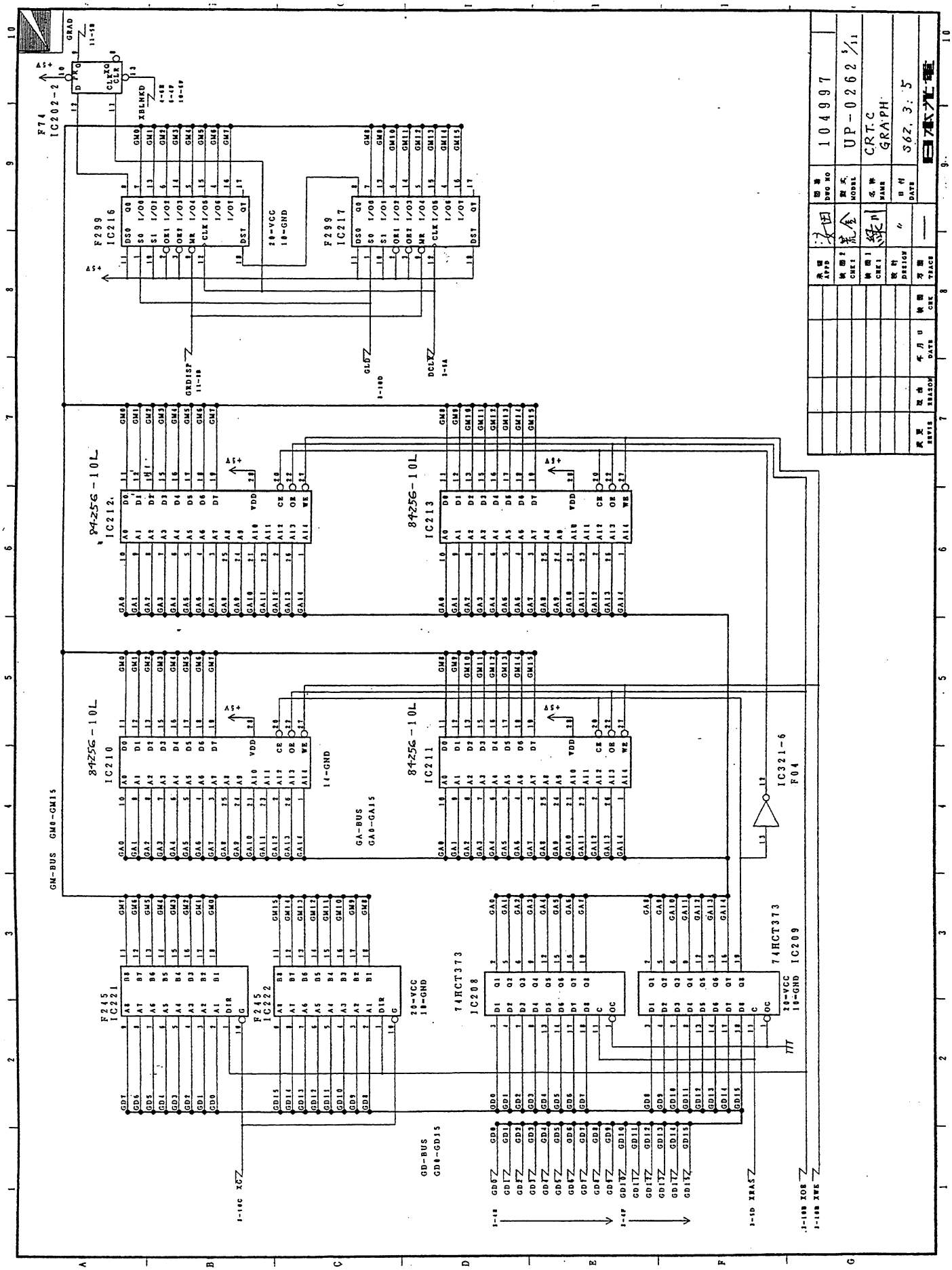


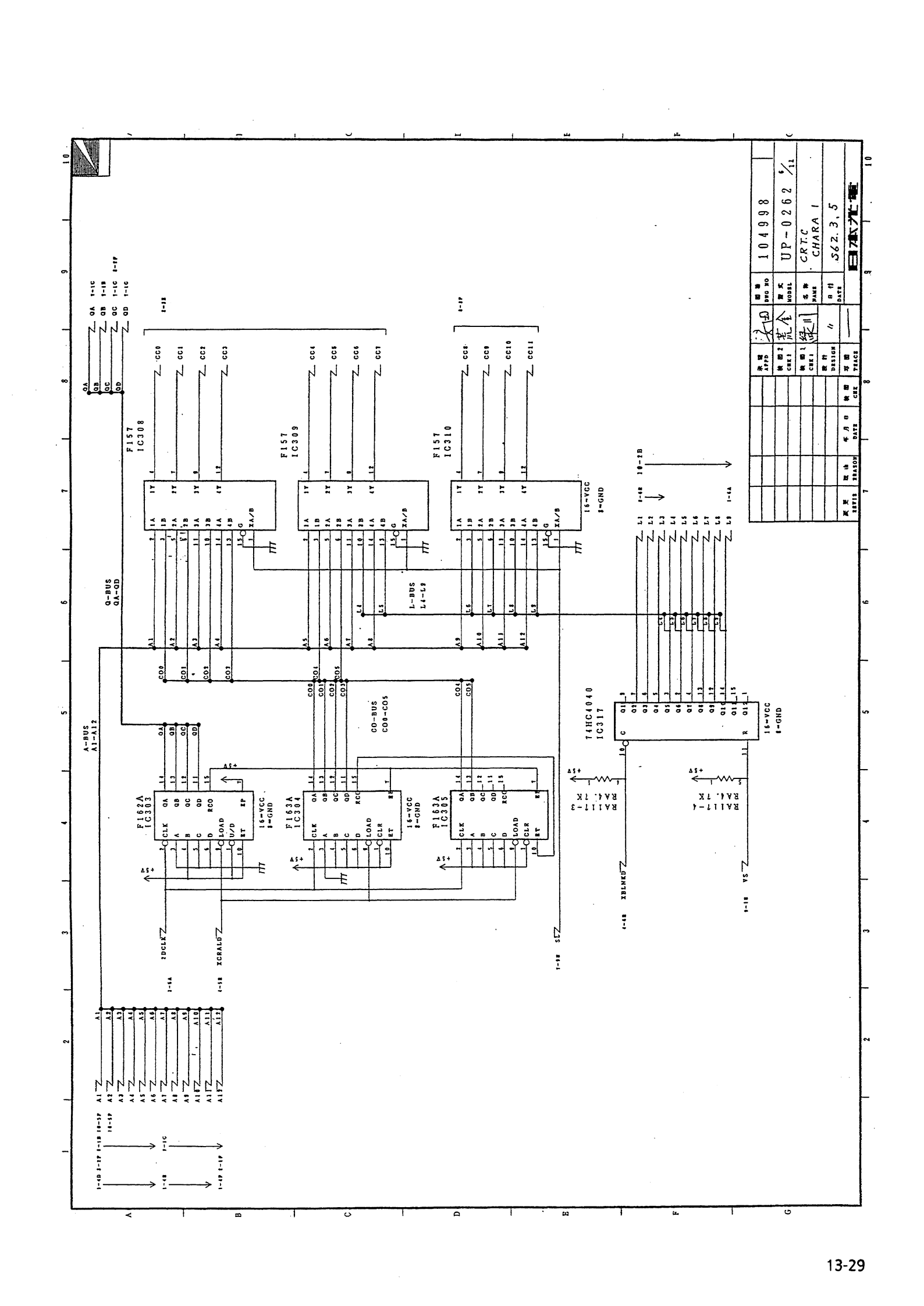
					承認 APPD	石田	図番 DWG NO	104994
					検図2 CHK 2	荒金	型式 MODEL	UP-0262 2/11
					検図1 CHK 1	緑川	名称 NAME	CRT.C DECODER
					設計 DESIGN	〃	日付 DATE	S62.3.5
改定 REVIS	改由 REASON	年月日 DATE	検図 CHK		写図 TRACE	—	日本光電	

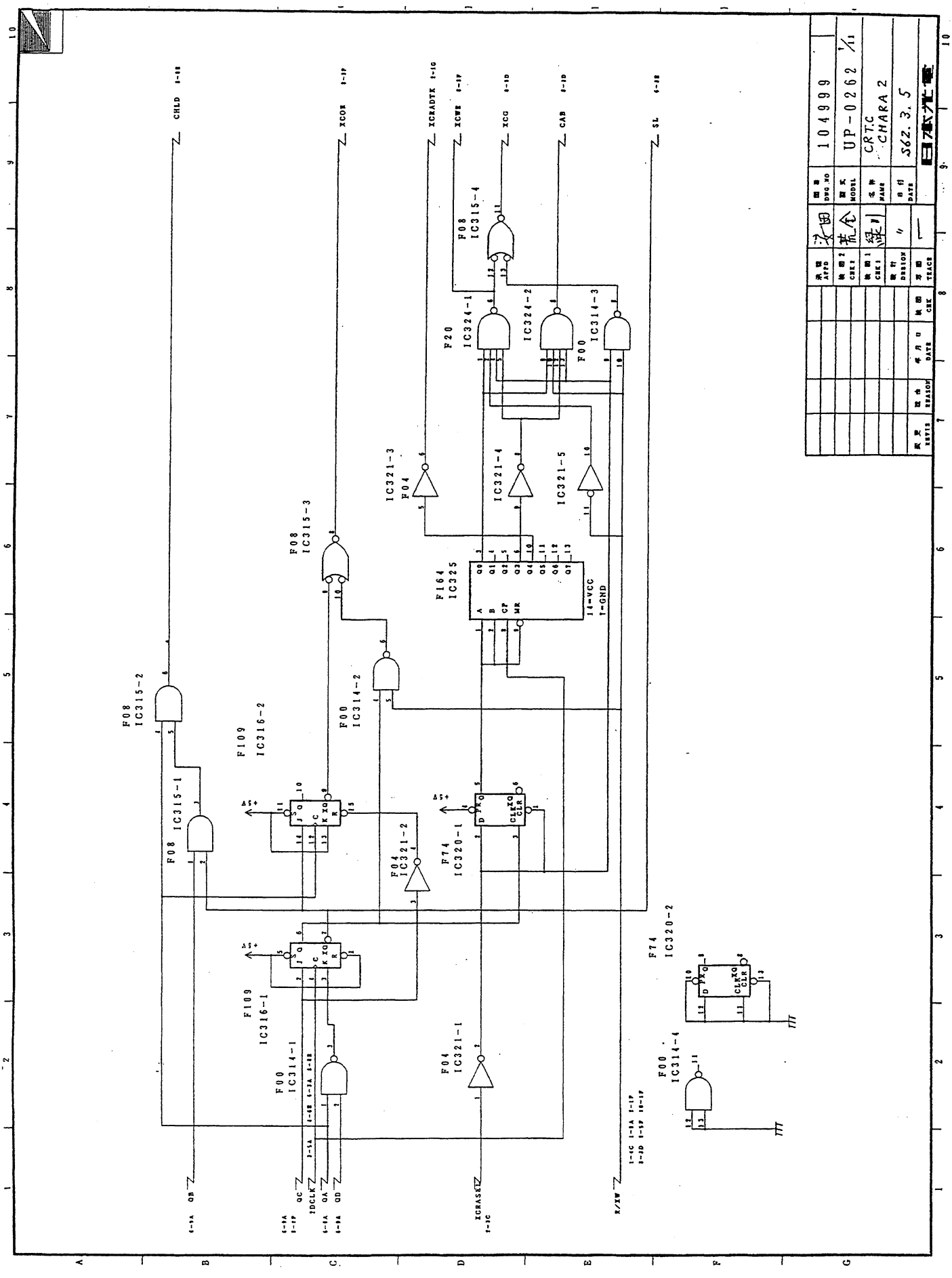

DCLK
TP110
64M
TP111
F04
IC227-2
IC227-1
64.000.MHZ
X101
100F
R101
30PF/VC
VC101
0.01MF
C121
F163A
IC203
F175
IC204
MPD7220
IC201
RA100K
RA110
RA100K
RA108
RA117-2
RA4.7K
RA117-1
RA4.7K
F74
IC206-1
IC206-2
IC207-1
IC207-2
F74
IC202-1
F02
IC229-1
F02
IC229-2
F08
IC226-2
F32
IC223-1
F109
IC215-2
F109
IC215-1
F04
IC227-6
F32
IC223-4
F08
IC226-1
F08
IC226-4
XRGATE
XRAS
BLANK
VSYNC
HREF
104995
UP-0262 1/1
CRTC
GRAPH TIMING.1
'92.3.5
日本ビクター

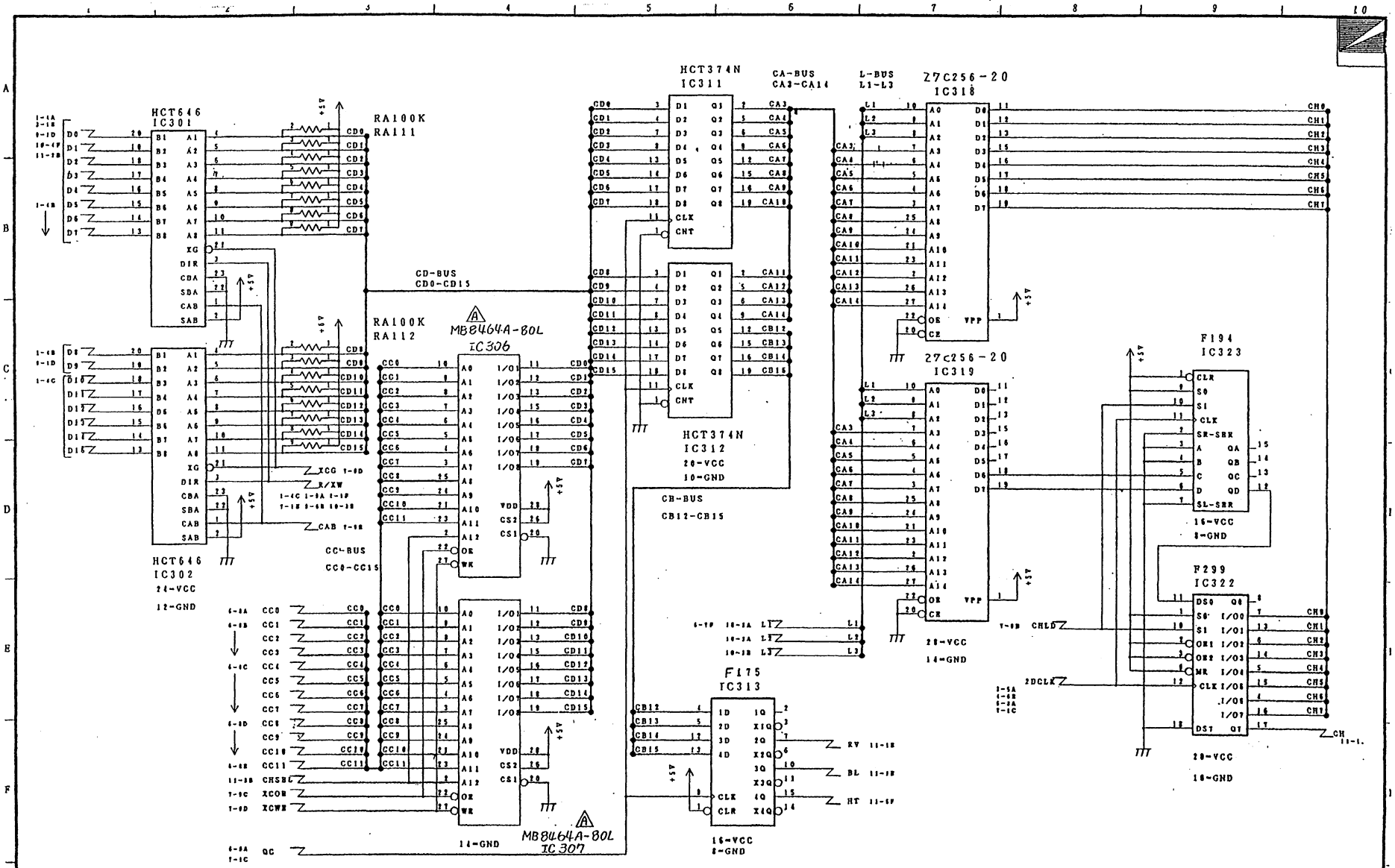


					承認 APPD	安田	図番 DWG NO	104996
					検図2 CHK 2	荒金	型式 MODEL	UP-0262 4/11
					検図1 CHK 1	緑川	名称 NAME	CRTC GRAPH TIMING 2
					設計 DESIGN	〃	日付 DATE	S62.3.5
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK		写図 TRACE	—	日本電	

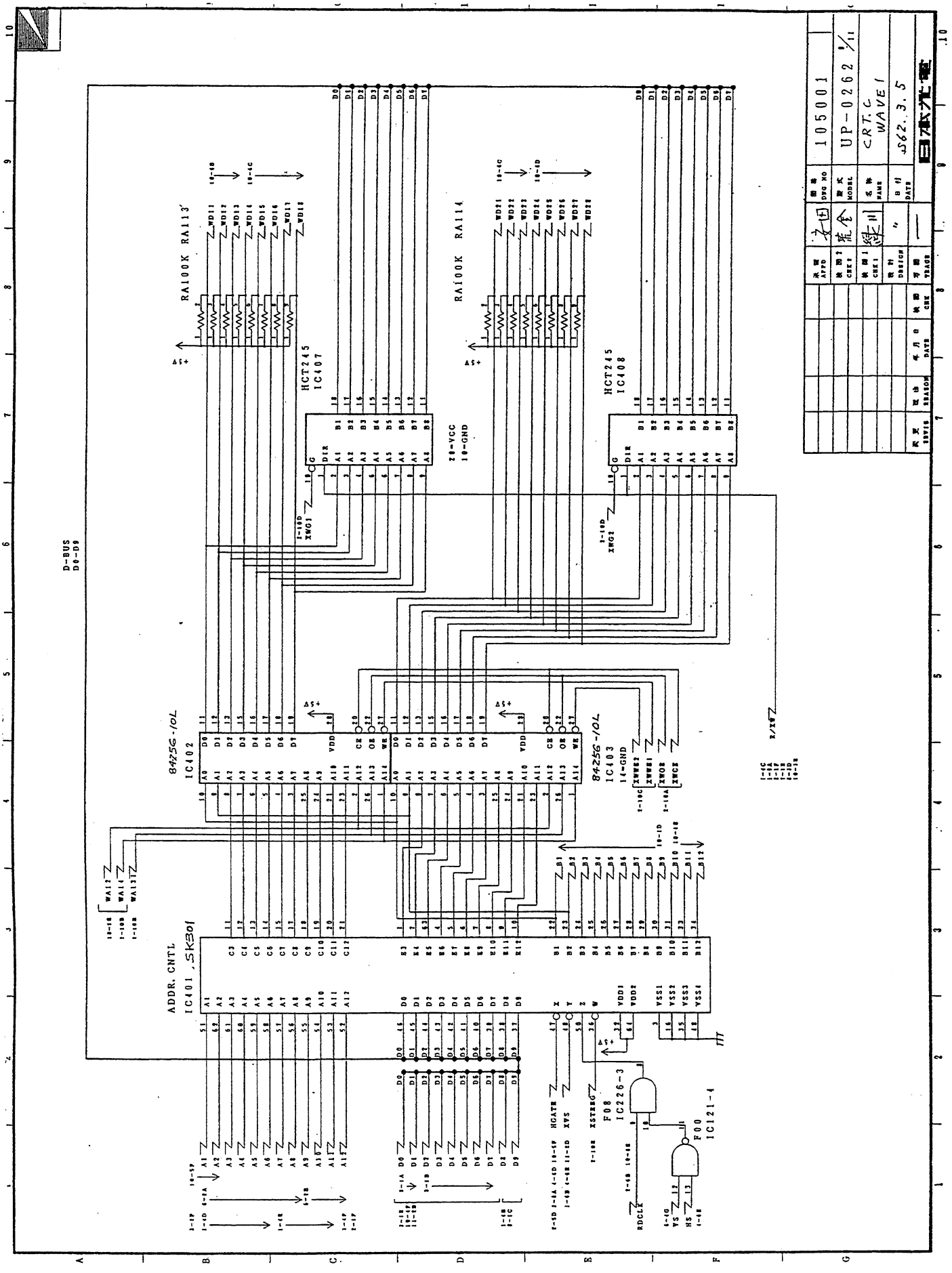

F74
IC202-2
F299
IC216
F299
IC217
84256-10L
IC212
84256-10L
IC213
84256-10L
IC210
84256-10L
IC211
F245
IC221
F245
IC222
74HCT373
IC208
74HCT373
IC209
IC321-6
F04
GA-BUS
GA0-GA15
GD-BUS
GD0-GD15
GM-BUS
GM0-GM15
104997
UP-0262
CRT.C
GRAPH
S62. 3. 5

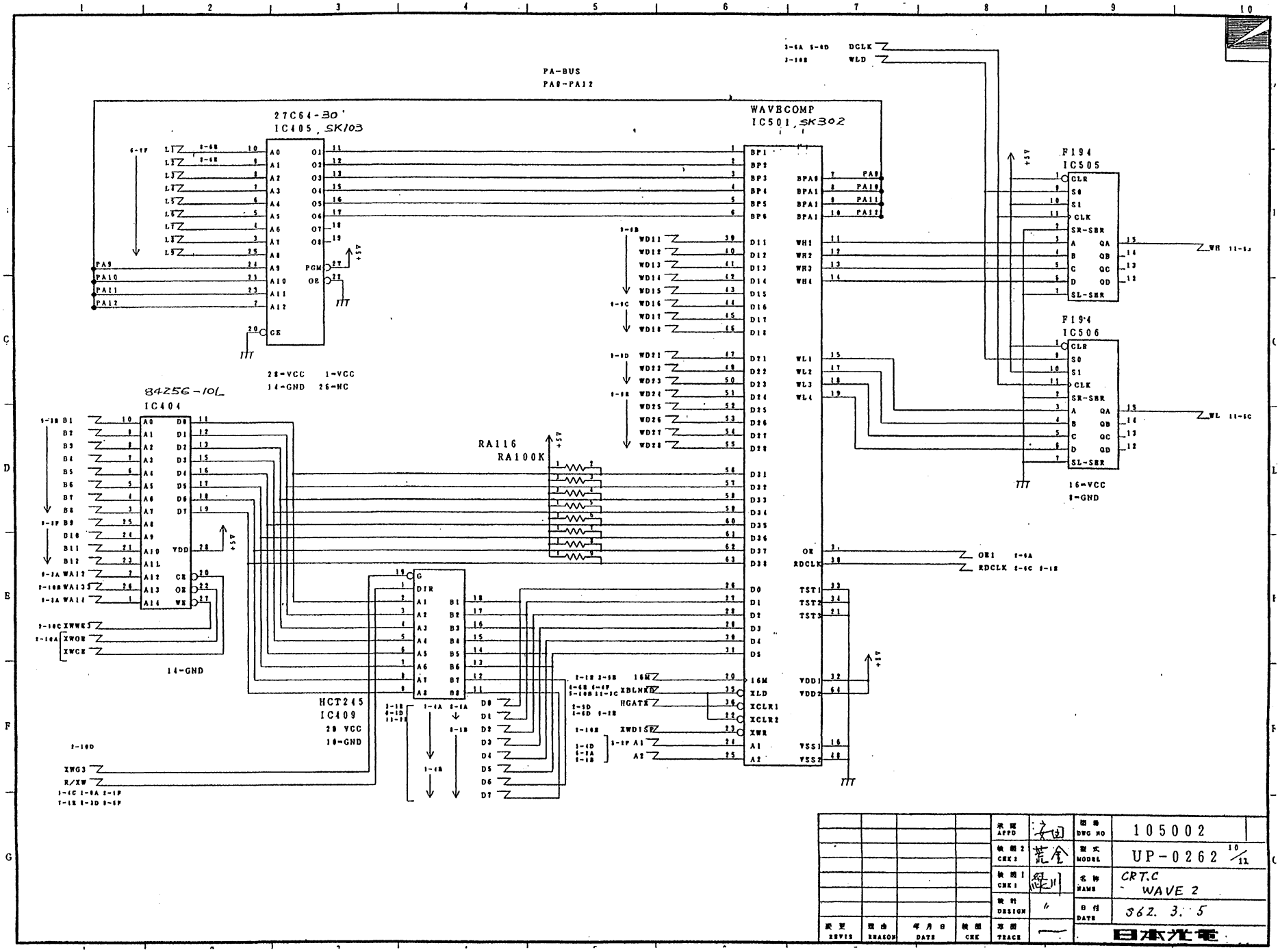

F157 IC308
F157 IC309
F157 IC310
F162A IC303
F163A IC304
F163A IC305
74HC4040 IC317
A-BUS A1-A12
Q-BUS QA-QD
L-BUS L1-L8
CO-BUS CO0-CO5
104998
UP-0262 5/11
CRT.C CHARA 1
S62.3.5


CHLD
XCOR
XCRADTK
XCWR
XCG
CAB
SL
F08 IC315-2
F08 IC315-1
F109 IC316-2
F00 IC314-2
F08 IC315-3
F164 IC325
F04 IC321-3
F08 IC315-4
F20 IC324-1
IC324-2
F00 IC314-3
IC321-4
IC321-5
14-VCC
7-GND
F109 IC316-1
F00 IC314-1
F04 IC321-2
F74 IC320-1
F04 IC321-1
F74 IC320-2
F00 IC314-4
QB
QC
IDCLK
QA
QD
XCRASEL
R/W
104999
UP-0262 1/1
CRTC CHARA 2
S62.3.5



					承認 APPD	安田	図番 DWG NO	105000 A
					検図2 CHK 2	荒金	型式 MODEL	UP-0262/11
					検図1 CHK 1	緑川	名称 NAME	CRT.C - CHARA 3
⚠×2	24	62-9-4	荒金		設計 DESIGN	〃	日付 DATE	S62.3.5
改更 REVIS	改由 REASON	年月日 DATE	検図 CHK		作図 TRACE	—	日本光電	


D-BUS
D0-D9
RA100K RA113
RA100K RA114
HCT245
IC407
HCT245
IC408
84256-10L
IC402
84256-10L
IC403
ADDR. CNTL
IC401 ,SK30
F08
IC226-3
F00
IC121-4
105001
UP-0262 1/11
<RT.C
WAVE1
S62.3.5



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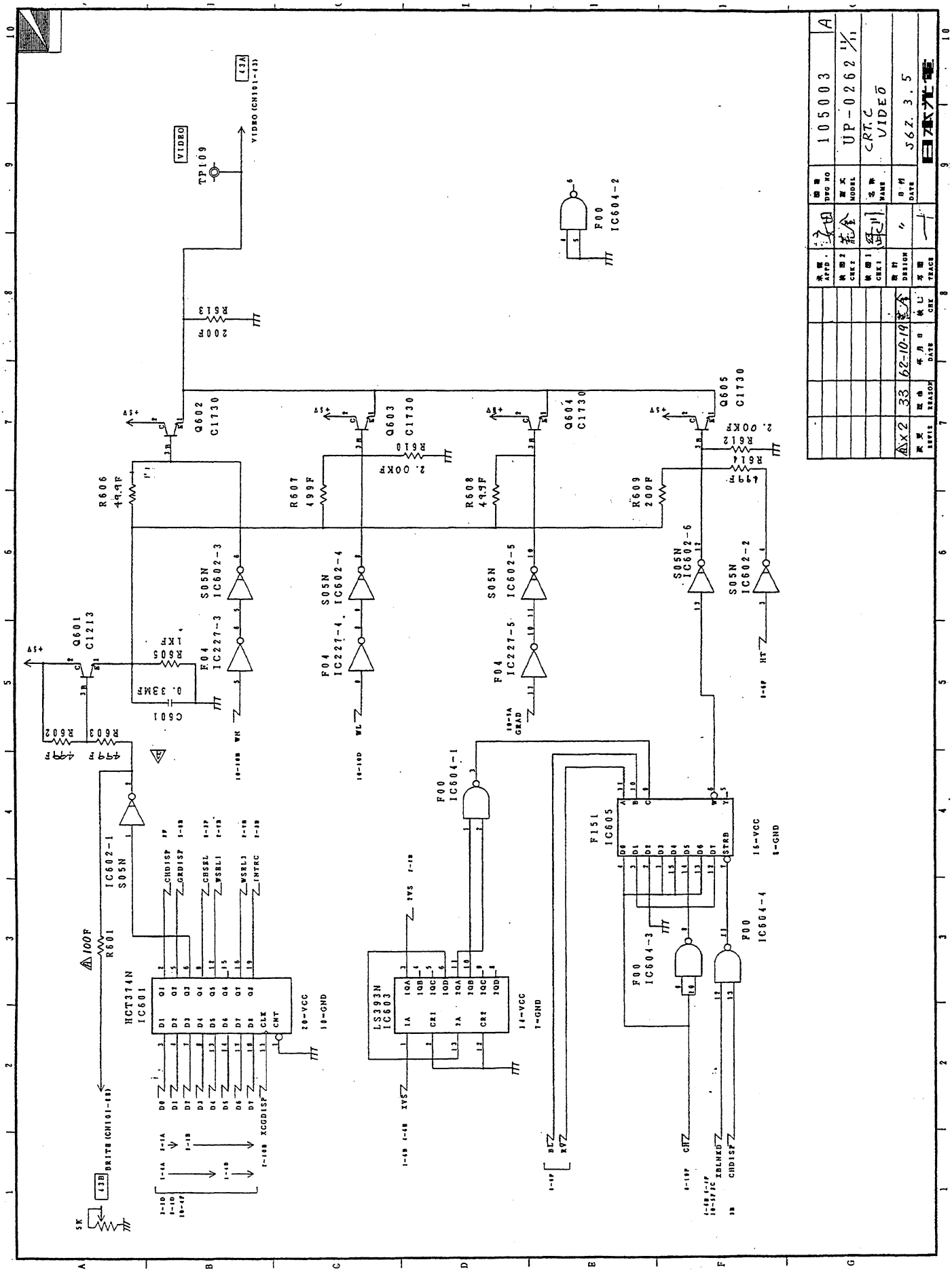
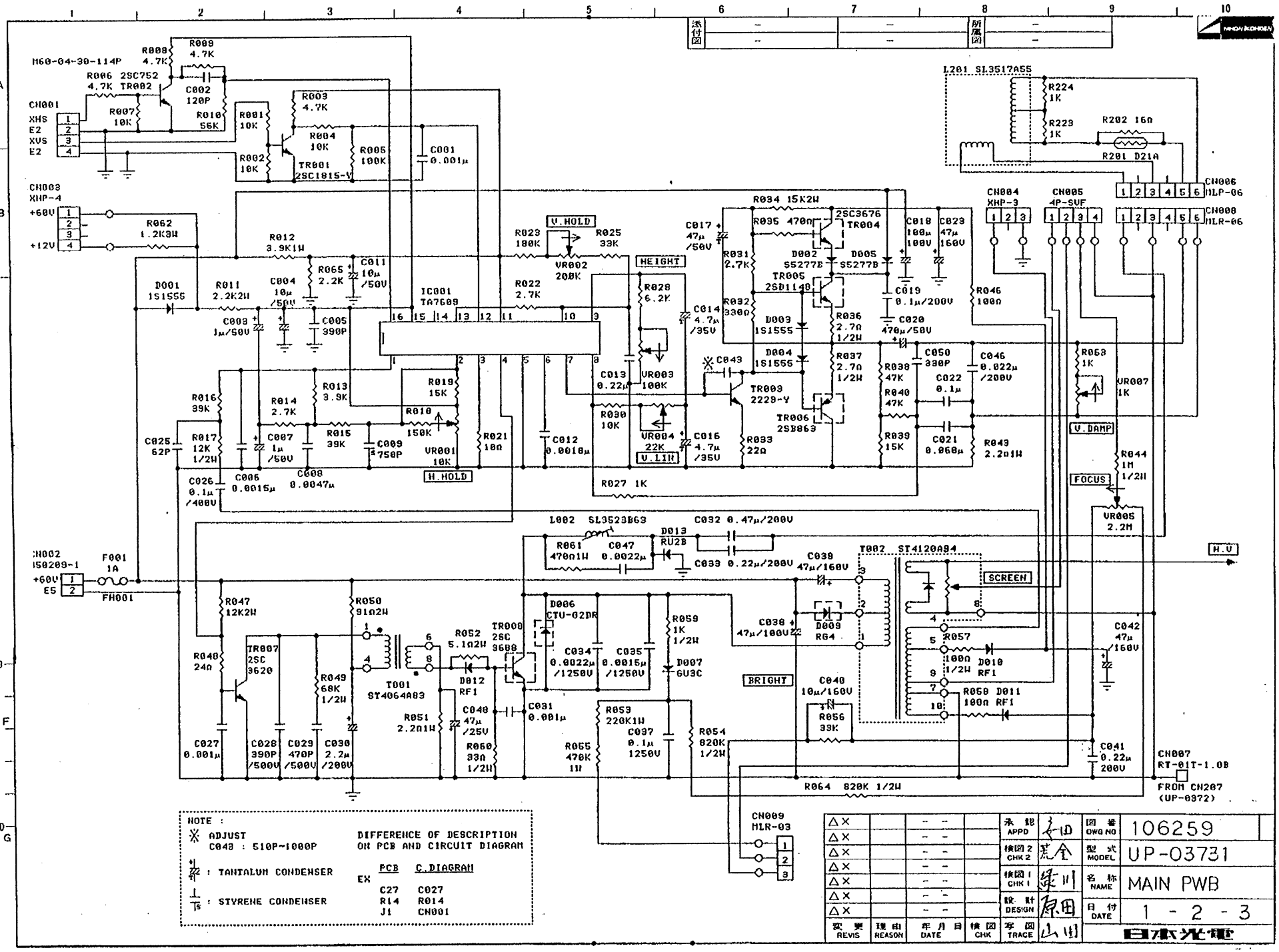
					検図2 CHK 2	荒金	型式 MODEL	UP-0262 10/11
					検図1 CHK 1	梁川	名称 NAME	CRT.C WAVE 2
					設計 DESIGN	〃	日付 DATE	86. 3. 5
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK		写図 TRACE	—	日本光電	


VIDEO
TP109
R613
200F
Q602 C1730
Q603 C1730
Q604 C1730
Q605 C1730
R606 49.9F
R607 499F
R608 49.9F
R609 200F
R610 2.00KF
R612 2.00KF
R614 499F
Q601 C1213
R605 1KF
0.33MF
C601
R602 499F
R603 499F
IC602-1 S05N
IC602-2 S05N
IC602-3 S05N
IC602-4 S05N
IC602-5 S05N
IC602-6 S05N
IC227-3 F04
IC227-4 F04
IC227-5 F04
IC604-1 F00
IC604-2 F00
IC604-3 F00
IC604-4 F00
IC605 F151
IC601 HCT374N
IC603 LS393N
100F
R601
5K
VIDEO (CN101-13)
BRITE (CN101-18)
WR
WG
HT
GRAD
CHDISP
GRDISP
CBSEL
WSEL1
WSEL2
INTRC
XCGDISP
XVS
XBLNKG
CHDISP
STRB
VCC
GND

| | | |



NOTE :

※ ADJUST
C048 : 510P~1000P

: TANTALUM CONDENSER

: STYRENE CONDENSER

DIFFERENCE OF DESCRIPTION ON PCB AND CIRCUIT DIAGRAM

	PCB	C.DIAGRAM
EX	C27	C027
	R14	R014
	J1	CN001

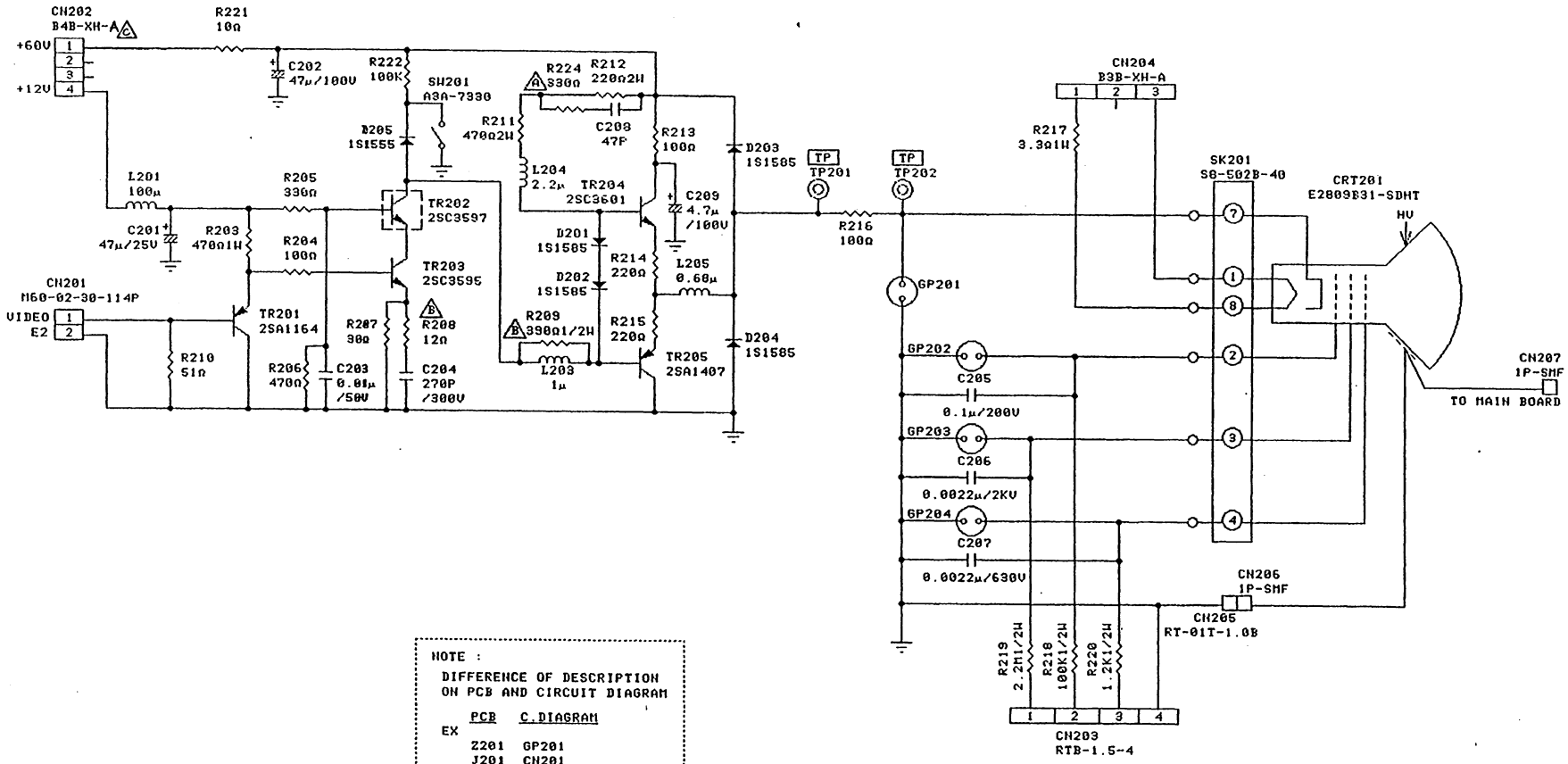
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK
△×		-- --	
△×		-- --	
△×		-- --	
△×		-- --	
△×		-- --	
△×		-- --	

承認 APPD	長山
検図2 CHK 2	荒金
検図1 CHK 1	梁川
設計 DESIGN	原田
写図 TRACE	山川

図番 DWG NO	106259
型式 MODEL	UP-03731
名称 NAME	MAIN PWB
日付 DATE	1 - 2 - 3

日本光電

添付図	—	—	所属図	—
	—	—		—

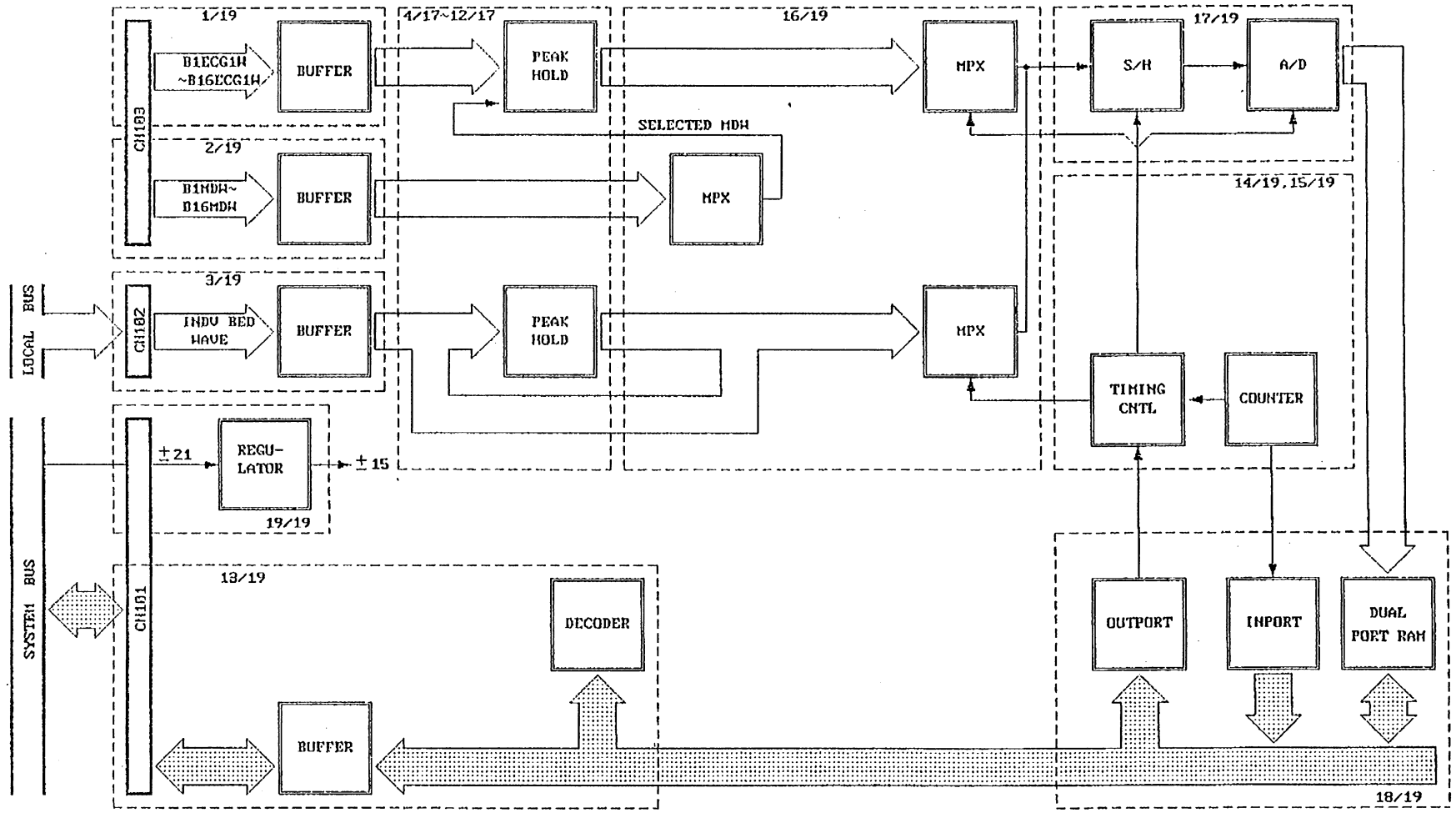


NOTE :
DIFFERENCE OF DESCRIPTION ON PCB AND CIRCUIT DIAGRAM

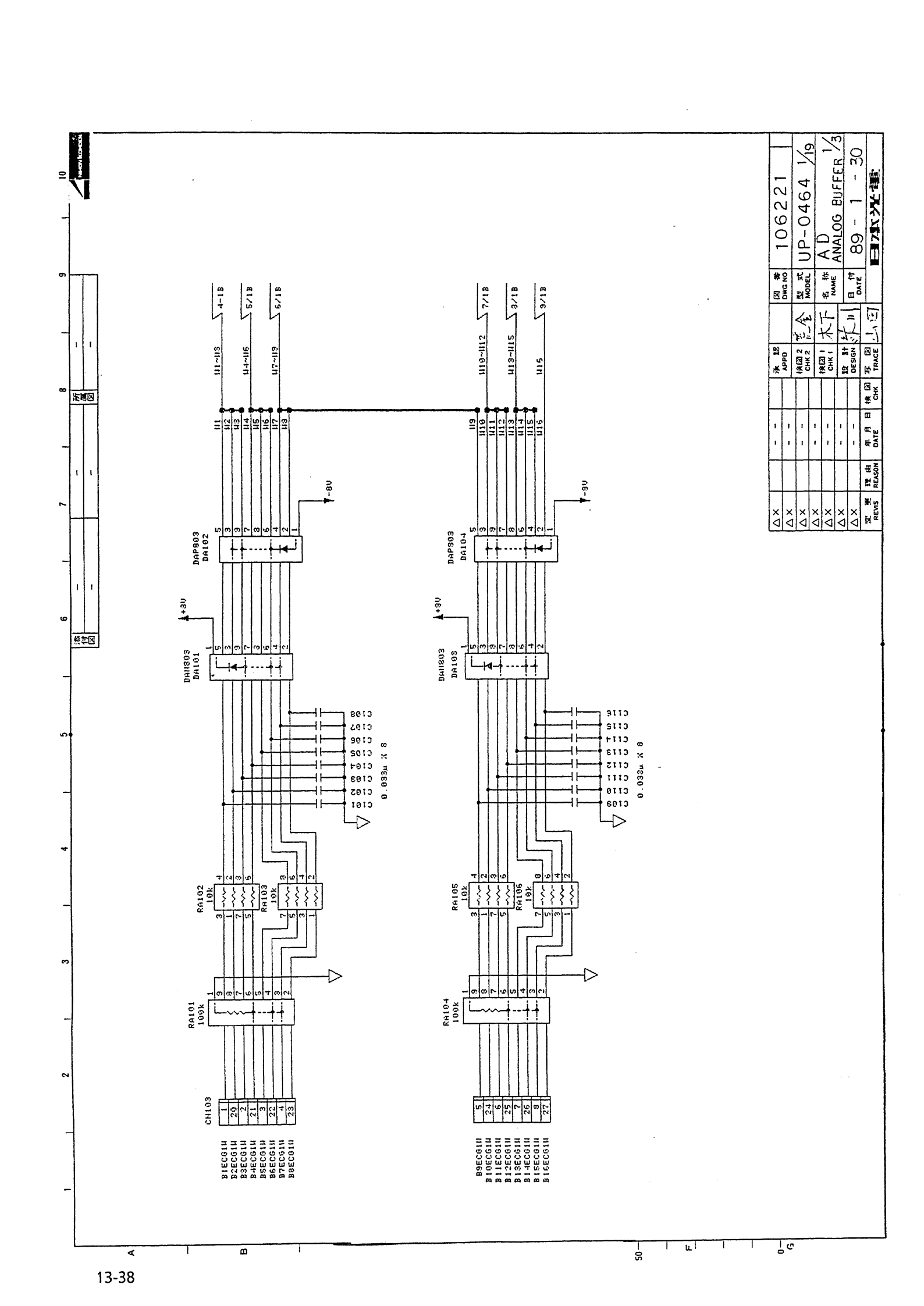
	PCB	C.DIAGRAM
EX	Z201	GP201
	J201	CN201

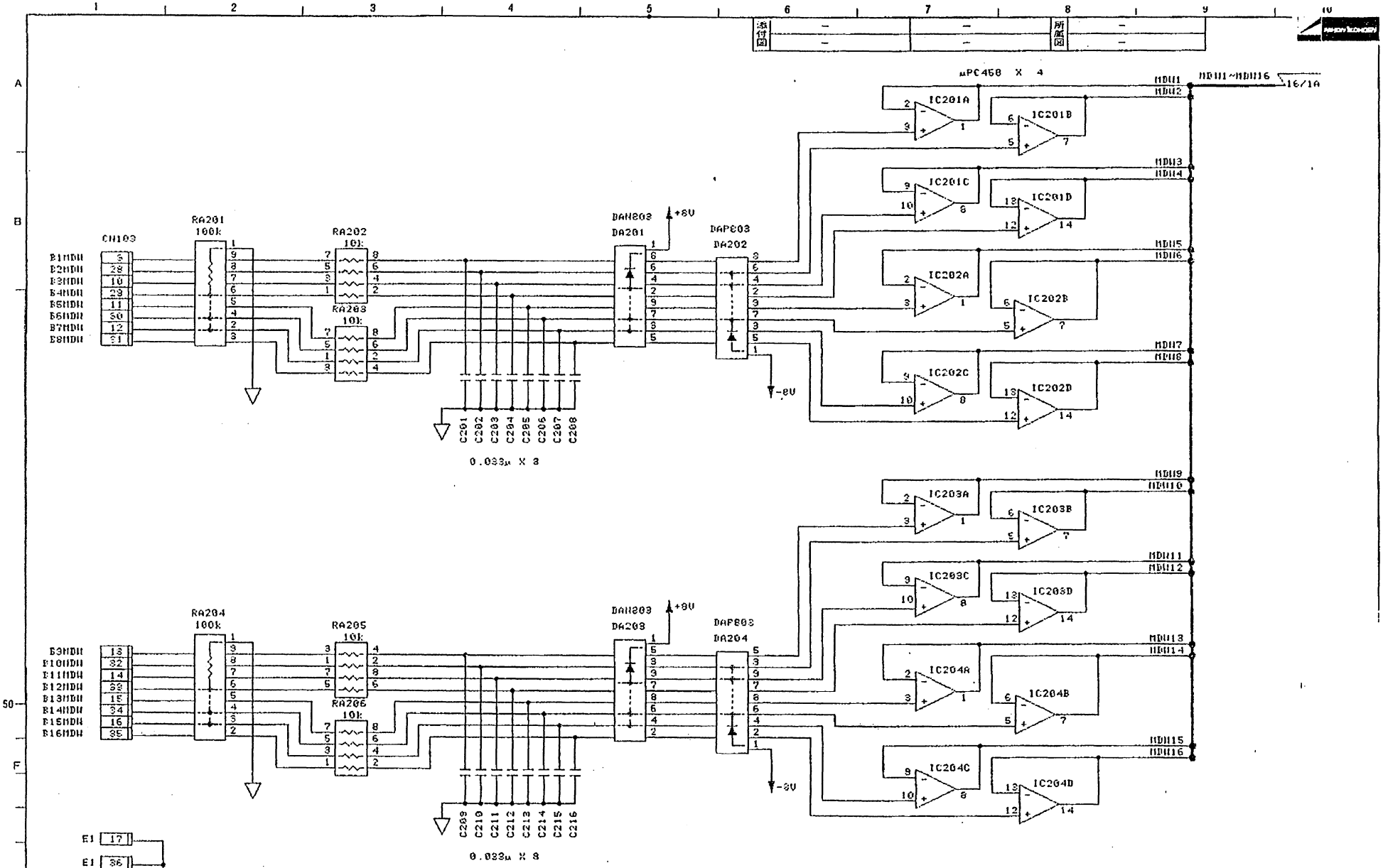
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK
△×		- -	
△×		- -	
△×		- -	
△×		- -	
⚠×1	11	'89-2-14	孫
⚠×2		62-12-11	梁
⚠×2		62-12-11	梁

承認 APPD	安田	図番 DWG NO	105600 C
検図2 CHK 2	荒金	型式 MODEL	UP-0372
検図1 CHK 1	—	名称 NAME	CRT PWB
設計 DESIGN	梁川	日付 DATE	62 - 12 - 11
写図 TRACE	斉藤	日本光電	

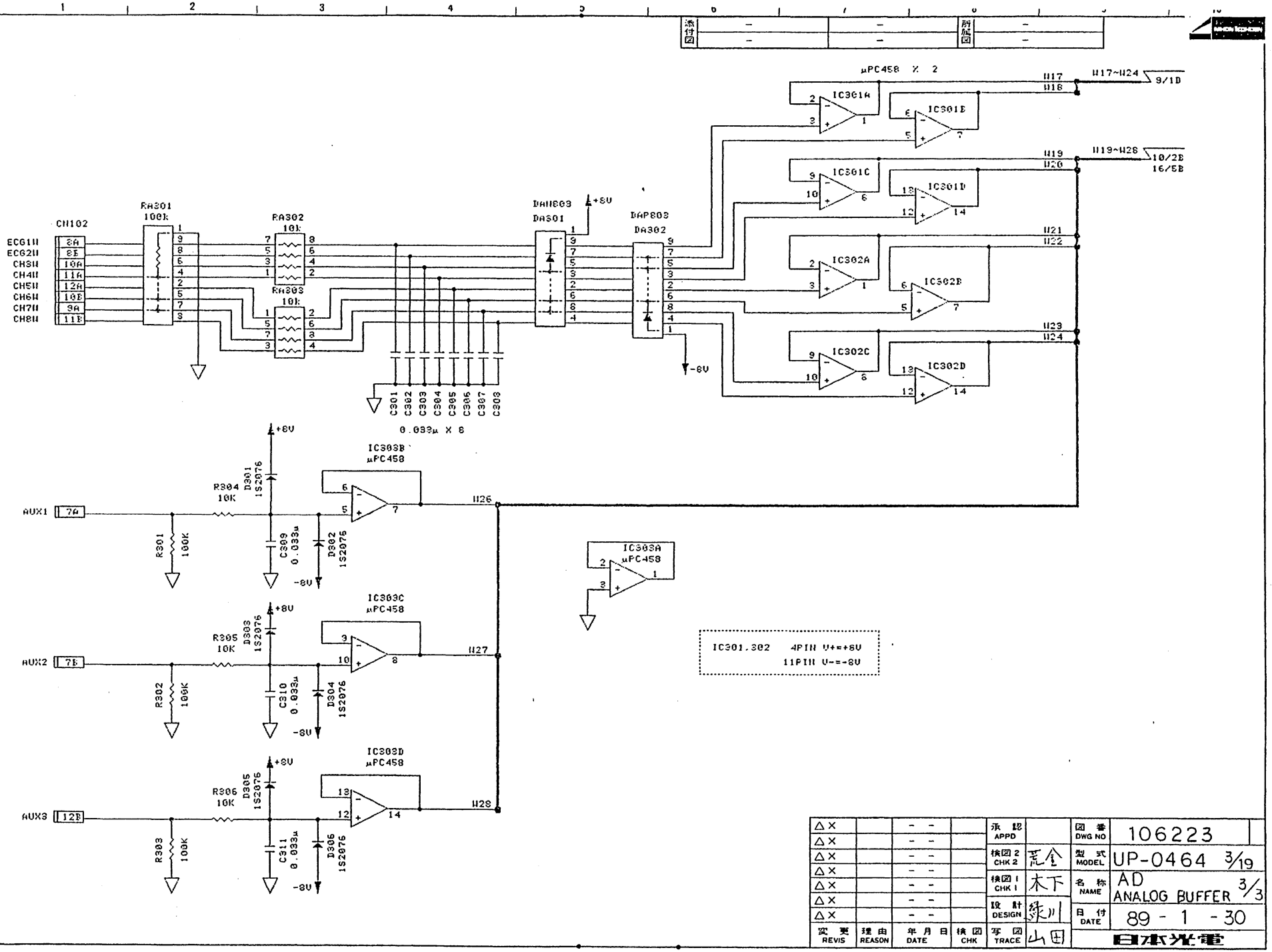


△X		- -		承認 APPD		図番 DWG NO	106220				
△X		- -		検図2 CHK 2	荒金	型式 MODEL	UP-0464				
△X		- -		検図1 CHK 1	木下	名称 NAME	AD BLOCK DIAGRAM				
△X		- -		設計 DESIGN	統川	日付 DATE	89 - 1 - 30				
△X		- -									
△X		- -									
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE	山口	日本光電					

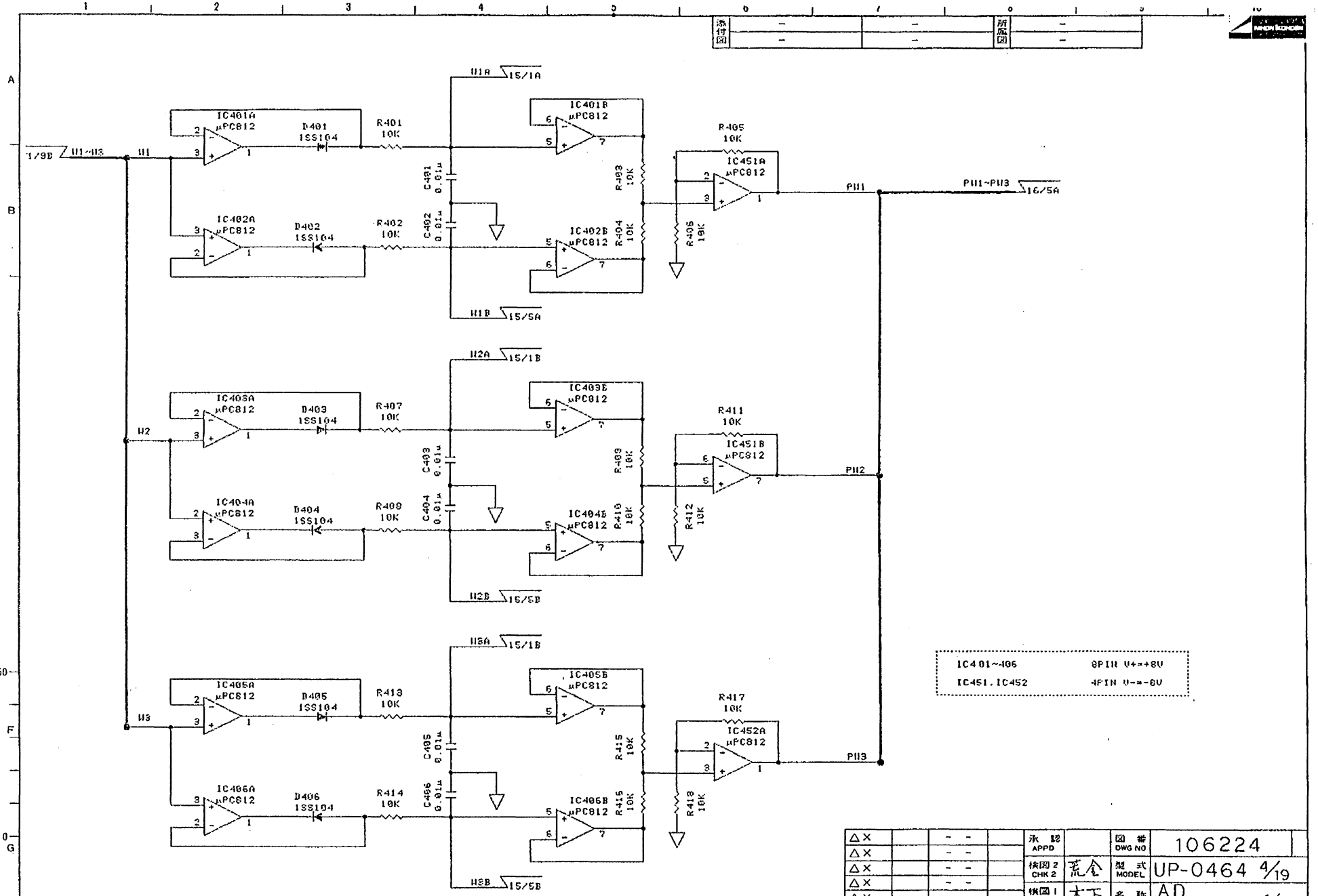

106221
UP-0464 1/19
AD
ANALOG BUFFER 1/3
89 - 1 - 30
DAP903
DA102
DAP903
DA104
DAH803
DA101
DAH803
DA103
RA101
10k
RA102
10k
RA103
10k
RA104
10k
RA105
10k
RA106
10k
CH103
0.033u X 8
0.033u X 8
+8V
+3V



△×					承認 APPD		図番 DWG NO	106222	
△×					検図2 CHK 2	荒金	型式 MODEL	UP-0464 2/19	
△×					検図1 CHK 1	木下	名称 NAME	AD ANALOG BUFFER 2/3	
△×					設計 DESIGN	緑川	日付 DATE	89 - 1 - 30	
△×					写図 TRACE	山田			
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK					日本光電	

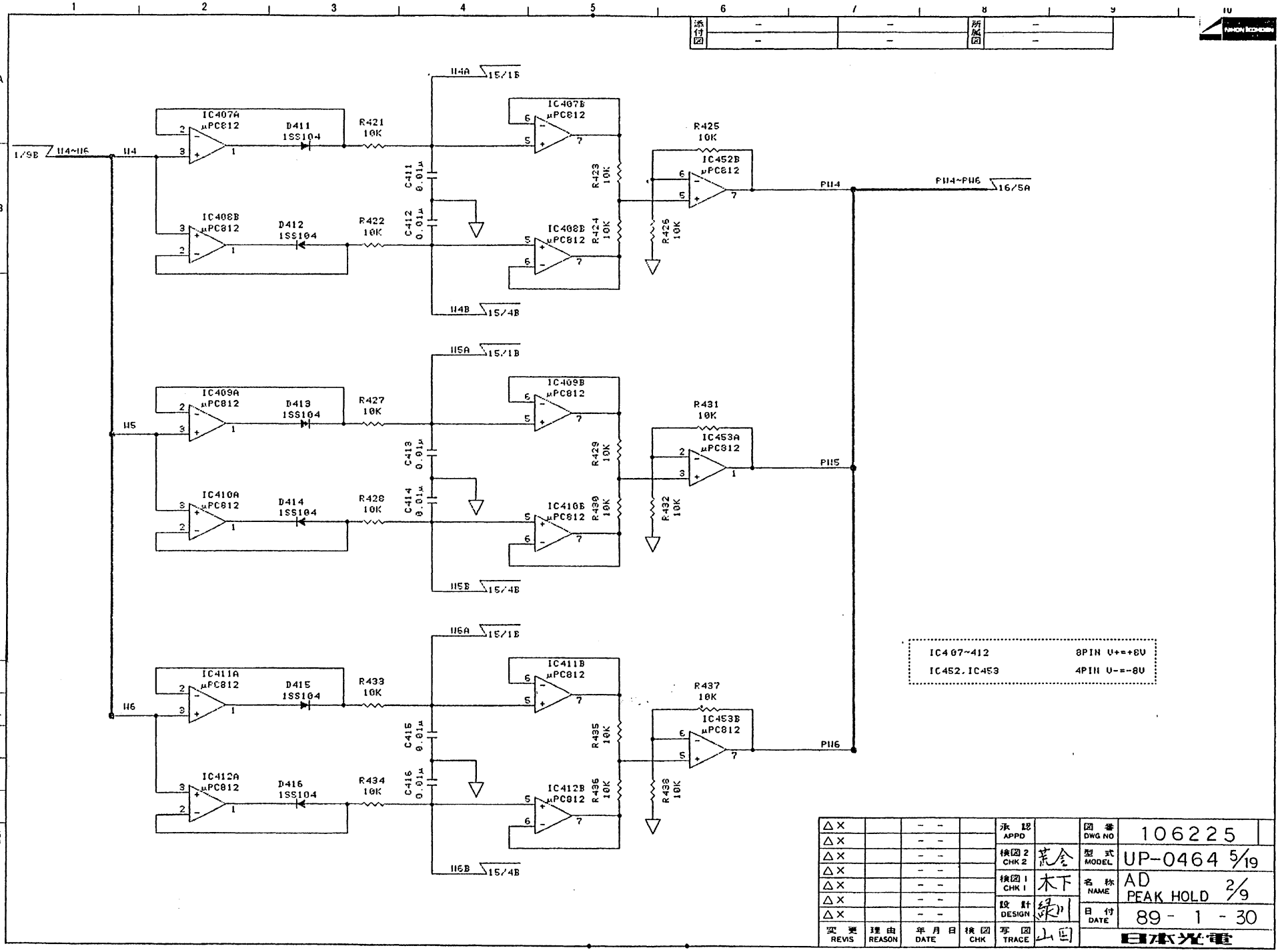


△×		- -		承認 APPD		図番 DWG NO	106223	
△×		- -		検図2 CHK 2	荒金	型式 MODEL	UP-0464	3/19
△×		- -		検図1 CHK 1	木下	名称 NAME	AD ANALOG BUFFER	3/3
△×		- -		設計 DESIGN	綠川	日付 DATE	89 - 1 - 30	
△×		- -						
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE	山田	日本光電		

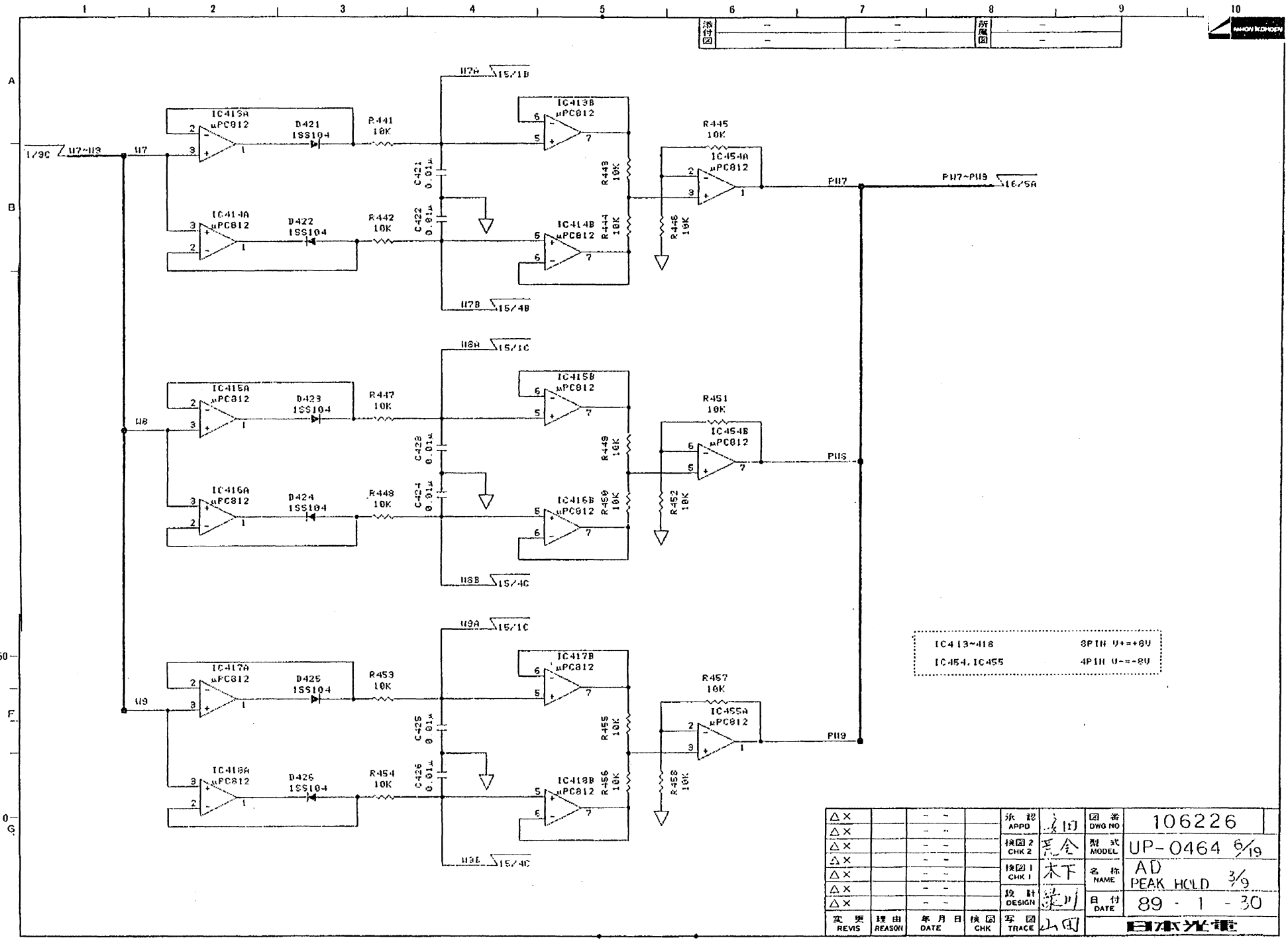


添付図	–	–	所属図	–
	–	–		–

△×		– –		承認 APPD		図番 DWG NO	106224	
△×		– –		検図2 CHK 2	荒金	型式 MODEL	UP-0464	4/19
△×		– –		検図1 CHK 1	木下	名称 NAME	AD PEAK HOLD	1/9
△×		– –		設計 DESIGN	梁川	日付 DATE	89 - 1 - 30	
△×		– –		写図 TRACE	山田			
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK				日本光電	



△×		- -		承認 APPD		図番 DWG NO	106225
△×		- -		検図2 CHK 2	荒金	型式 MODEL	UP-0464 5/19
△×		- -		検図1 CHK 1	木下	名称 NAME	AD PEAK HOLD 2/9
△×		- -		設計 DESIGN	緑川	日付 DATE	89 - 1 - 30
△×		- -		写図 TRACE	山田		日本光電
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK				

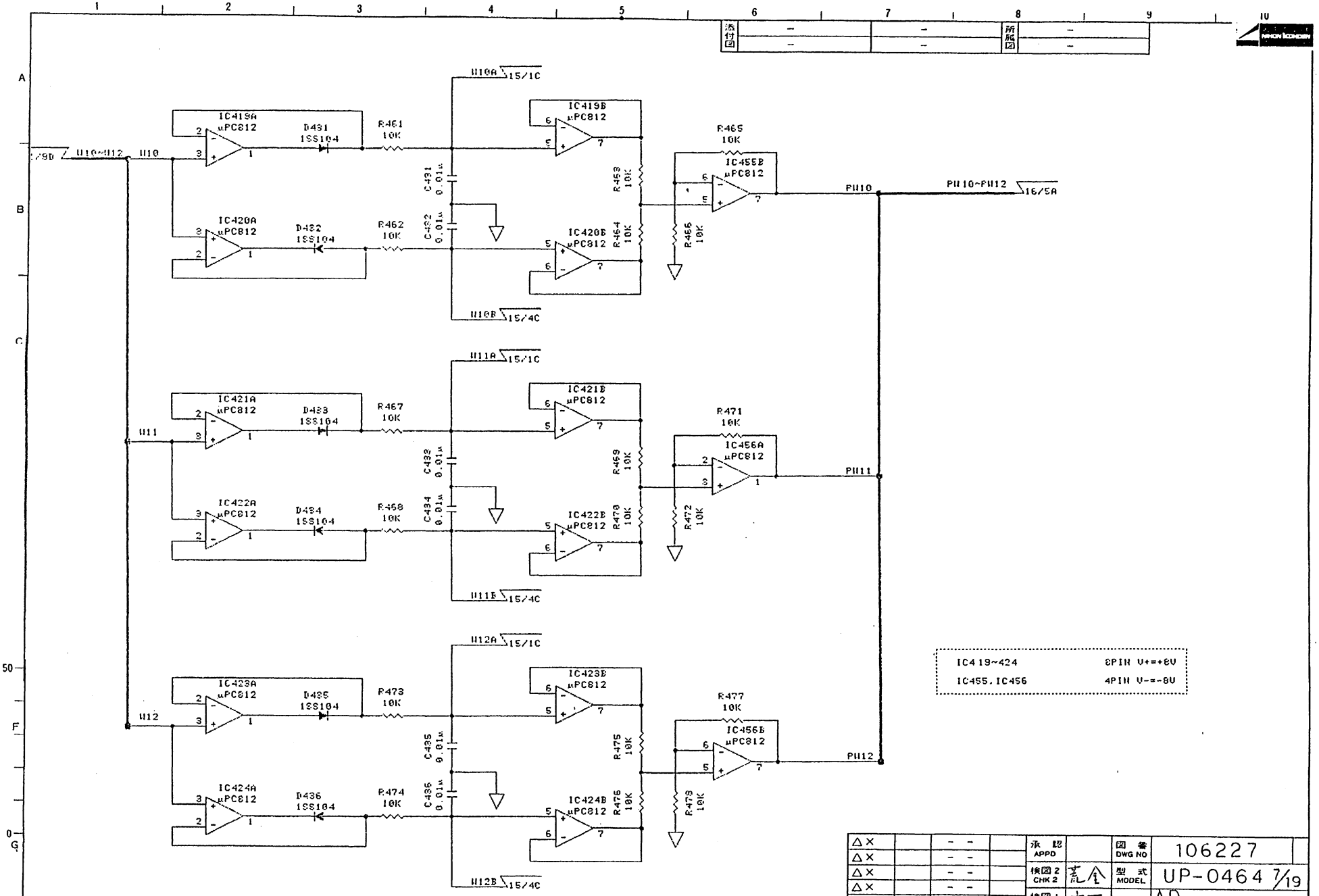


添付図	–	–	所属図	–
	–	–		–

REVIS	REASON	DATE	CHK	TRACE
△×		– –		
△×		– –		
△×		– –		
△×		– –		
△×		– –		
△×		– –		
△×		– –		山田

APPD	永田
CHK 2	長倉
CHK 1	木下
DESIGN	渡川
DWG NO	106226
MODEL	UP-0464 6/19
NAME	AD PEAK HOLD 3/9
DATE	89 - 1 - 30

日本光電

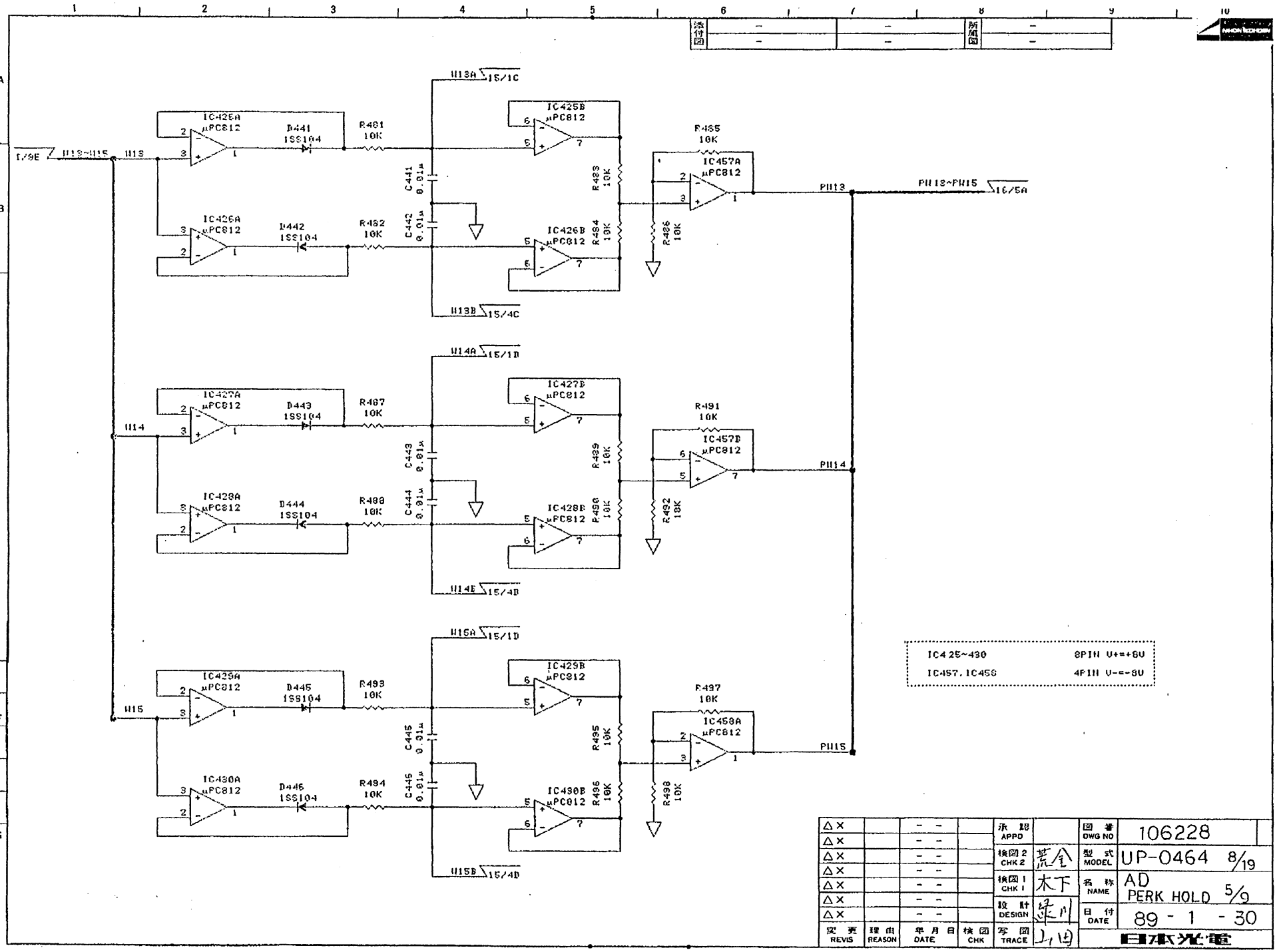


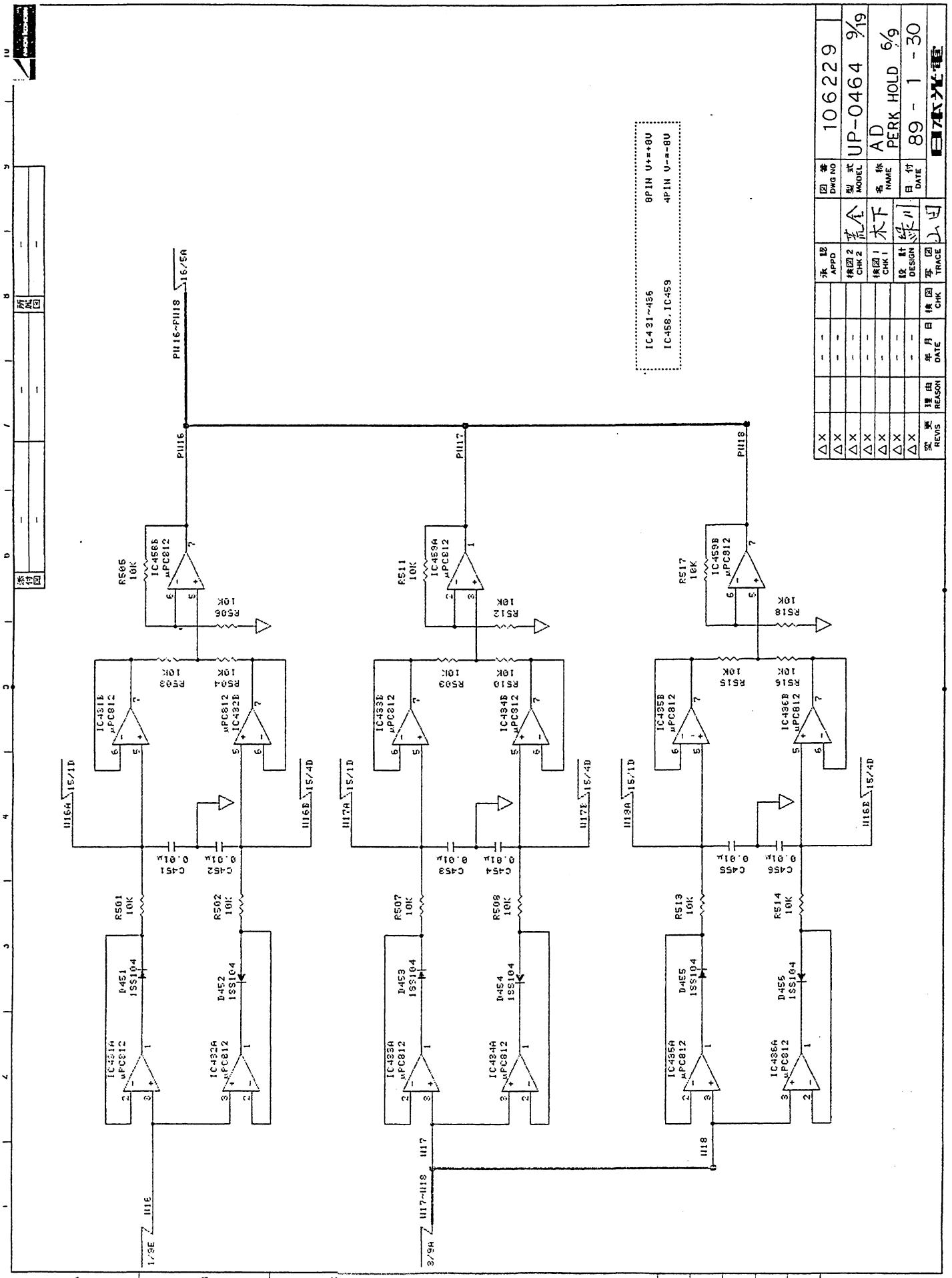
添付図	–	–	所属図	–
	–	–		–

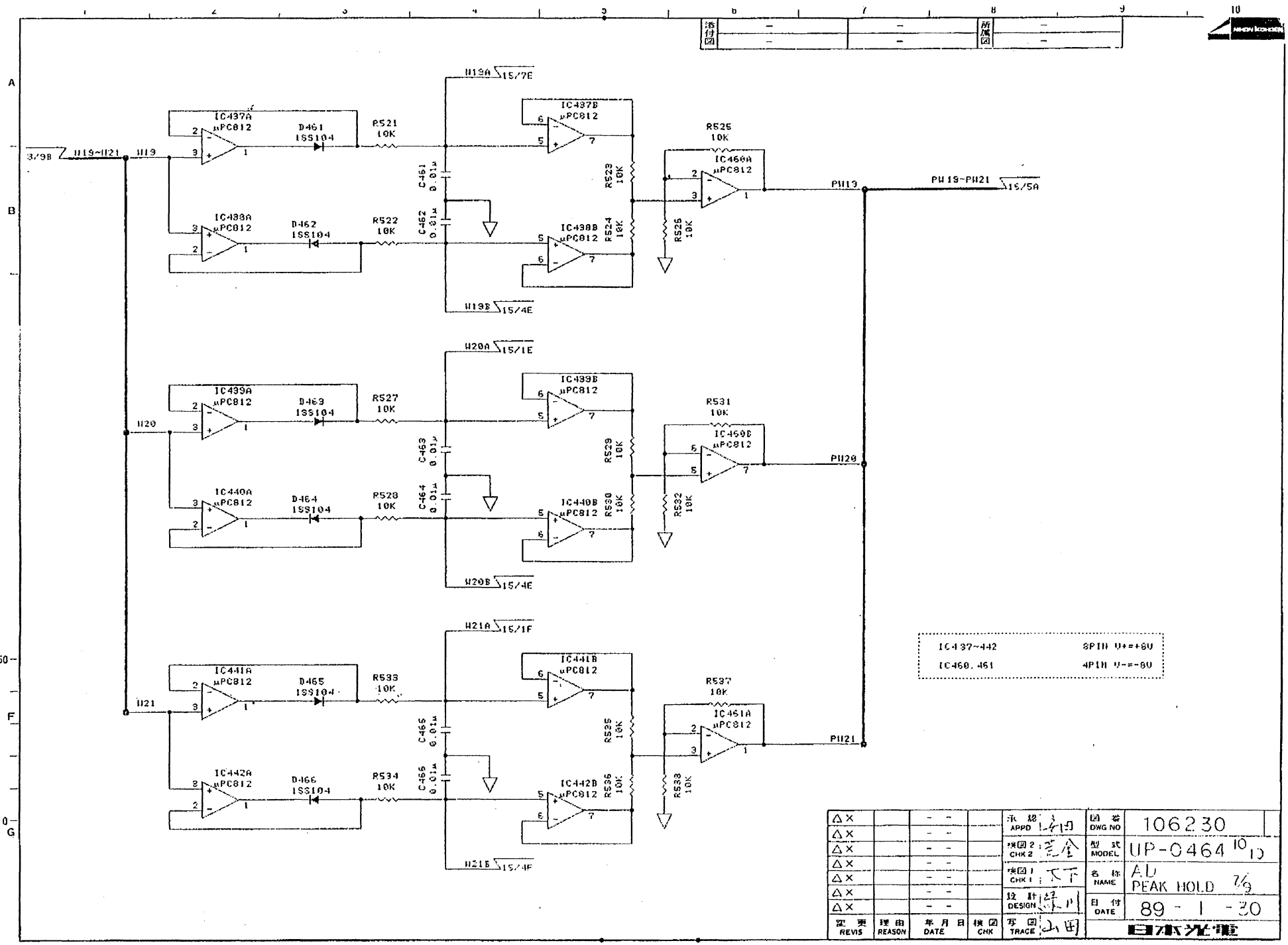
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE	山田
△×		– –		設計 DESIGN	緑川
△×		– –		検図1 CHK 1	木下
△×		– –		検図2 CHK 2	荒金
△×		– –		承認 APPD	
△×		– –			
△×		– –			
△×		– –			

図番 DWG NO	106227
型式 MODEL	UP-0464 7/19
名称 NAME	AD PERK HOLD 4/9
日付 DATE	89 - 1 - 30

日本光電

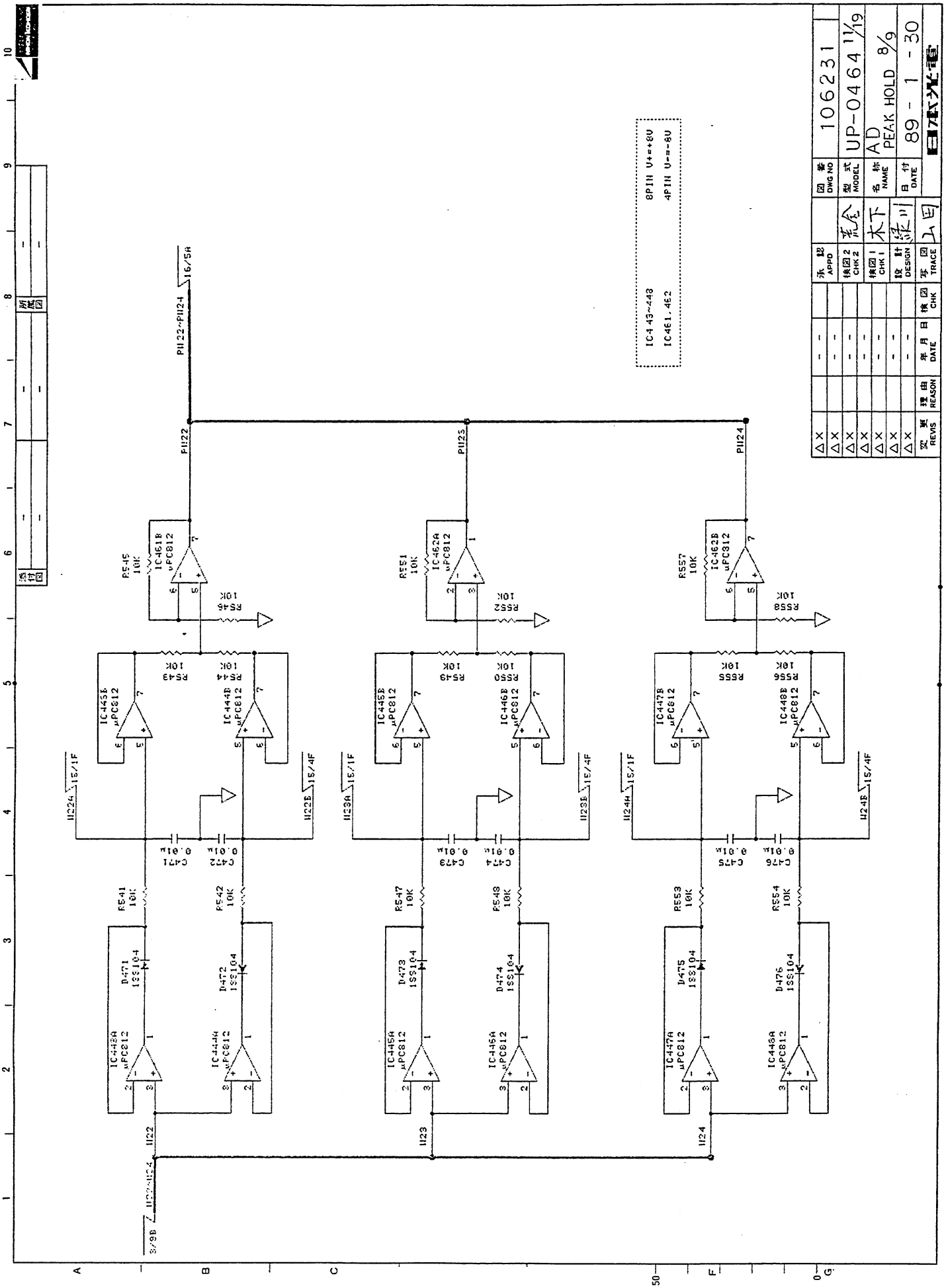

IC425A μPC812
D441 1SS104
R481 10K
IC425B μPC812
R485 10K
IC457A μPC812
PH13
PH13~PH15
IC426A μPC812
D442 1SS104
R482 10K
IC426B μPC812
R484 10K
R486 10K
C441 0.01μ
C442 0.01μ
R483 10K
H13A
H13B
IC427A μPC812
D443 1SS104
R487 10K
IC427B μPC812
R491 10K
IC457B μPC812
PH14
IC428A μPC812
D444 1SS104
R488 10K
IC428B μPC812
R490 10K
R492 10K
C443 0.01μ
C444 0.01μ
R489 10K
H14A
H14B
IC429A μPC812
D445 1SS104
R493 10K
IC429B μPC812
R497 10K
IC458A μPC812
PH15
IC430A μPC812
D446 1SS104
R494 10K
IC430B μPC812
R496 10K
R498 10K
C445 0.01μ
C446 0.01μ
R495 10K
H15A
H15B
IC425~430 8PIN V+=+5V
IC457, IC458 4PIN V-=-5V
APPD
CHK2 荒金
CHK1 木下
DESIGN 梁川
TRACE 山田
DWG NO 106228
MODEL UP-0464 8/19
NAME AD PERK HOLD 5/9
DATE 89 - 1 - 30
日本光電


PH16~PH18
IC431~435
IC458.IC459
8PIN V+=+8V
4PIN V-=-8V
106229
UP-0464 9/19
AD
PERK HOLD 6/9
89 - 1 - 30
日本光電

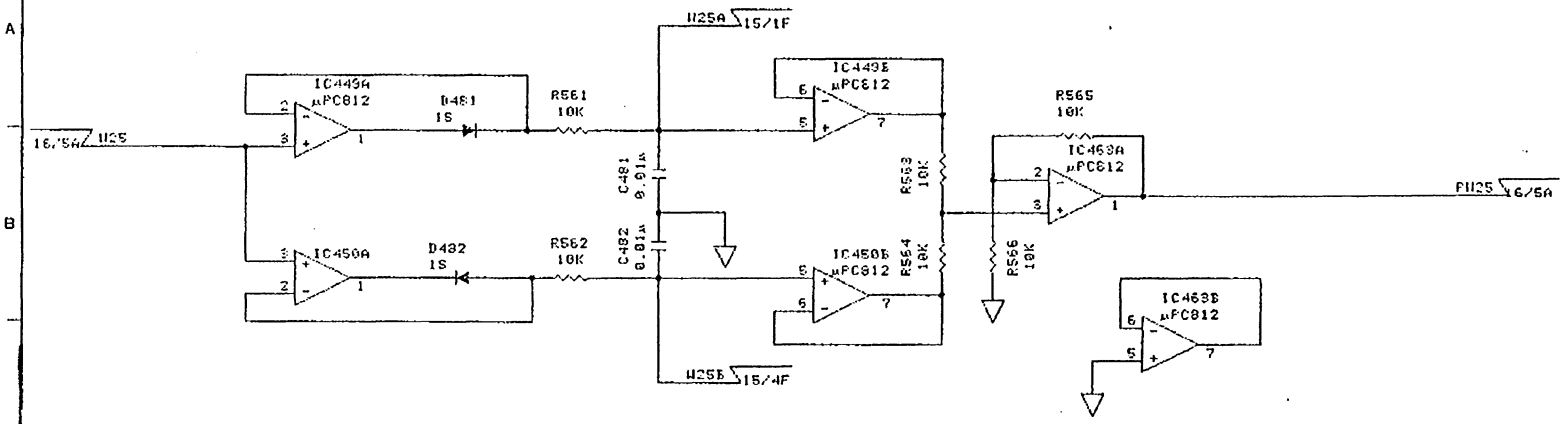


添付図	–	–	所属図	–	–		

△×		– –		承認 APPD		図番 DWG NO	106230
△×		– –		検図2 CHK 2		型式 MODEL	UP-0464 10
△×		– –		検図1 CHK 1		名称 NAME	AD PEAK HOLD 1/9
△×		– –		設計 DESIGN		日付 DATE	89 - 1 - 30
△×		– –		写図 TRACE			
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK				

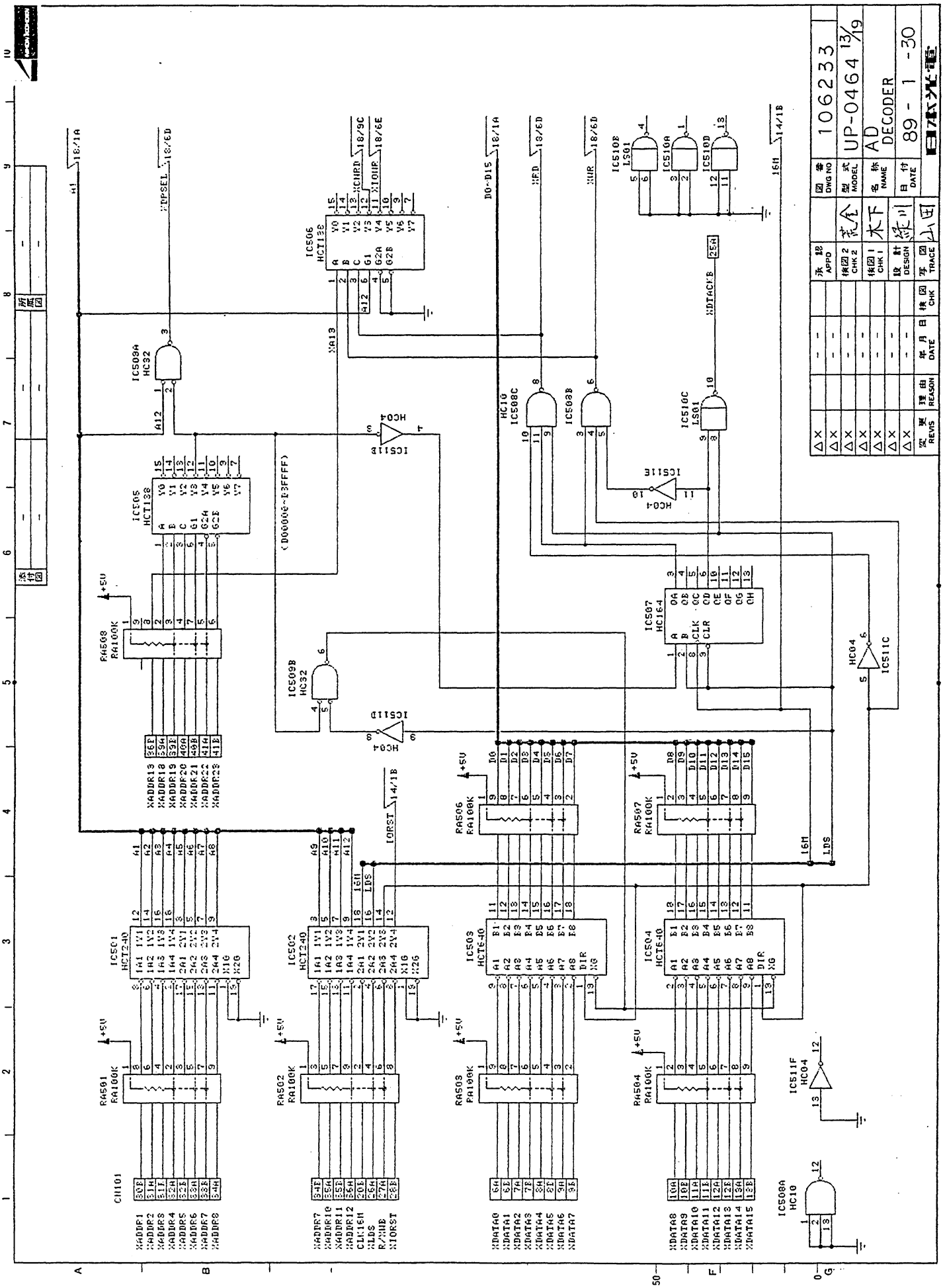

IC443~448 8PIN V+=+8V
IC461.462 4PIN V-=-8V
P1122~P1124
P1122
P1123
P1124
IC461B μPC812
IC462A μPC812
IC462B μPC812
IC443B μPC812
IC444B μPC812
IC445B μPC812
IC446B μPC812
IC447B μPC812
IC448B μPC812
IC443A μPC812
IC444A μPC812
IC445A μPC812
IC446A μPC812
IC447A μPC812
IC448A μPC812
R545 10K
R546 10K
R551 10K
R552 10K
R557 10K
R558 10K
R543 10K
R544 10K
R549 10K
R550 10K
R555 10K
R556 10K
C471 0.01μ
C472 0.01μ
C473 0.01μ
C474 0.01μ
C475 0.01μ
C476 0.01μ
R541 10K
R542 10K
R547 10K
R548 10K
R553 10K
R554 10K
D471 1SS104
D472 1SS104
D473 1SS104
D474 1SS104
D475 1SS104
D476 1SS104
U22
U23
U24
U22A 15/1F
U22B 15/4F
U23A 15/1F
U23B 15/4F
U24A 15/1F
U24B 15/4F
89/98
P1122~P1124 16/54
添付図
所属図
△X
承認 APPD
検図2 CHK 2
検図1 CHK 1
設計 DESIGN
写図 TRACE
検図 CHK
年月日 DATE
理由 REASON
変更 REVIS
図番 DWG NO 106231
型式 MODEL UP-0464 11/19
名称 NAME AD PEAK HOLD 8/9
日付 DATE 89 - 1 - 30
東光電

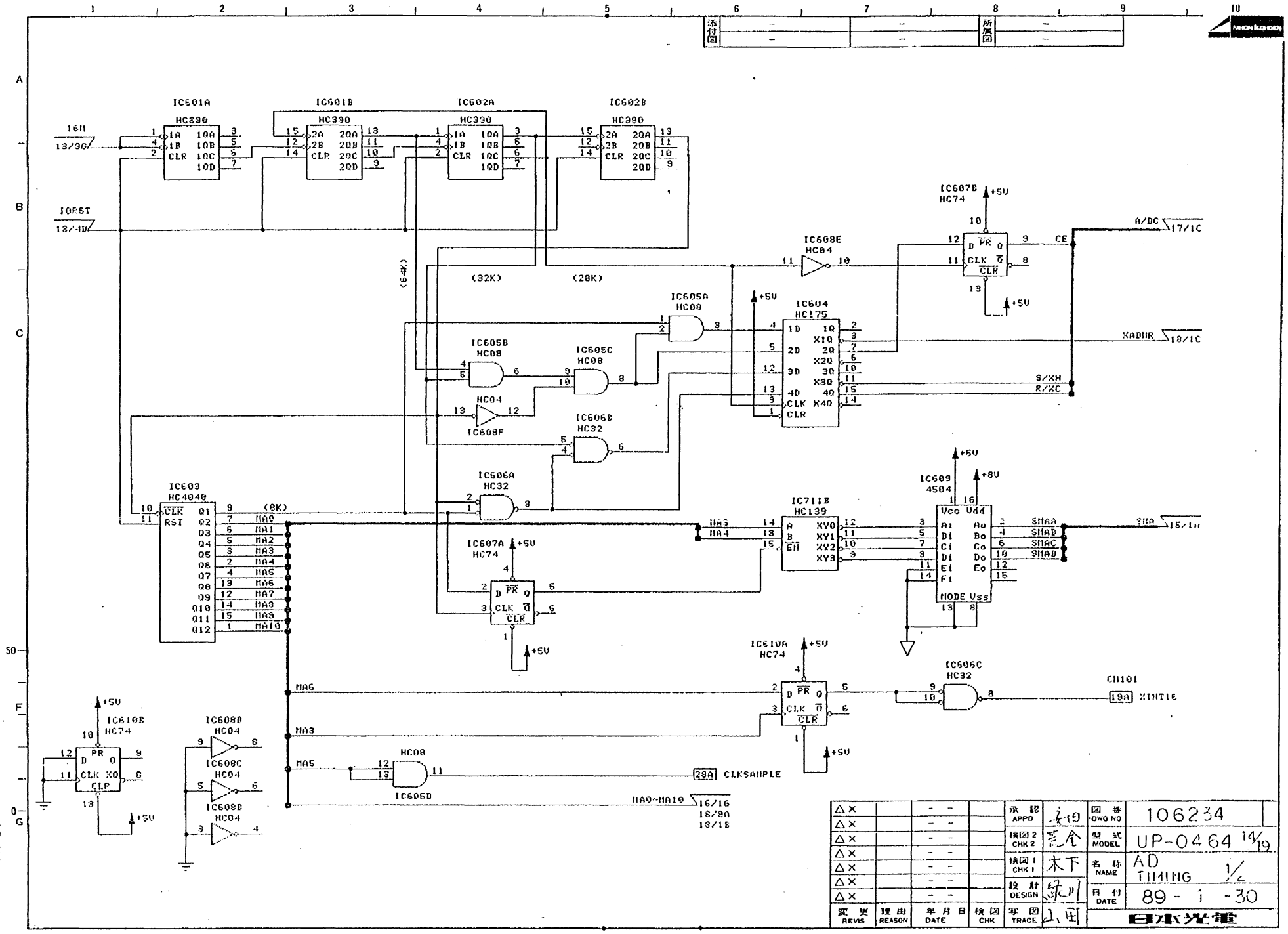
添付図	–	–	所属図	–
	–	–		–



IC449, IC450 4PIN V+=+8V
IC463 11PIN V-=-8V

△×		– –		承認 APPD		図番 DWG NO	106232	
△×		– –		検図2 CHK 2	荒倉	型式 MODEL	UP-0464 12/19	
△×		– –		検図1 CHK 1	木下	名称 NAME	AD PEAK HOLD 9/9	
△×		– –		設計 DESIGN	綠川	日付 DATE	89 - 1 - 30	
△×		– –		写図 TRACE	山田		日本光電	
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK					





添付図	–	–	所属図	–
	–	–		–

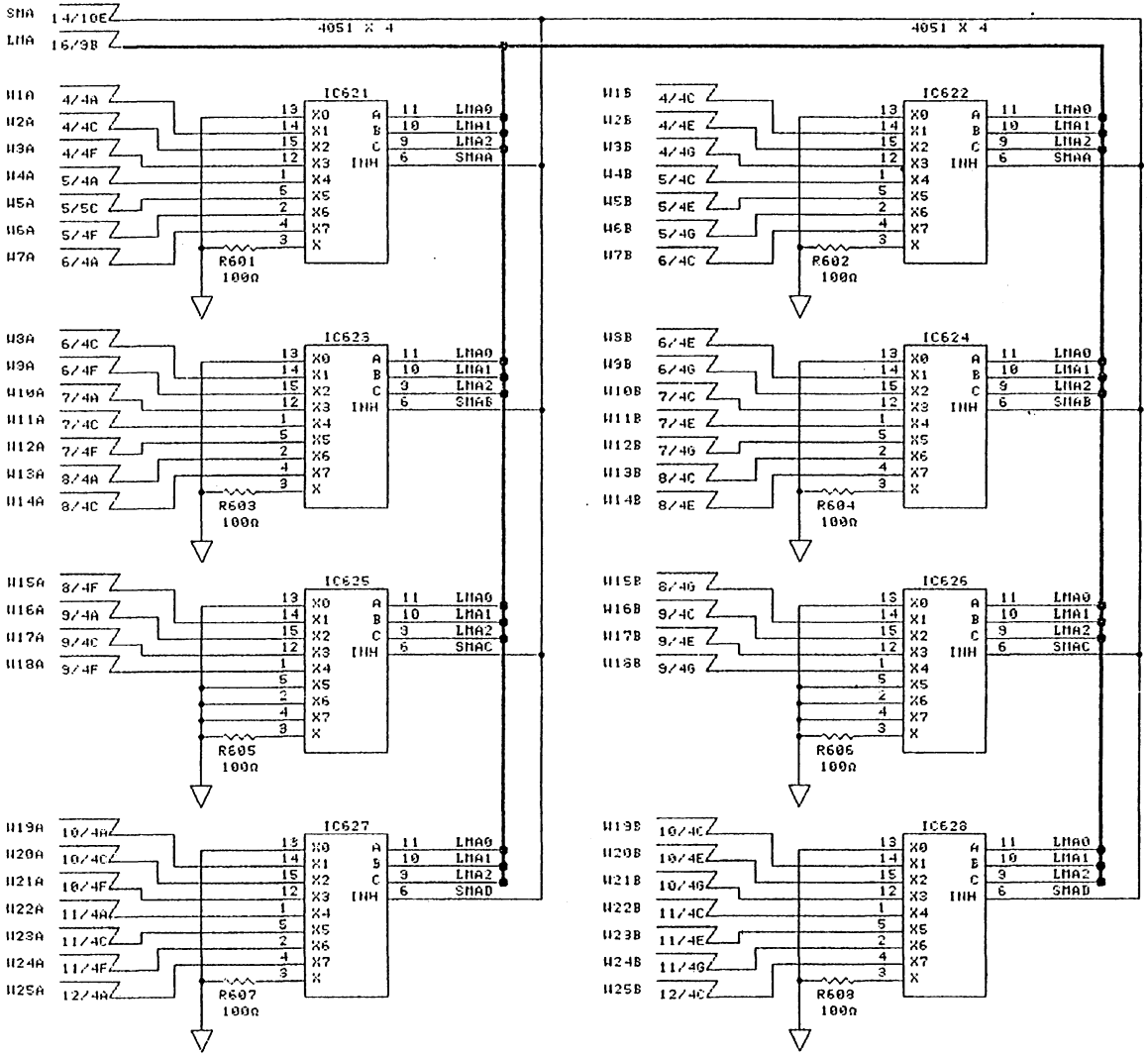
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK
△×		– –	
△×		– –	
△×		– –	
△×		– –	
△×		– –	
△×		– –	
△×		– –	

承認 APPD	永19
検図2 CHK 2	芝金
検図1 CHK 1	木下
設計 DESIGN	緑川
製図 TRACE	上田

図番 DWG NO	106234
型式 MODEL	UP-0464 14/19
名称 NAME	AD TIMING 1/2
日付 DATE	89 - 1 - 30

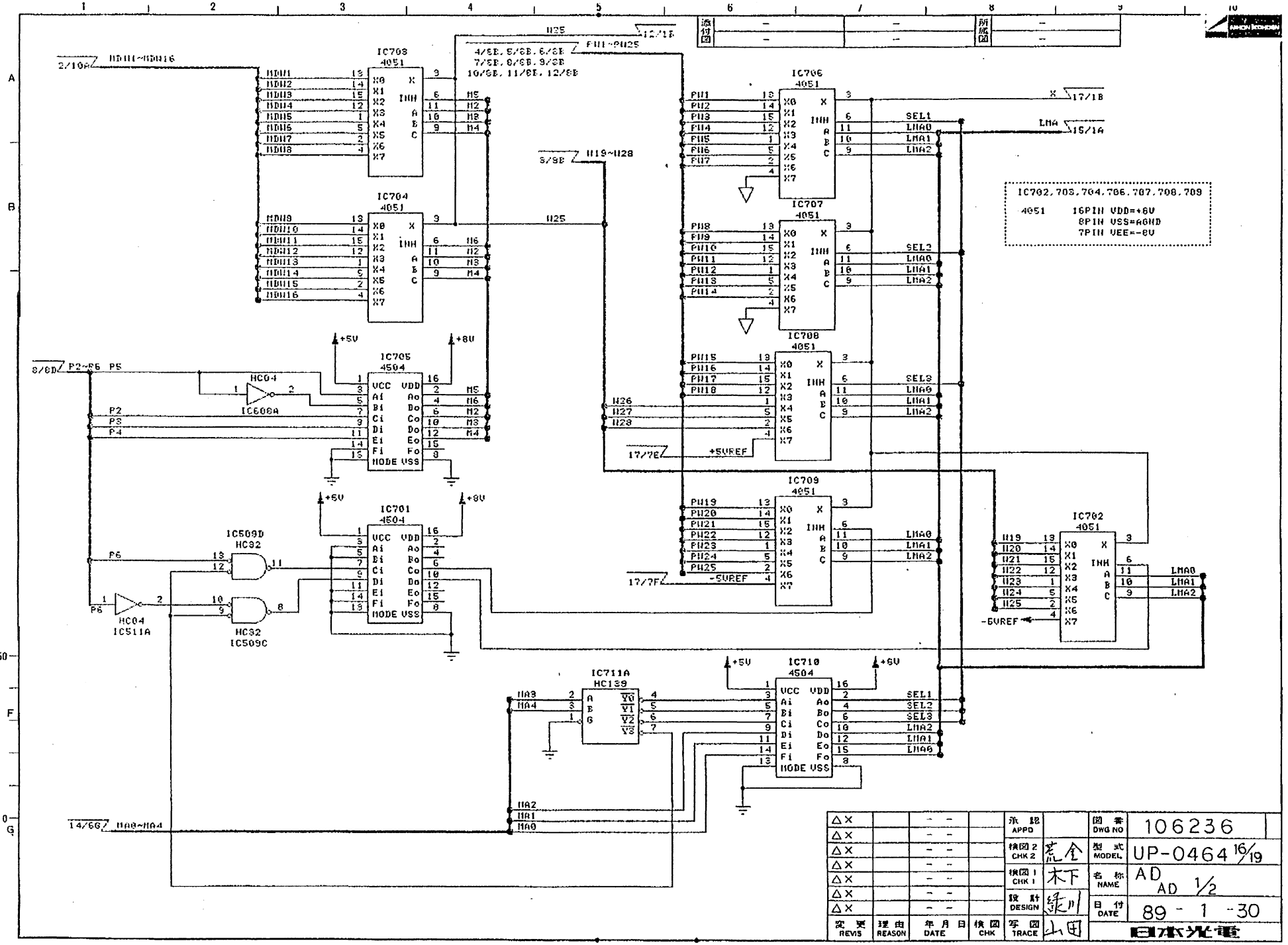
日本光電

添付図	–	–	所属図	–
	–	–		–



IC621~IC628
7PIN....-8V
8PIN....E1
16PIN...+8V

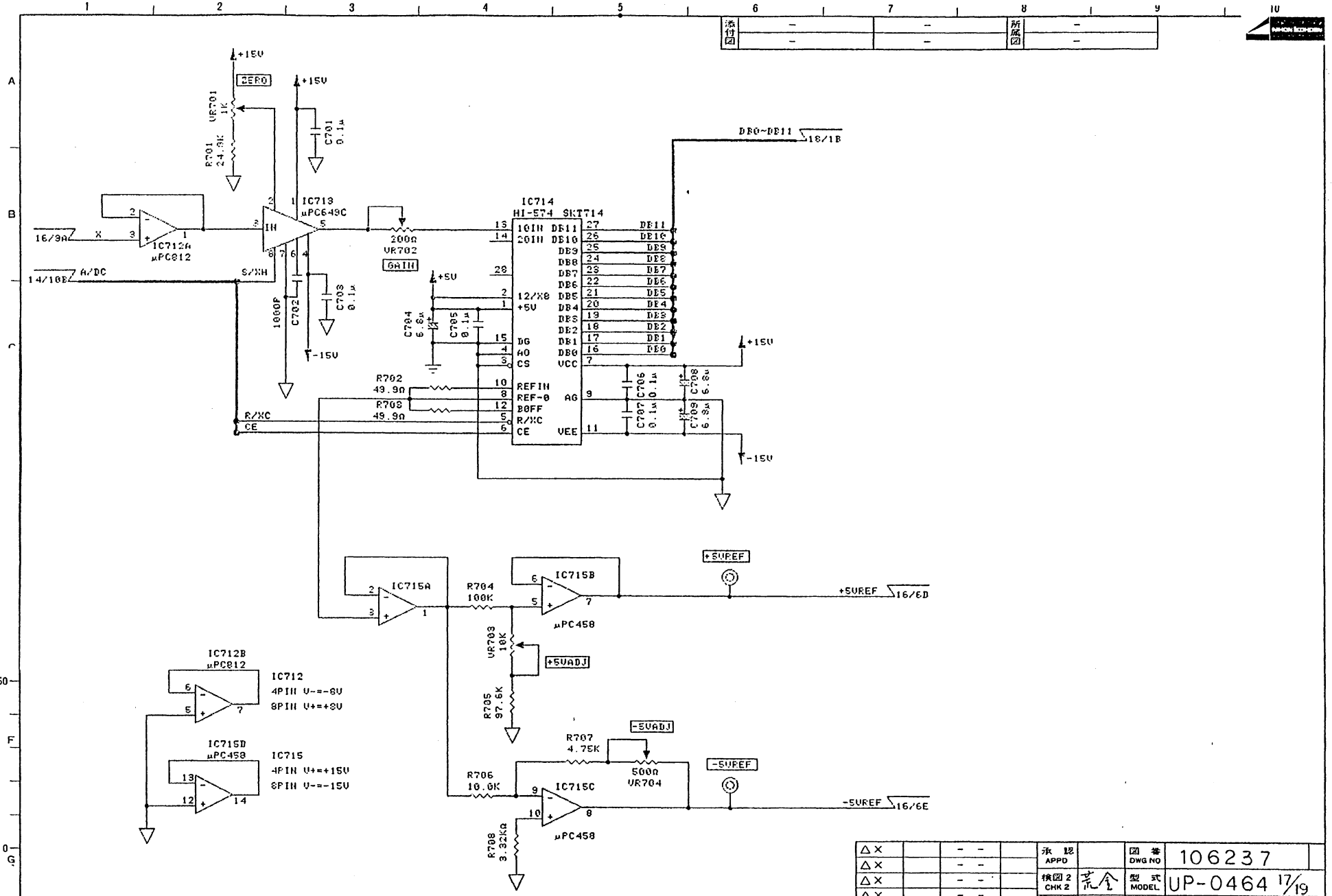
乙×		– –		承認 APPD		図番 DWG NO	106235
乙×		– –		検図2 CHK 2		型式 MODEL	UP-0464 15/19
乙×		– –		検図1 CHK 1		名称 NAME	AD TIMING 2/2
乙×		– –		設計 DESIGN		日付 DATE	89 - 1 - 30
乙×		– –					
乙×		– –					
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE		日本光電	



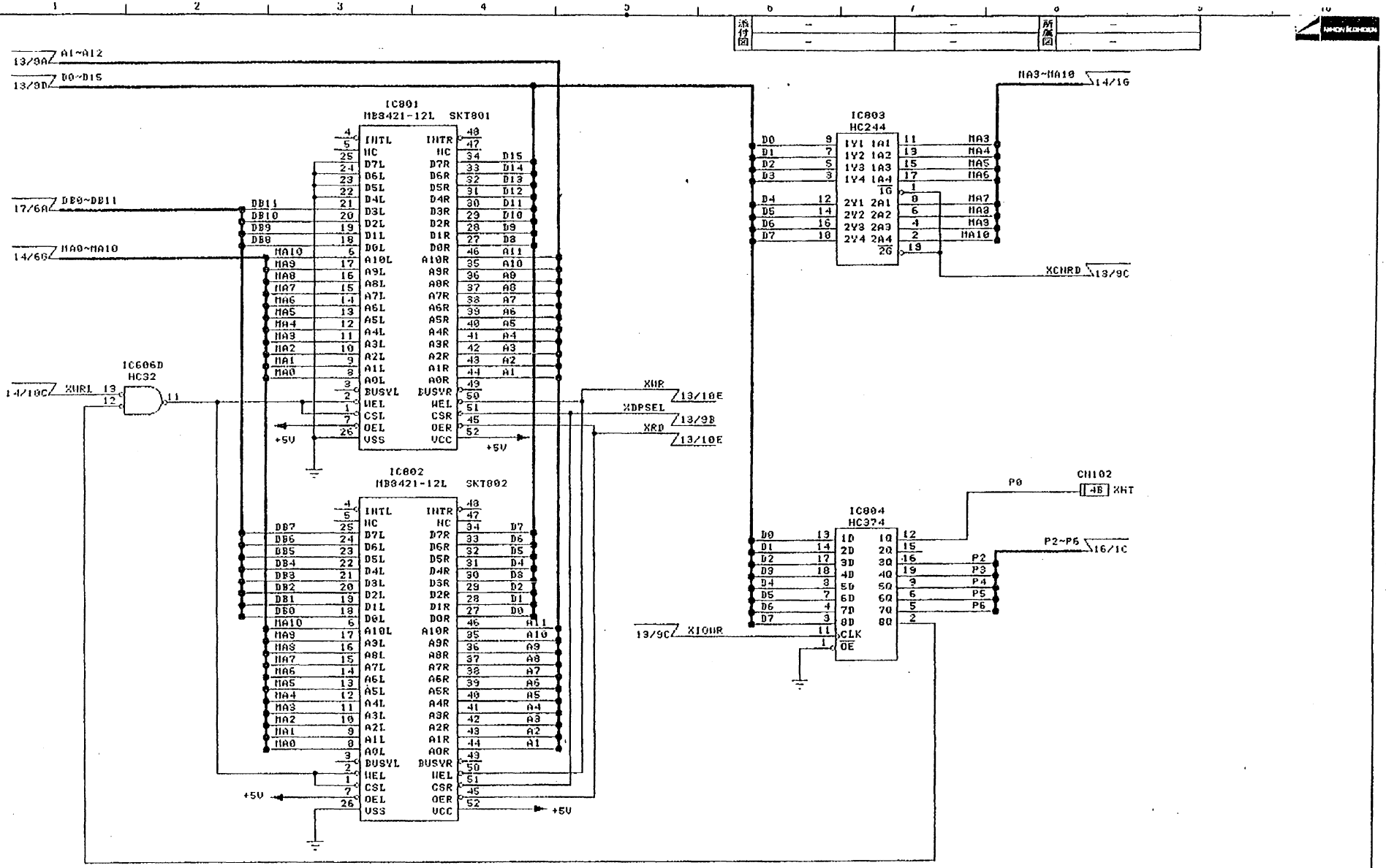
添付図	–	–		所属図	–			

変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE			
△×		– –			承認 APPD		図番 DWG NO	106236
△×		– –			検図2 CHK 2	荒金	型式 MODEL	UP-0464 16/19
△×		– –			検図1 CHK 1	木下	名称 NAME	AD AD 1/2
△×		– –			設計 DESIGN	緑川	日付 DATE	89 - 1 - 30
△×		– –				山田		日本光電

添付図	–	–	所属図	–
	–	–		–



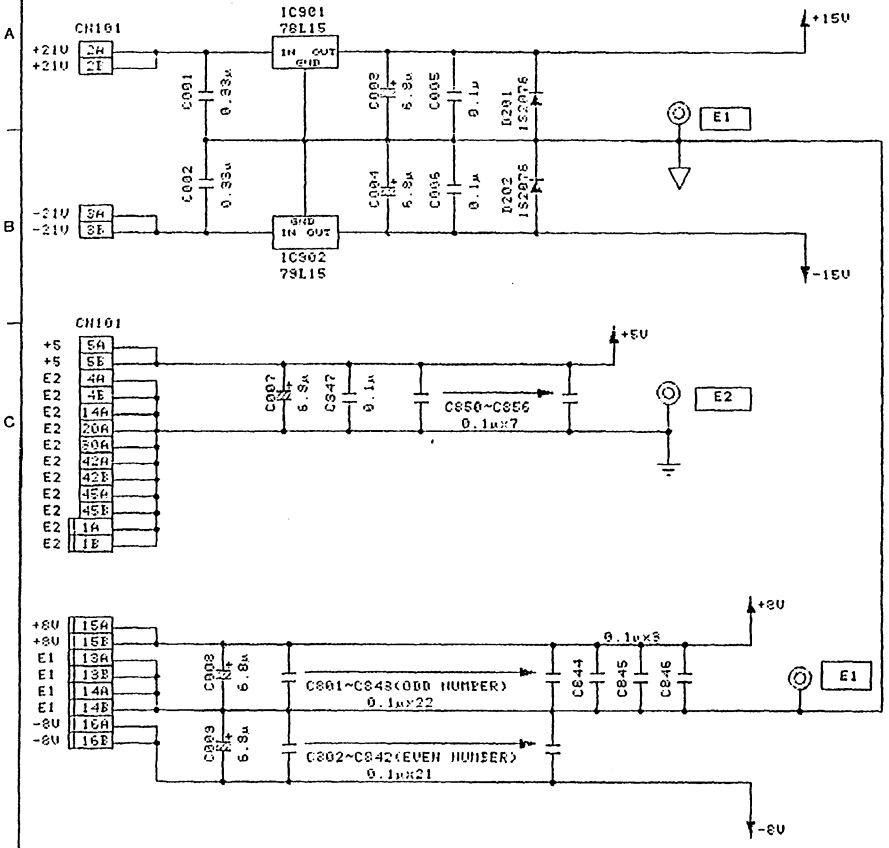
△×		– –		承認 APPD		図番 DWG NO	106237	
△×		– –		検図2 CHK 2	荒金	型式 MODEL	UP-0464 17/19	
△×		– –		検図1 CHK 1	木下	名称 NAME	AD AD 2/2	
△×		– –		設計 DESIGN	梁川	日付 DATE	89 - 1 - 30	
△×		– –		写図 TRACE	山田			
△×		– –						
変更 REVS	理由 REASON	年月日 DATE	検図 CHK				日本光電	



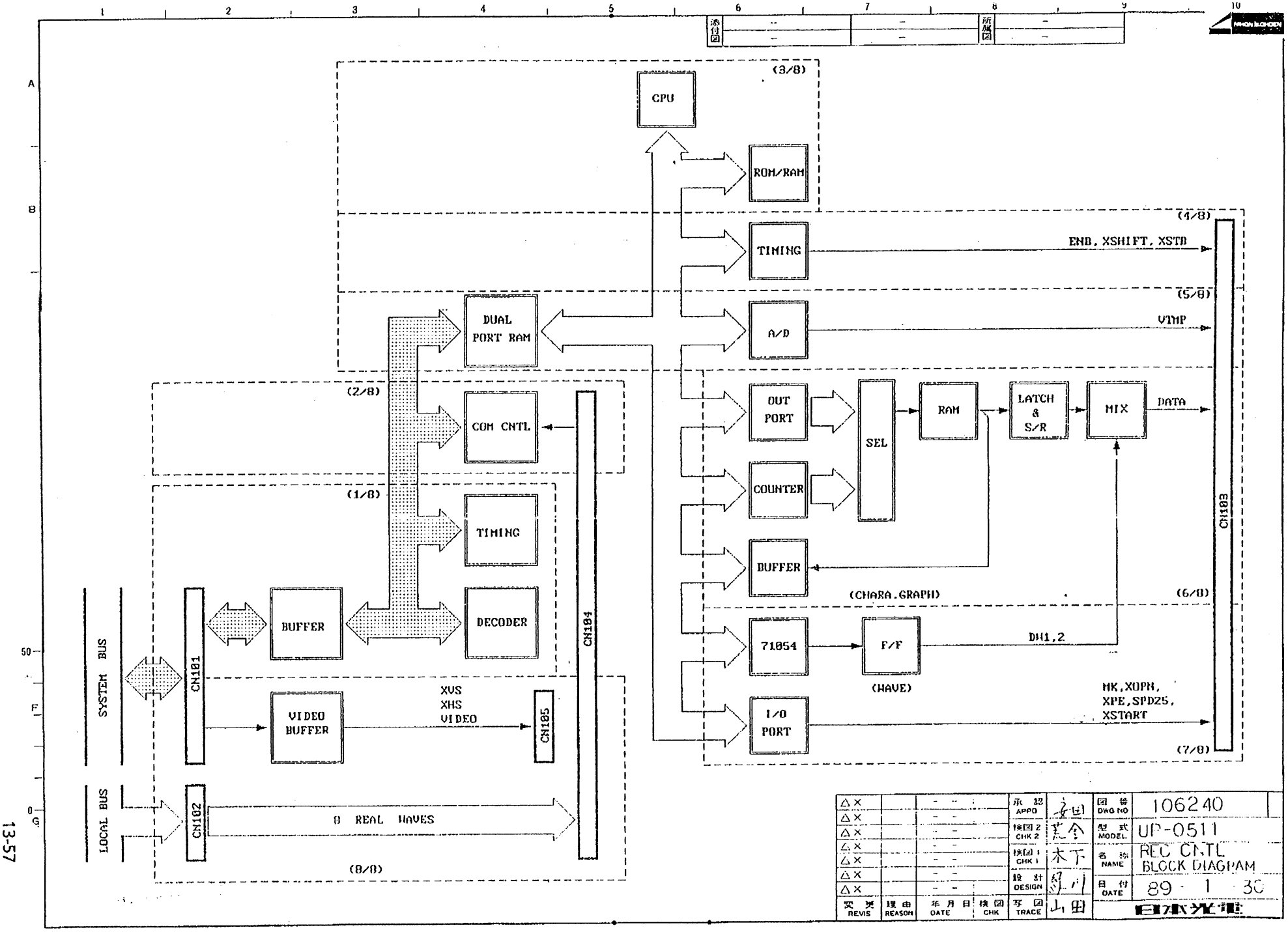
添付図	-	-		所属図	-				

△×		- -		承認 APPD	永田	図番 DWG NO	106238		
△×		- -		検図2 CHK 2	荒金	型式 MODEL	UP-3464 18/19		
△×		- -		検図1 CHK 1	木下	名称 NAME	AD MEMORY		
△×		- -		設計 DESIGN	鈴川	日付 DATE	89 - 1 - 30		
△×		- -		写図 TRACE	山田				
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK				日本光電		

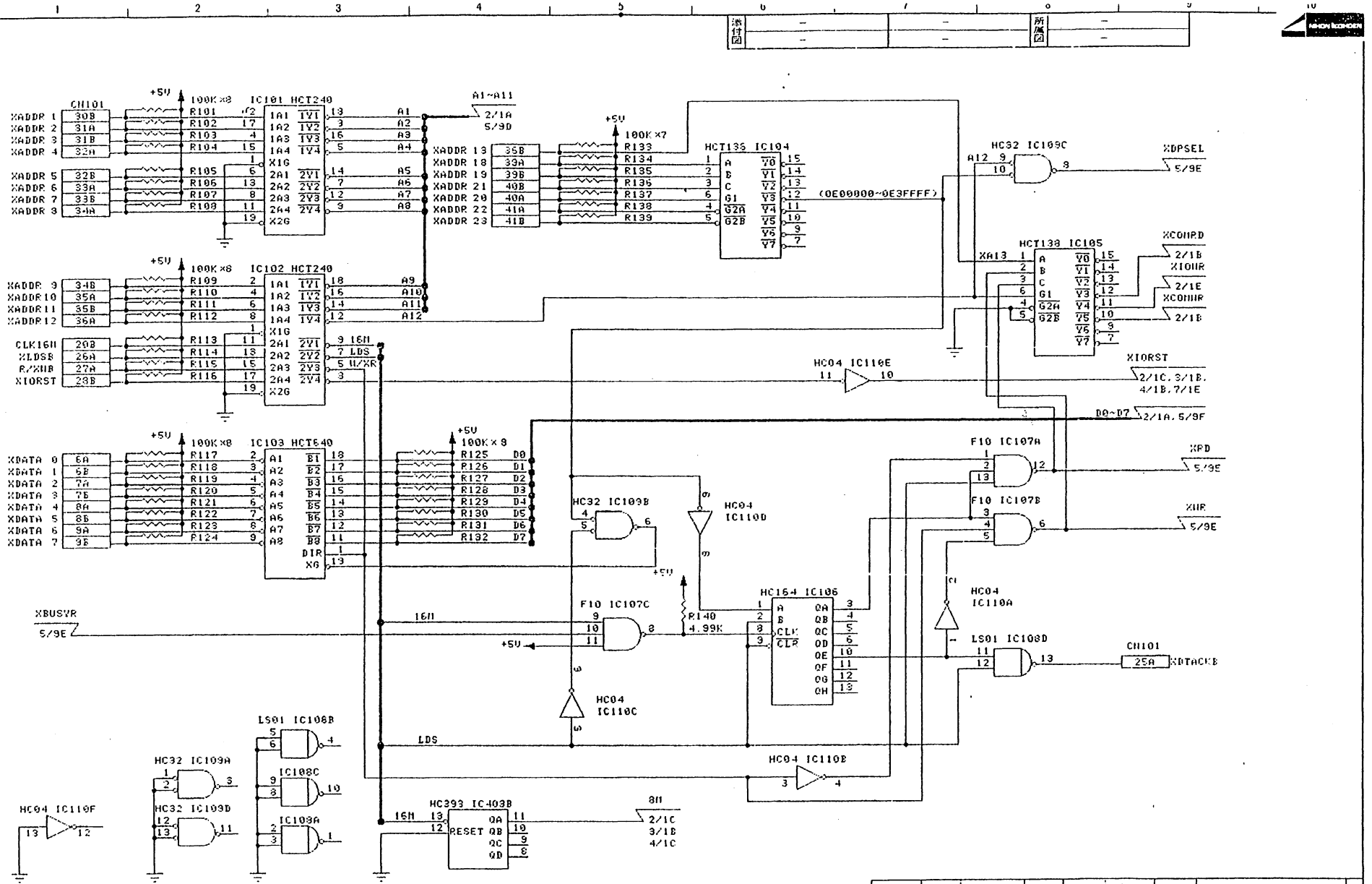
添付図	–	–	所属図	–
	–	–		–



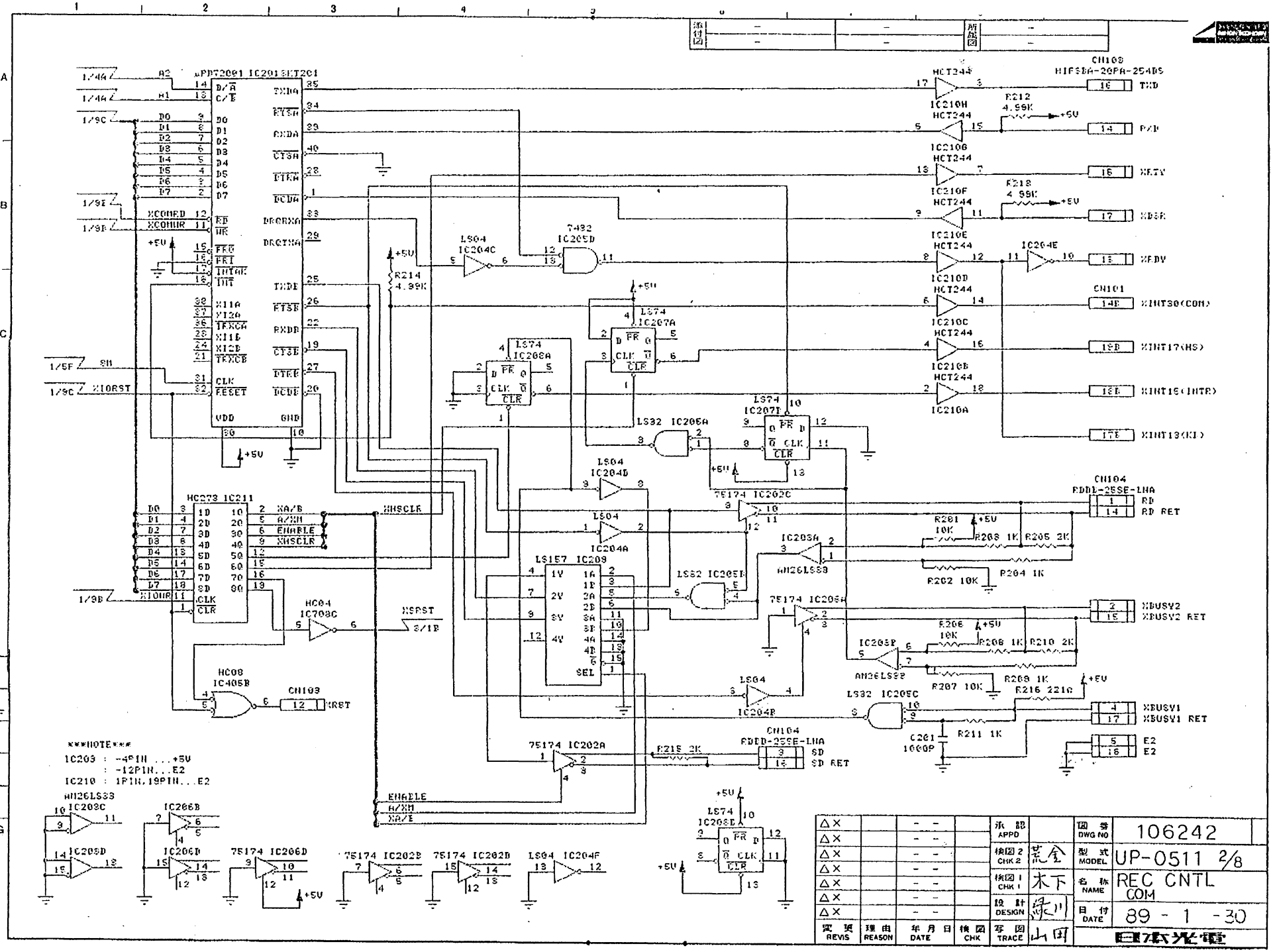
△×		– –		承認 APPD		図番 DWG NO	106239
△×		– –		検図2 CHK 2	荒金	型式 MODEL	UP-0464 19/19
△×		– –		検図1 CHK 1	木下	名称 NAME	AD POWER
△×		– –		設計 DESIGN	緑川	日付 DATE	89 - 1 - 30
△×		– –		写図 TRACE	山田		
変更 REVS	理由 REASON	年月日 DATE	検図 CHK				双葉電子



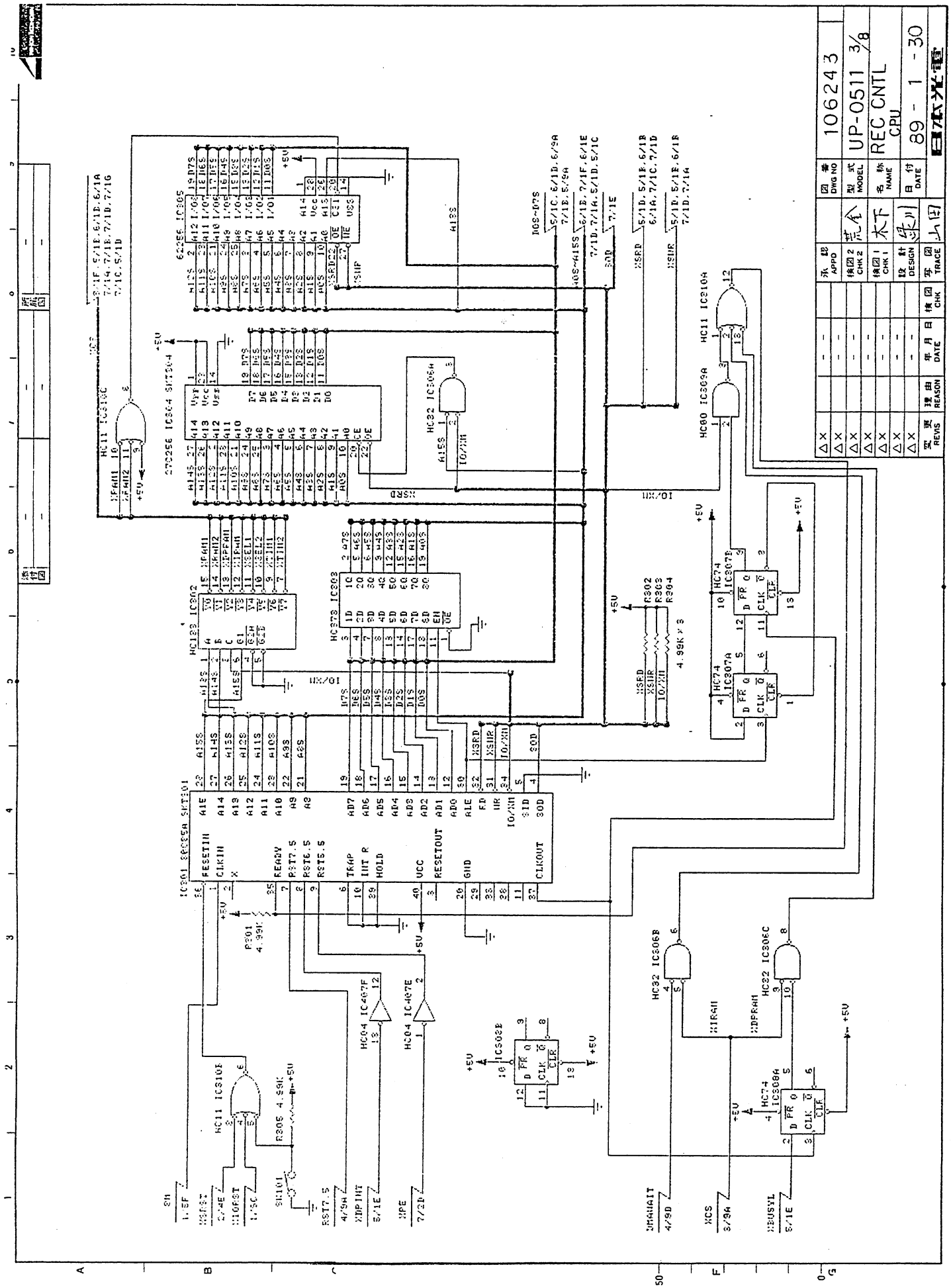
承認 APPD		図番 DWG NO	106240		
検図2 CHK 2		型式 MODEL	UP-0511		
検図1 CHK 1	木下	名称 NAME	REC CNTL BLOCK DIAGRAM		
設計 DESIGN		日付 DATE	89 · 1 · 30		
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE	山田

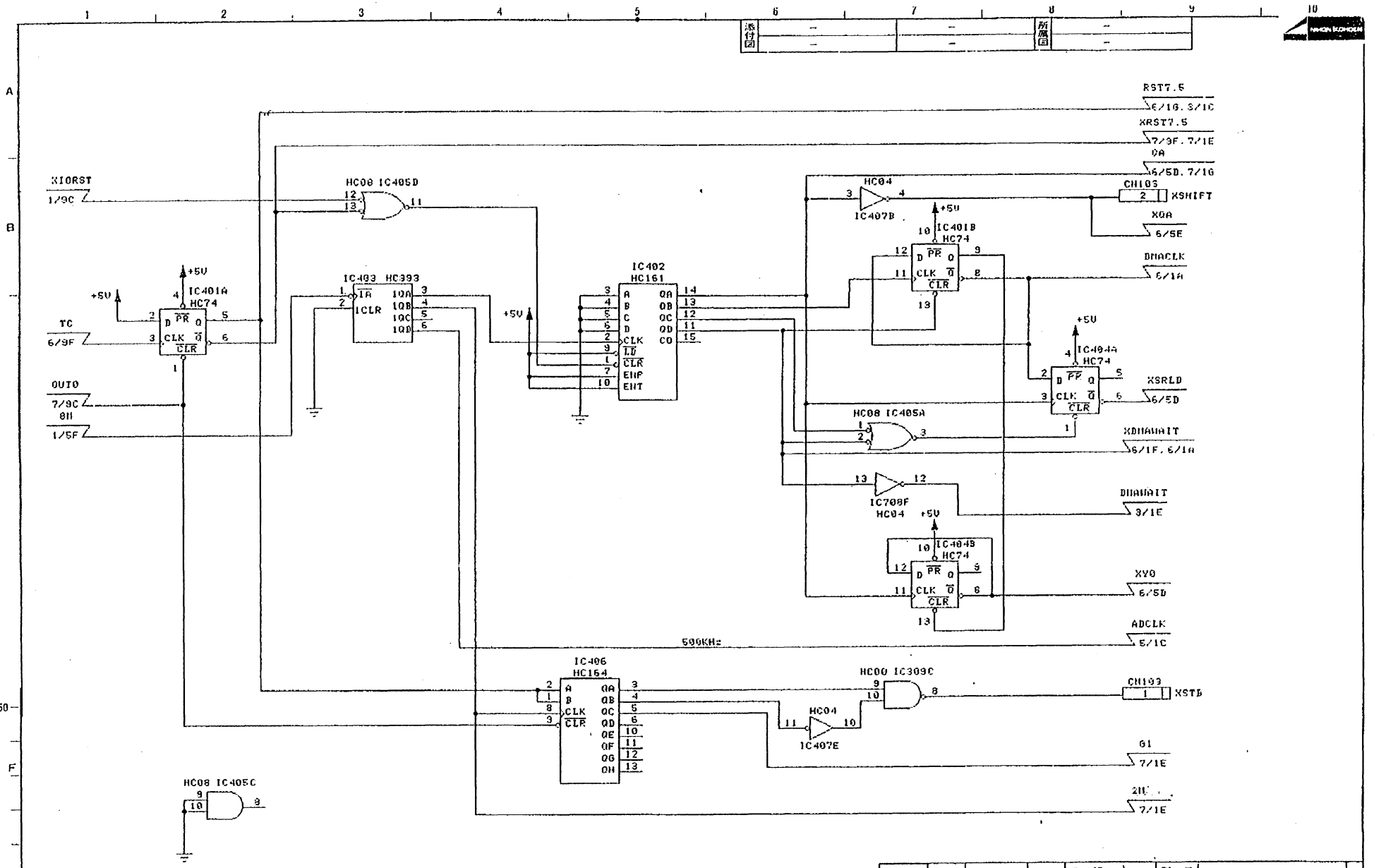


△×				承認 APPD	安田	図番 DWG NO	106241		
△×				検図2 CHK 2	芳谷	型式 MODEL	UP-0511 1/8		
△×				検図1 CHK 1	木下	名称 NAME	REC CNTL DECODER		
△×				設計 DESIGN	秋川	日付 DATE	89 - 1 - 30		
△×				製図 TRACE	山田		日本光電		
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK						



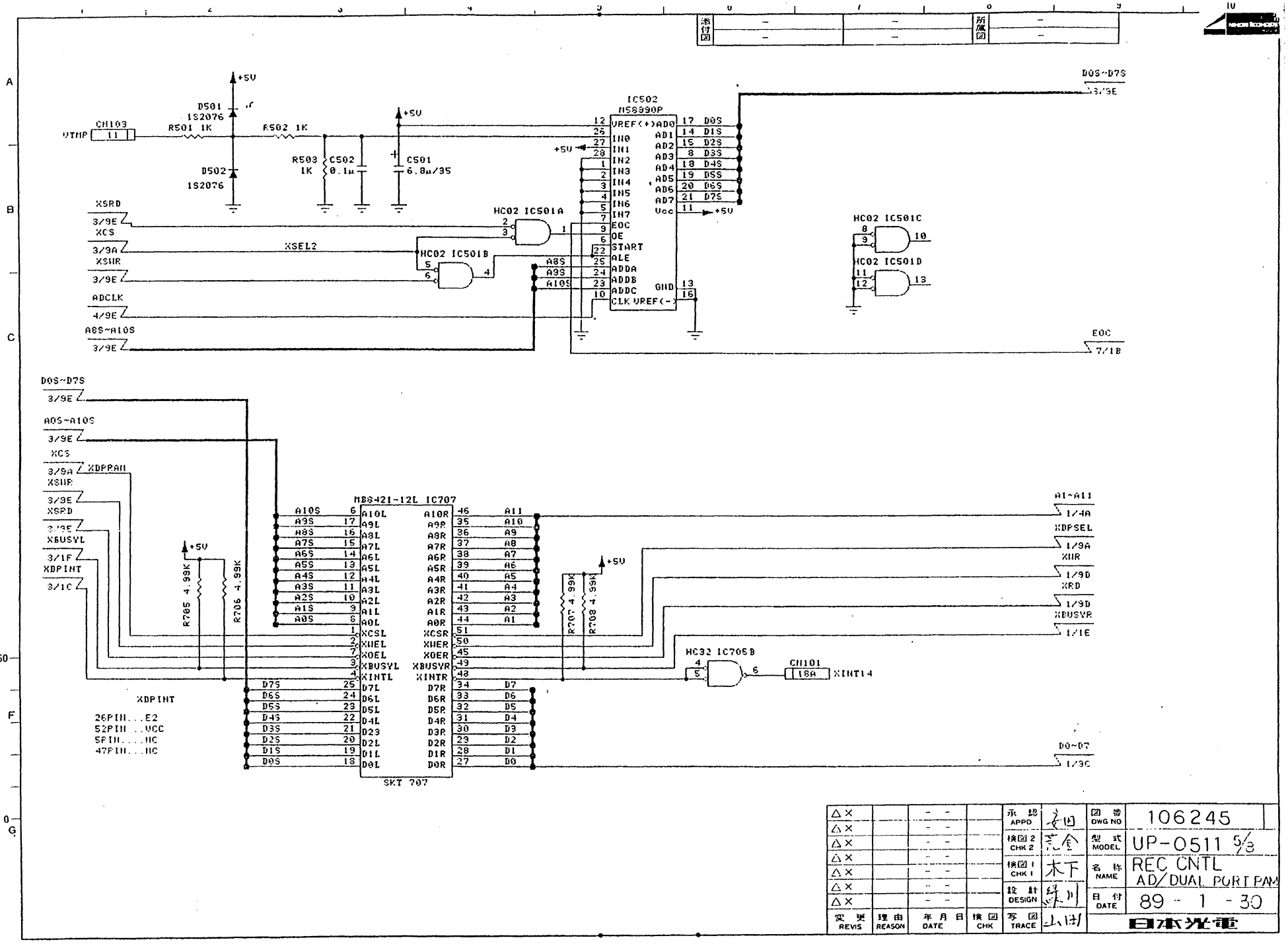
△X		- -		承認 APPD		図番 DWG NO	106242
△X		- -		検図2 CHK 2	芦倉	型式 MODEL	UP-0511 2/8
△X		- -		検図1 CHK 1	木下	名称 NAME	REC CNTL COM
△X		- -		設計 DESIGN	緑川	日付 DATE	89 - 1 -30
△X		- -		写図 TRACE	山田		
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK				日本光電


図番 DWG NO 106243
型式 MODEL UP-0511 3/8
名称 NAME REC CNTL CPU
日付 DATE 89 - 1 - 30
日本光電
IC301 8085A-2 CPU
IC302 HC138
IC303 HC373
IC304 HM6264 SRAM
IC305 62256
IC306 HC32
IC307 HC74
IC308 HC11
IC309 HC00
IC310 HC11
IC401 HC04
IC402 HC04
R301 4.99K
R302 R303 R304 4.99K × 3
R305 4.99K
SW101
+5V
RESETIN
CLKIN
READY
RST7.5
RST6.5
RST5.5
TRAP
INT R
HOLD
VCC
RESETOUT
GND
CLKOUT
ALE
RD
WR
IO/M
S1D
SOD
AD0~AD7
A8~A15
HIRAM
XDPRAM
XBUSYL
XMWAIT
XCS
XPE
XDPINT
XRESET
XSRD
XSWR
RST7.5
SOD
SID



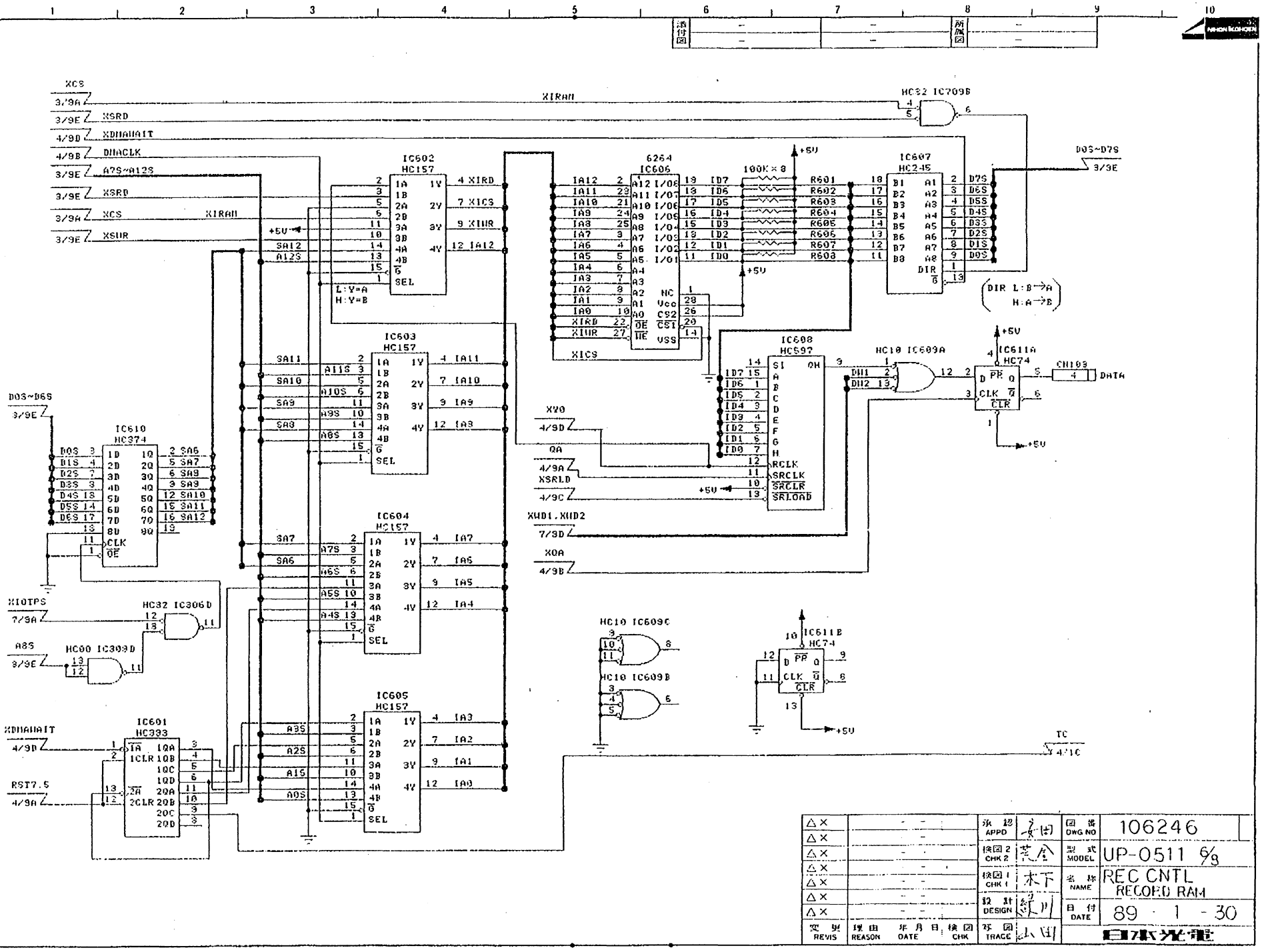
添付図	–	–	所属図	–
	–	–		–

変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	手図 TRACE	承認 APPD	図番 DWG NO	106244
△×		– –					
△×		– –					
△×		– –			検図2 CHK 2	型式 MODEL	UP-0511 4/8
△×		– –			検図1 CHK 1	名称 NAME	FEC CNTL TIMING
△×		– –			設計 DESIGN	日付 DATE	89 - 1 - 30
△×		– –					

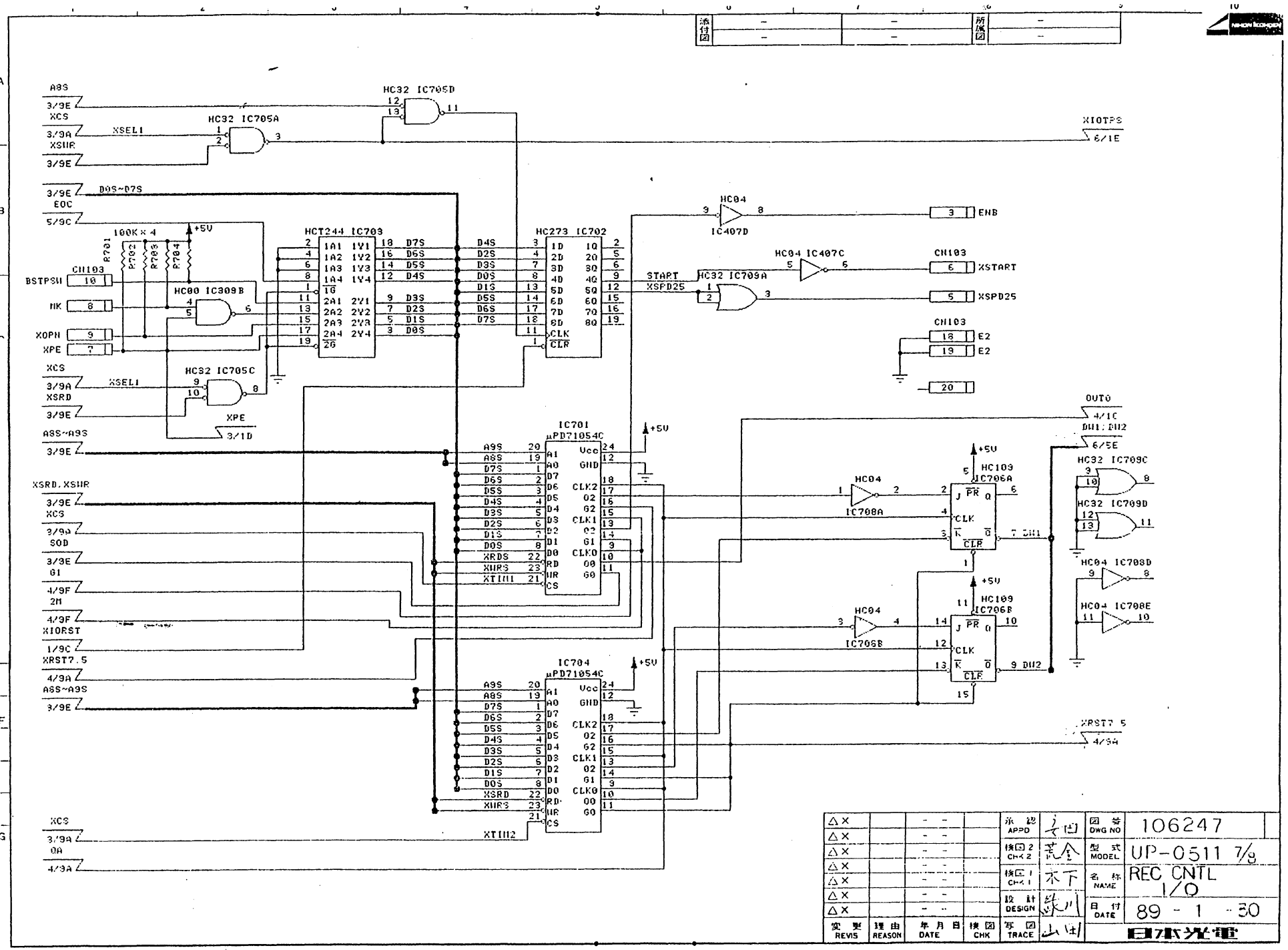


添付図	–	–	所属図	–
	–	–		–

変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE		
△×		– –		承認 APPD	安田	図番 DWG NO 106245
△×		– –		検図2 CHK 2	志倉	型式 MODEL UP-0511 5/8
△×		– –		検図1 CHK 1	木下	名称 NAME REC CNTL AD/DUAL PORT RAM
△×		– –		設計 DESIGN	緑川	日付 DATE 89 - 1 - 30
△×		– –		写図 TRACE	小川	日本光電
△×		– –				

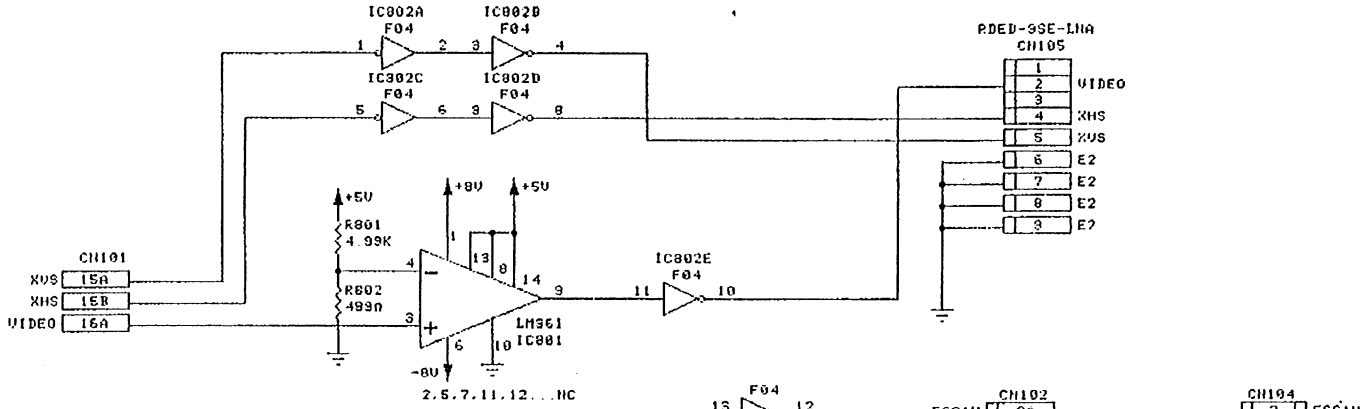


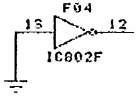
承認 APPD		図番 DWG NO	106246		
検図2 CHK 2	荒金	型式 MODEL	UP-0511 6/8		
検図1 CHK 1	木下	名称 NAME	REC CNTL RECORD RAM		
設計 DESIGN	紙川	日付 DATE	89 · 1 · 30		
作図 TRACE	山田	日本光電			
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK		

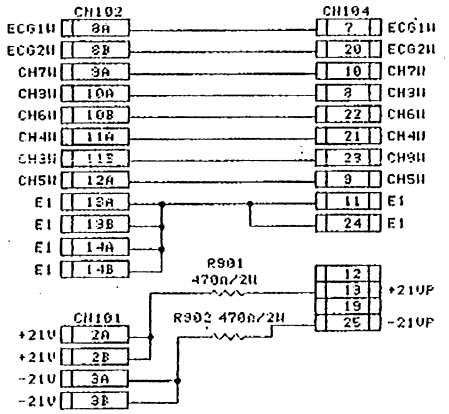


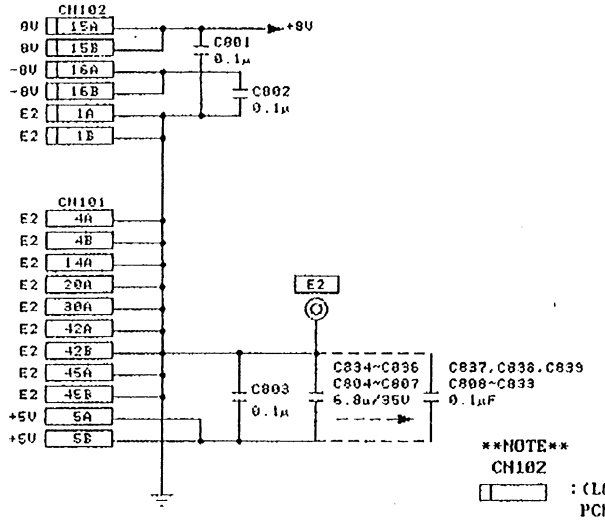
添付図	–	–	所属図	–					
	–	–		–					

△×		– –		承認 APPD	子田	図番 DWG NO	106247		
△×		– –		検図2 CHK 2	荒金	型式 MODEL	UP-0511 7/9		
△×		– –		検図1 CHK 1	木下	名称 NAME	REC CNTL I/O		
△×		– –		設計 DESIGN	鉄川	日付 DATE	89 - 1 - 30		
△×		– –							
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE	山村		日本光電		









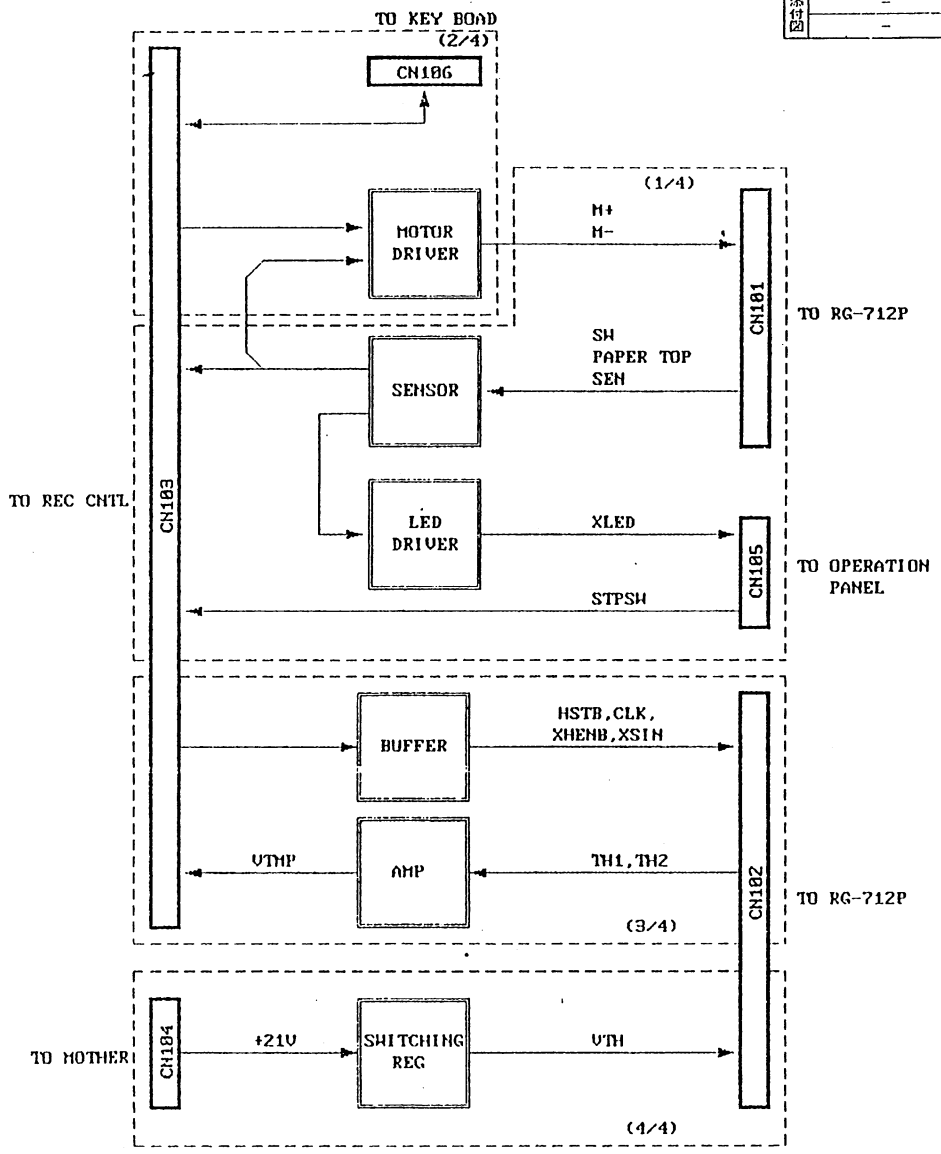
NOTE
CN102
: (LOCAL CONNECTOR)
PCN10EA-32P-2.54DS(105)

変更 REVIS	理由 REASON	年月日 DATE	検図 CHK
△×			
△×			
△×			
△×			
△×			
△×			
△×			

承認 APPD	
検図2 CHK 2	
検図1 CHK 1	木下
設計 DESIGN	鈴川
写図 TRACE	山辻

図番 DWG NO	106248
型式 MODEL	UP-0511 8/8
名称 NAME	REC CNTL HARD COPY 1/F
日付 DATE	99 - 1 - 30

日本光電



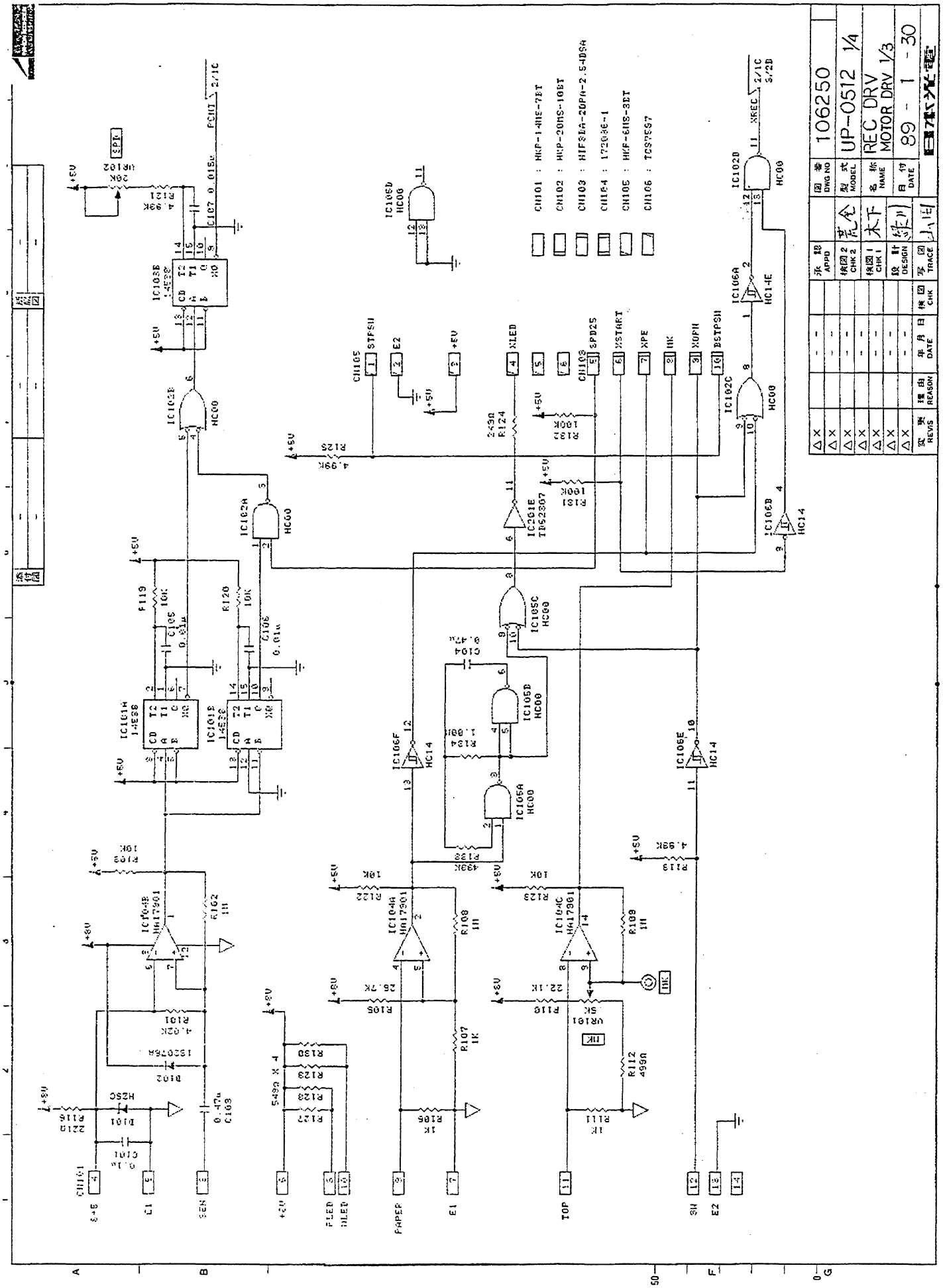
添付図	–	–	所属図	–
	–	–		–

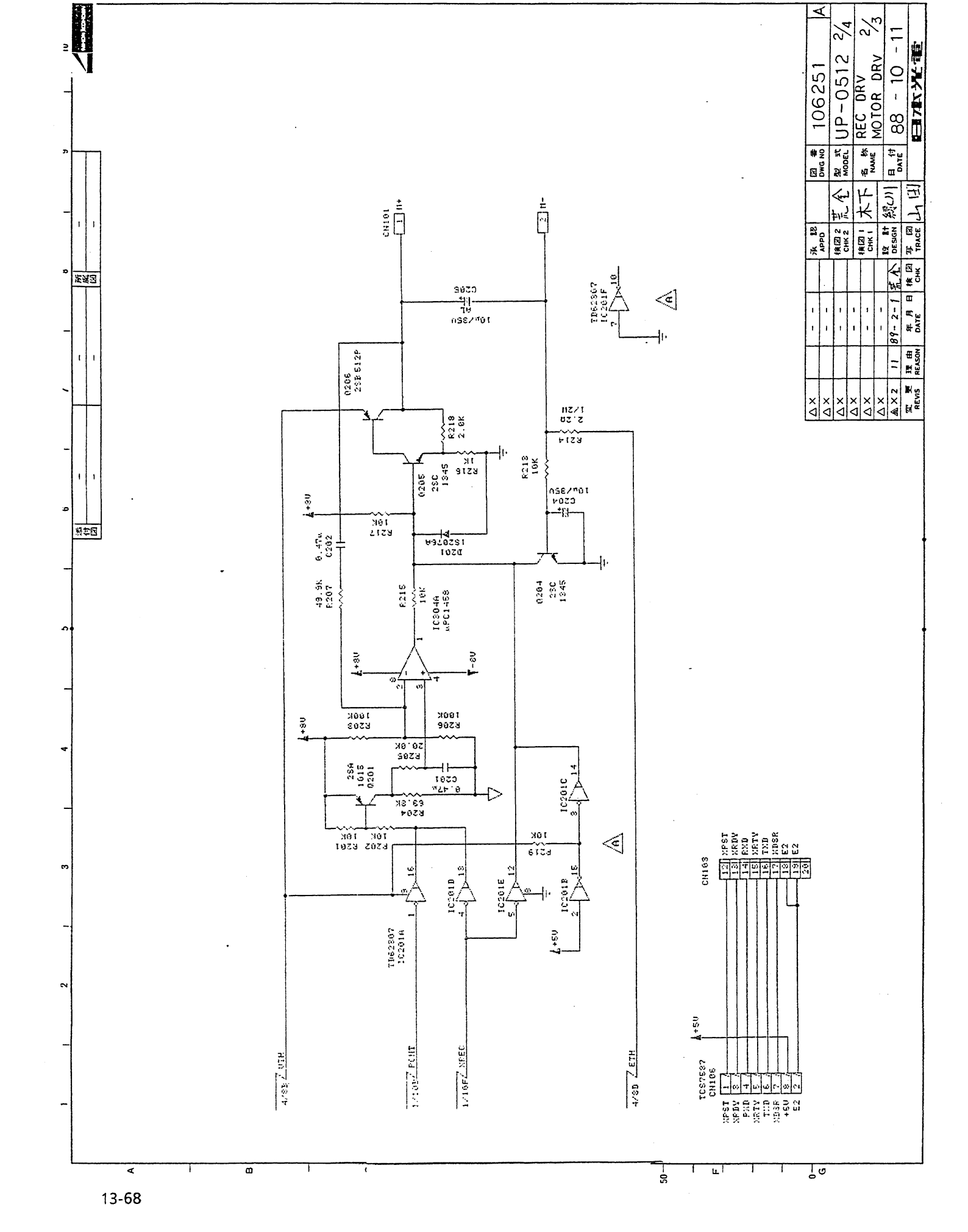
変更 REVS	理由 REASON	年月日 DATE	検図 CHK
△×	–	–	
△×	–	–	
△×	–	–	
△×	–	–	
△×	–	–	
△×	–	–	

承認 APPD	安田
検図2 CHK 2	荒金
検図1 CHK 1	木下
設計 DESIGN	梁川
写図 TRACE	山田

図番 DWG NO	106249
型式 MODEL	UP-0512
名称 NAME	REC DRV BLOCK DIAGRAM
日付 DATE	89 - 1 - 30

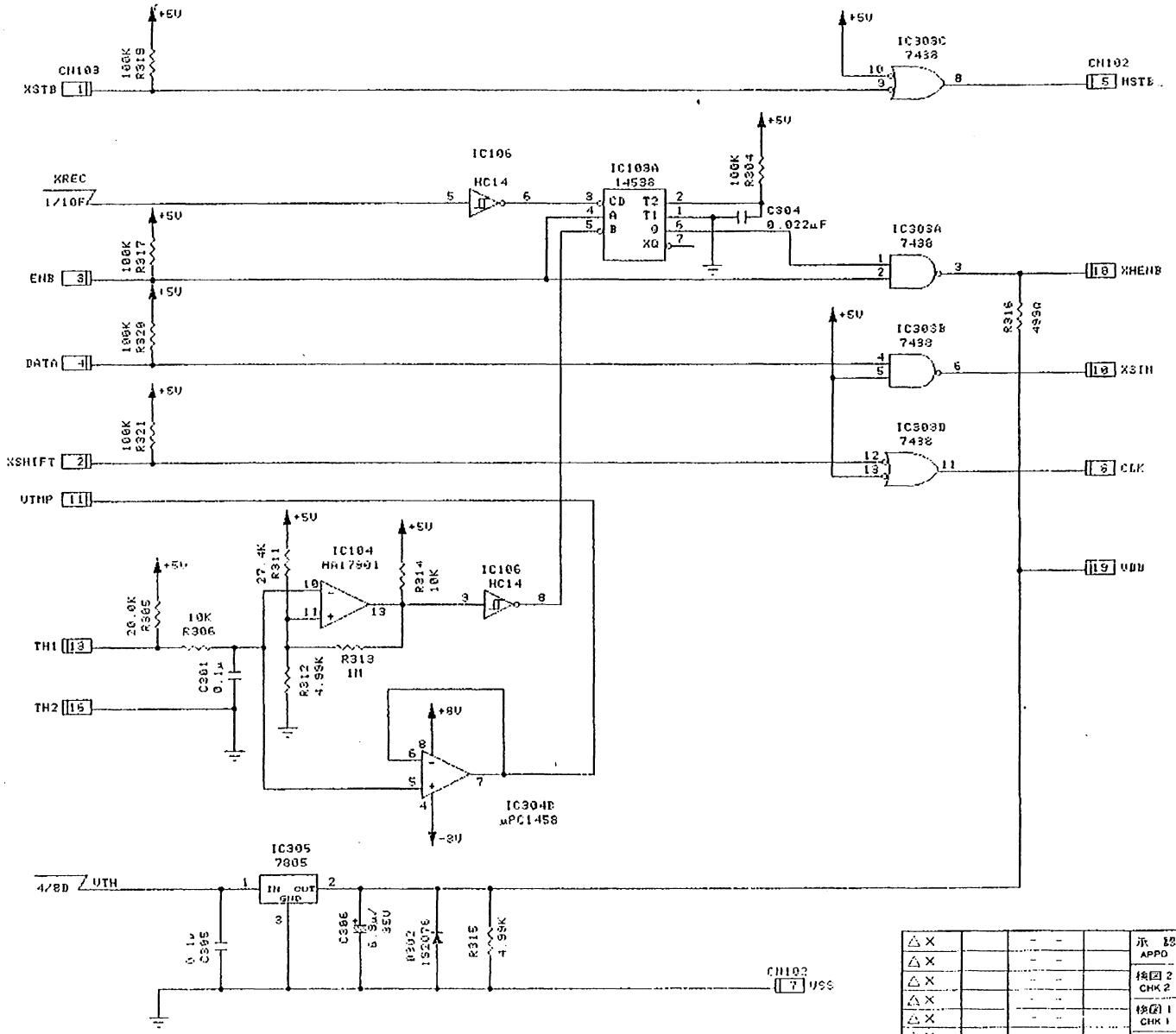
日本光電


106250
UP-0512 1/4
REC DRV
MOTOR DRV 1/3
89 - 1 - 30

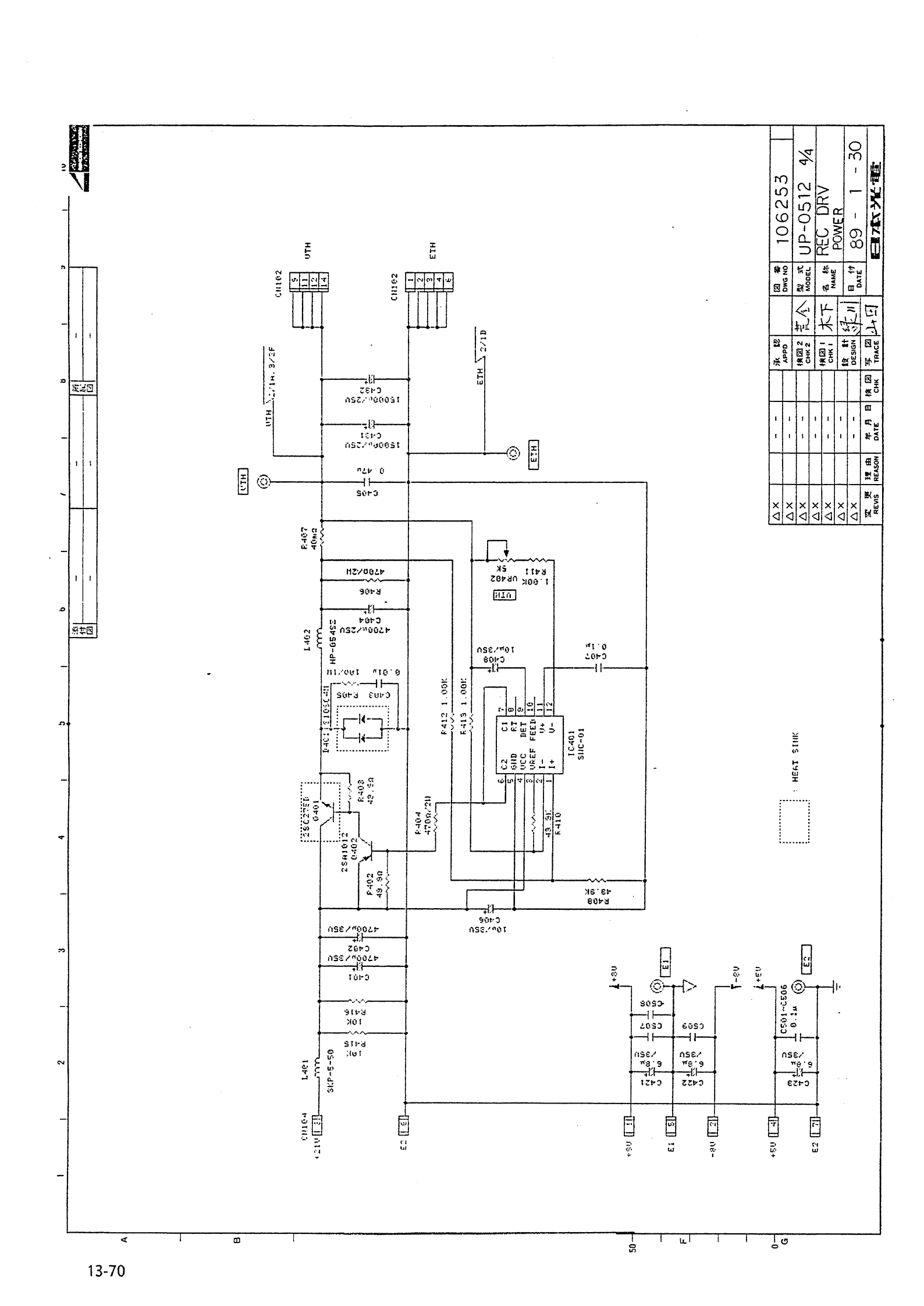


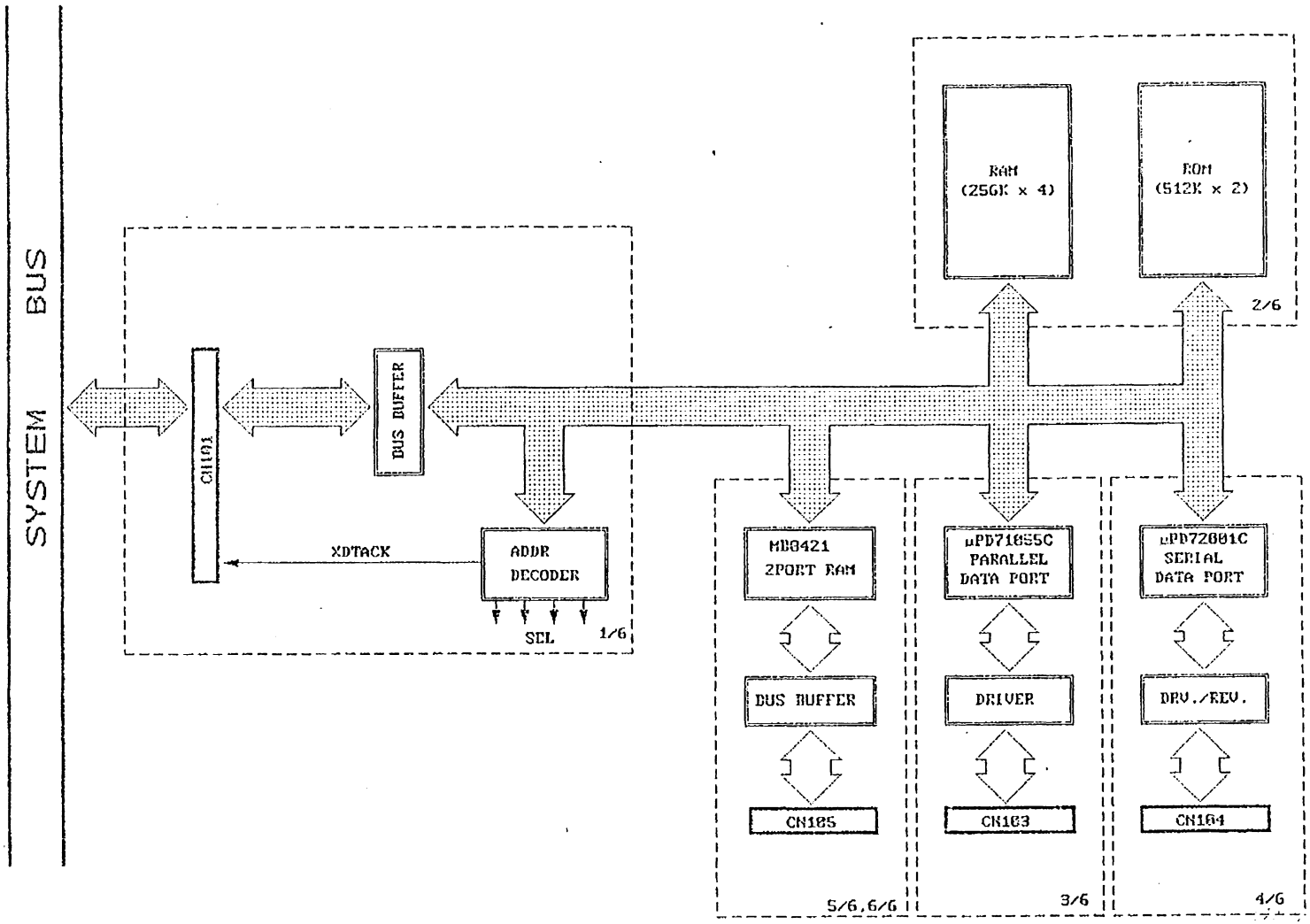
図番 DWG NO	106251	A
型式 MODEL	UP-0512	2/4
名称 NAME	REC DRV MOTOR DRV	2/3
日付 DATE	88 - 10 - 11	

REVIS	変更	REASON	理由	DATE	年月日	CHK	検図	TRACE	写図	DESIGN	設計	CHK 1	検図 1	CHK 2	検図 2	APPD	承認
△2		11		89-2-1		荒金		山田		綾川		木下		荒金			
△1																	
△1																	
△1																	
△1																	

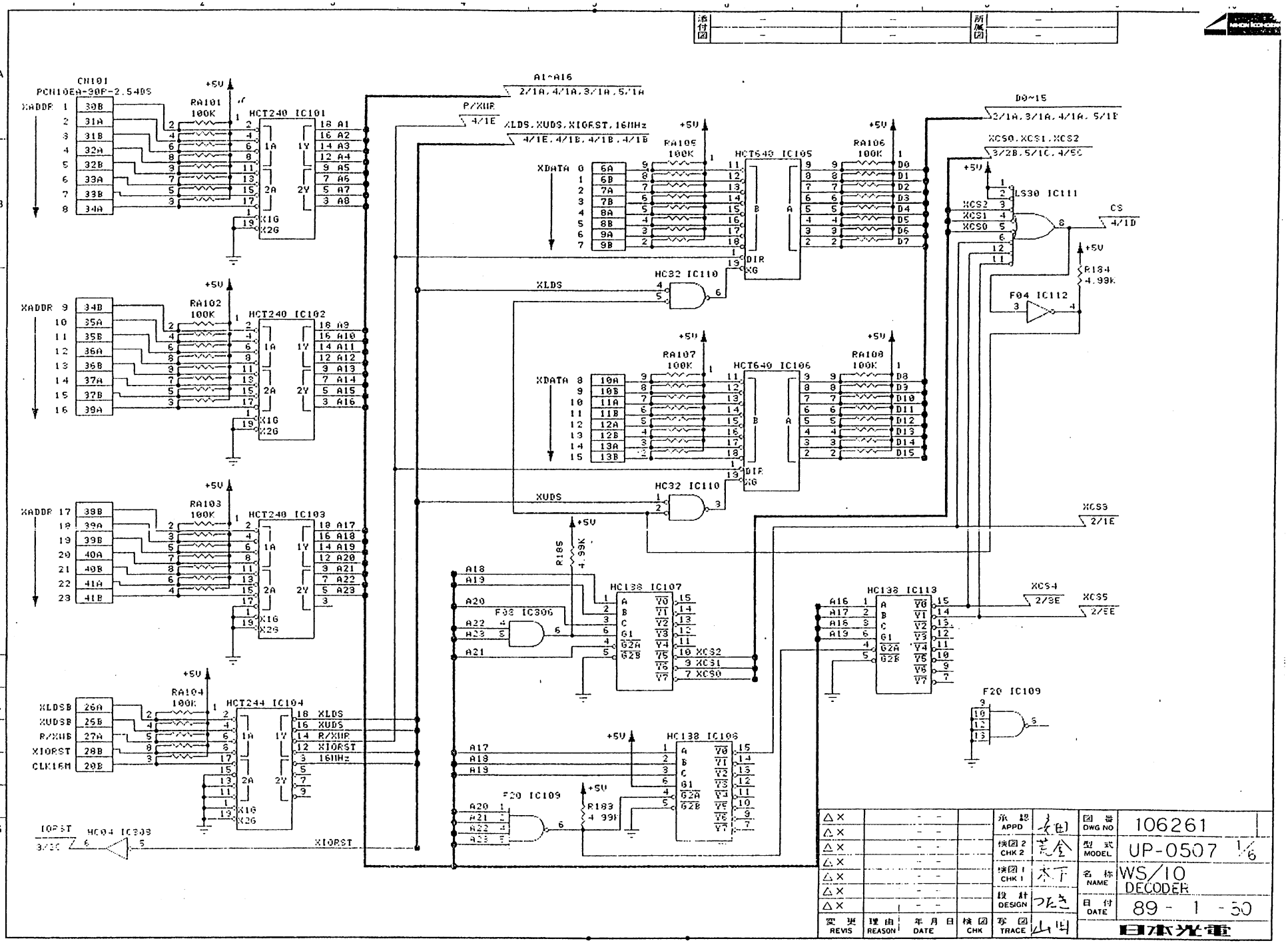


△×		– –		承認 APPD	吉田	図番 DWG NO	106252		
△×		– –		検図2 CHK 2	笠倉	型式 MODEL	UP-0512 3/4		
△×		– –		検図1 CHK 1	木下	名称 NAME	REC DRV MOTOR DRV 3/3		
△×		– –		設計 DESIGN	鈴川	日付 DATE	89 - 1 - 30		
△×		– –							
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE	山田	日本光電			


106253
UP-0512 4/4
REC DRV
POWER
89 - 1 - 30
UTH
ETH
HEAT SINK
IC401
SIIC-01
L402
HP-654S2
L401
SKP-5-50
2SC2712
2SA1612
UP402
1.00K
SK
R411
R412 1.00K
R413 1.00K
R404
470Ω/2W
R406
4700/2W
R407
40mΩ
R408
49.9K
R410
49.9K
R402
49.9Ω
R403
49.9Ω
R415
10K
R416
10K
C405
0.47u
C406
10u/35V
C407
0.1u
C408
10u/35V
C401
4700u/35V
C402
4700u/35V
C403
0.01u 100/1W
C404
4700u/25V
C421
6.8u /35V
C422
6.8u /35V
C423
6.8u /35V
C501-C506
0.1u
C505
C507
C509
CN102
CN104
+21V
+8V
E1
-8V
+5V
E2

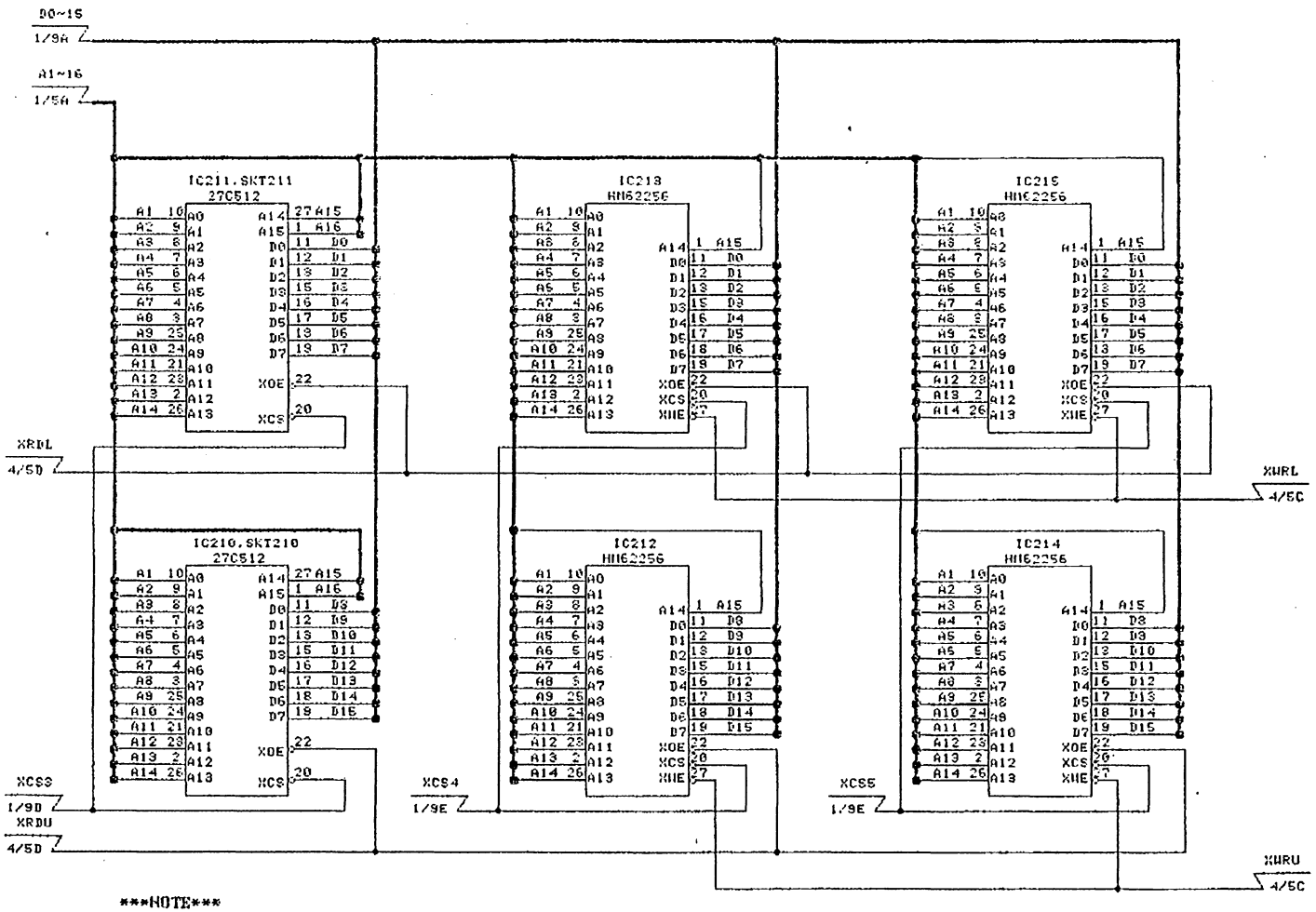


△×			- -		承認 APPD		図番 DWG NO	106260		
△×			- -		検図2 CHK 2	金	型式 MODEL	UP-0507		
△×			- -		検図1 CHK 1	木下	名称 NAME	WS/10 BLOCK DIAGRAM		
△×			- -		設計 DESIGN	つた	日付 DATE	89 - 1 - 30		
△×			- -		製図 TRACE	山田				
変更 REVIS	理由 REASON	年月日 DATE		検図 CHK				日本光電		



添付図	-	-	所属図	-			

△×				承認 APPD	青田	図番 DWG NO	106261
△×				検図2 CHK 2	荒金	型式 MODEL	UP-0507 1/6
△×				検図1 CHK 1	木下	名称 NAME	WS/10 DECODER
△×				設計 DESIGN	つたき	日付 DATE	89 - 1 - 30
△×				写図 TRACE	山田		
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK				日本光電



NOTE

IC210
211
212
213
214
215

14PIN...GND
28PIN...+5V

添付図	–	–	所属図	–
	–	–		–

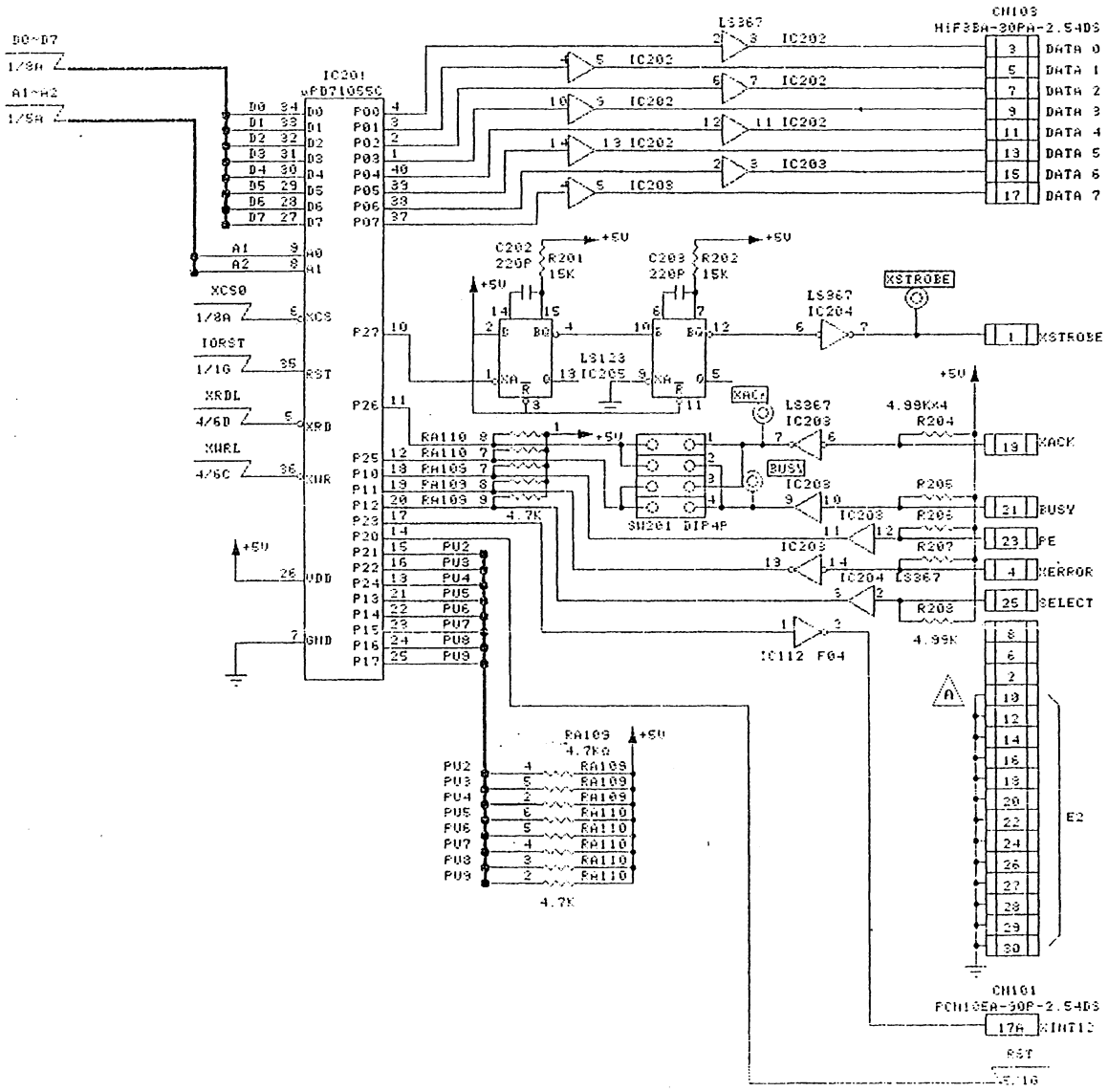
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK
△×		– –	
△×		– –	
△×		– –	
△×		– –	
△×		– –	
△×		– –	

承認 APPD	
検図2 CHK 2	荒金
検図1 CHK 1	木下
設計 DESIGN	つだ
写図 TRACE	山田

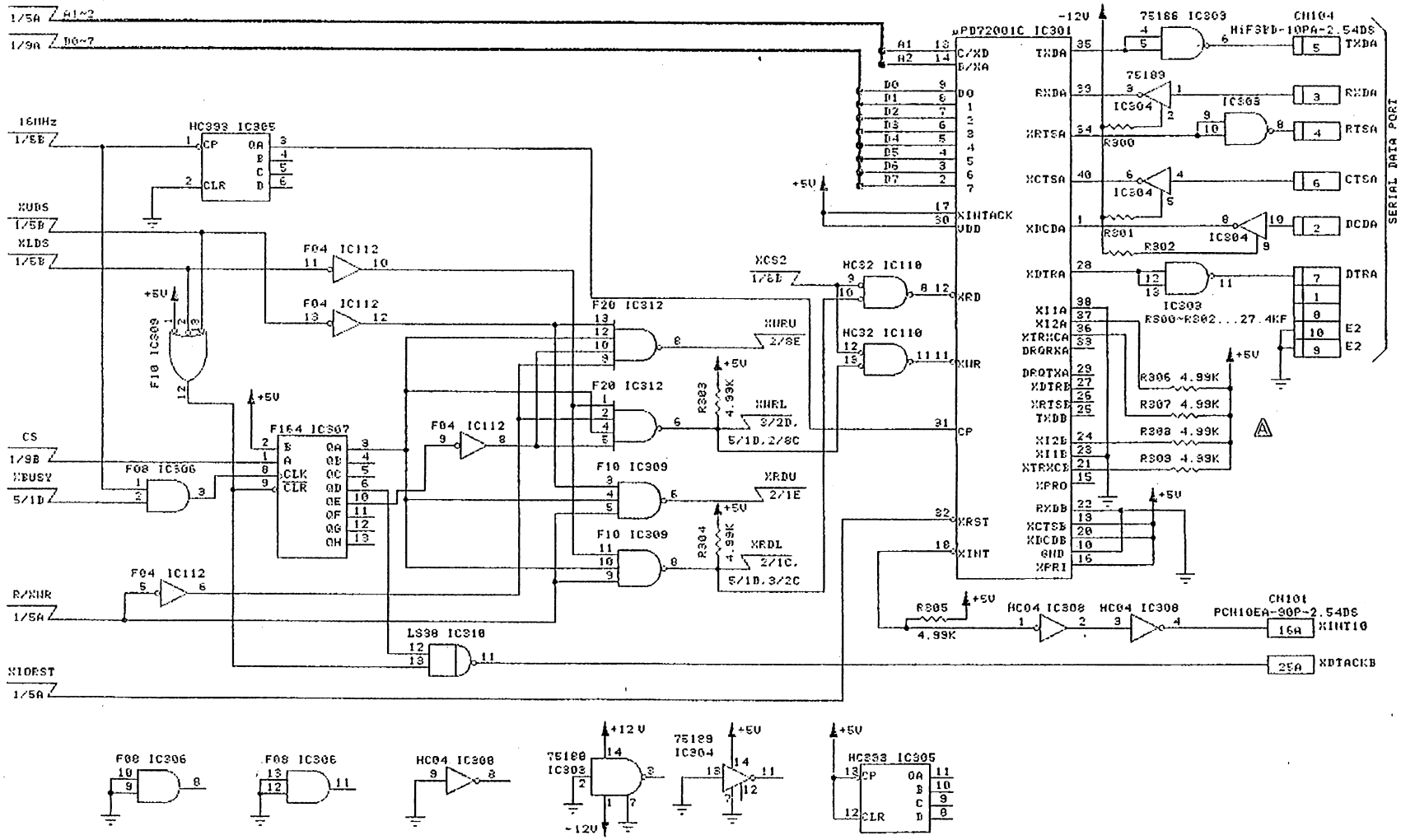
図番 DWG NO	106262
型式 MODEL	UP-0507 2/6
名称 NAME	WS/10 ROM/RAM
日付 DATE	89 - 1 - 30

日本光電

添付図	-	-	所属図	-	
	-	-		-	

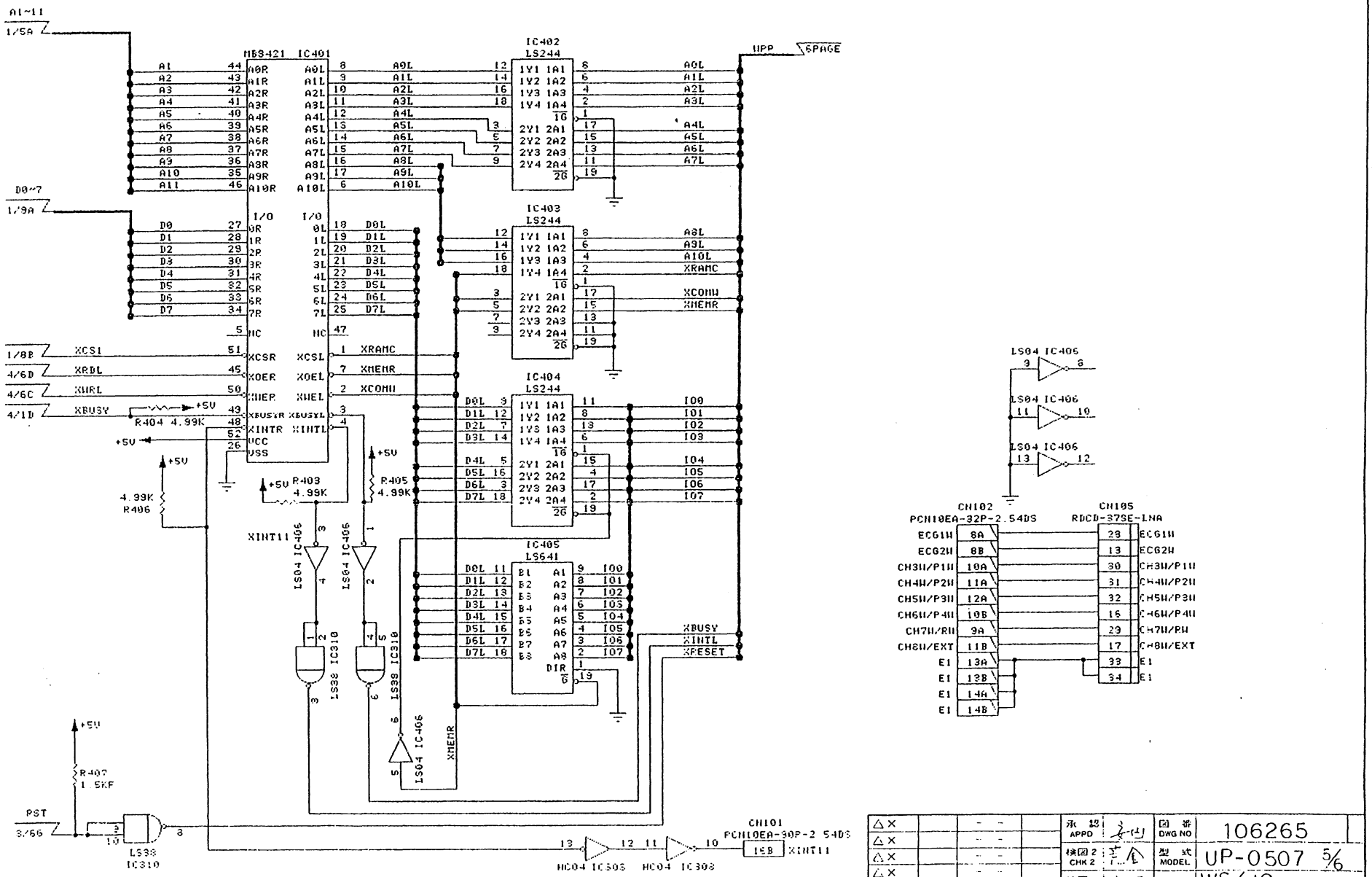


△×			- -		承認 APPD	安田	図番 DWG NO	106263	A
△×			- -		検図2 CHK 2	芦倉	型式 MODEL	UP-0507 3/6	
△×			- -		検図1 CHK 1	木下	名称 NAME	WS/10 PARA. PRINTER PCRT	
△×			- -		設計 DESIGN	つだき	日付 DATE	88 - 11 - 30	
△×			- -						
△×1	21	89-1-17	芦倉		写図 TRACE	山田		日本光電	
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK						

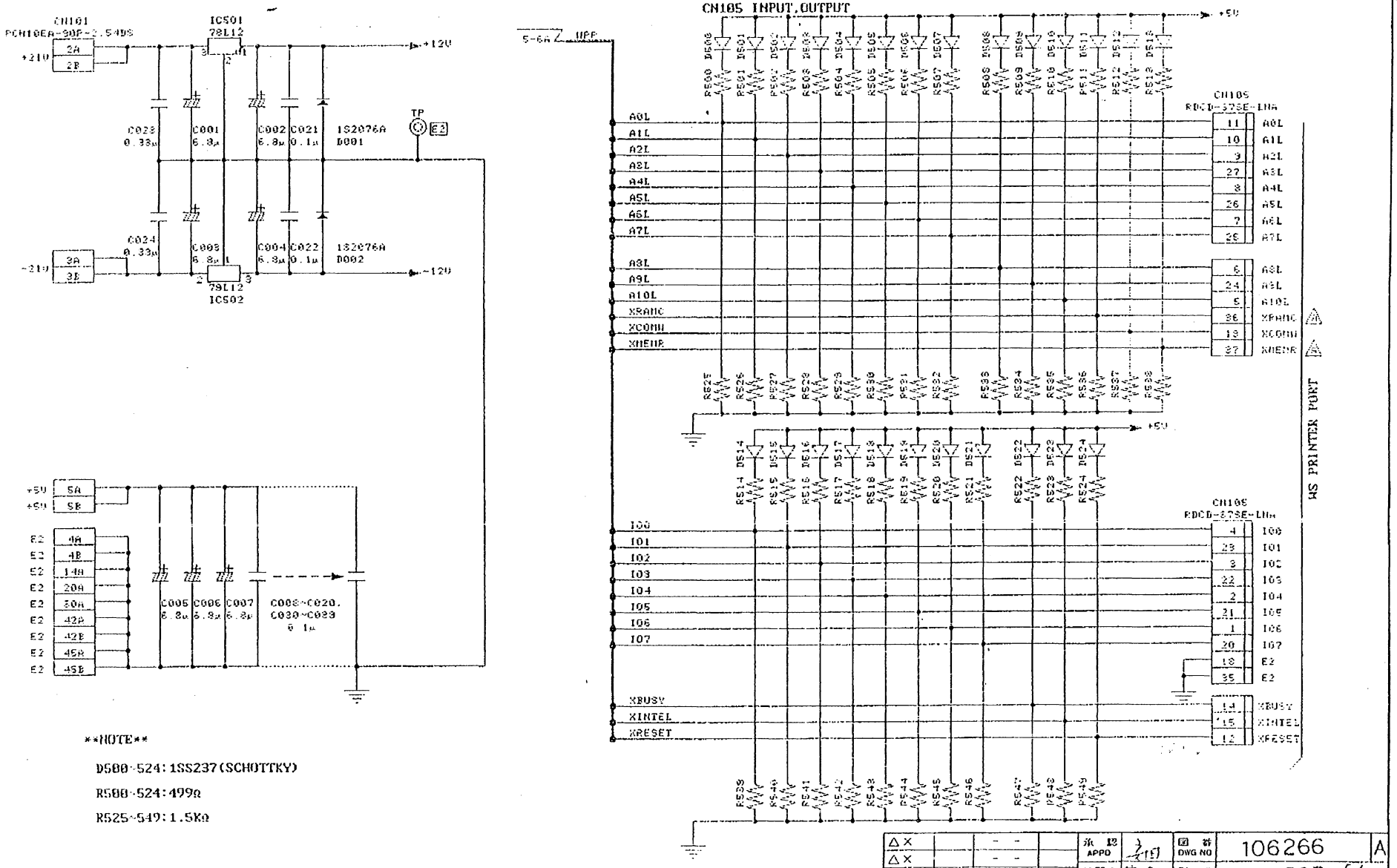


△X		- -		承認 APPD		図番 DWG NO	106264	A
△X		- -		検図2 CHK 2	荒金	型式 MODEL	UP-0507 4/6	
△X		- -		検図1 CHK 1	木下	名称 NAME	WS/IO SERIAL PORT	
△X		- -		設計 DESIGN	つた	日付 DATE	89 - 1 - 30	
△X		- -						
⚠X1	11	89-3-8	つた	写図 TRACE	山田	日本光電		
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK					

添付図	–	–	所属図	–
	–	–		–



REVIS	REASON	DATE	CHK				
△×		– –		承認 APPD	安田	図番 DWG NO	106265
△×		– –		検図2 CHK 2	芝金	型式 MODEL	UP-0507 5/6
△×		– –		検図1 CHK 1	木下	名称 NAME	WS/10 2 PORT RAM
△×		– –		設計 DESIGN	つたき	日付 DATE	89 - 1 - 30
△×		– –		写図 TRACE	山田		日本光電
変更	理由	年月日	検図				



NOTE

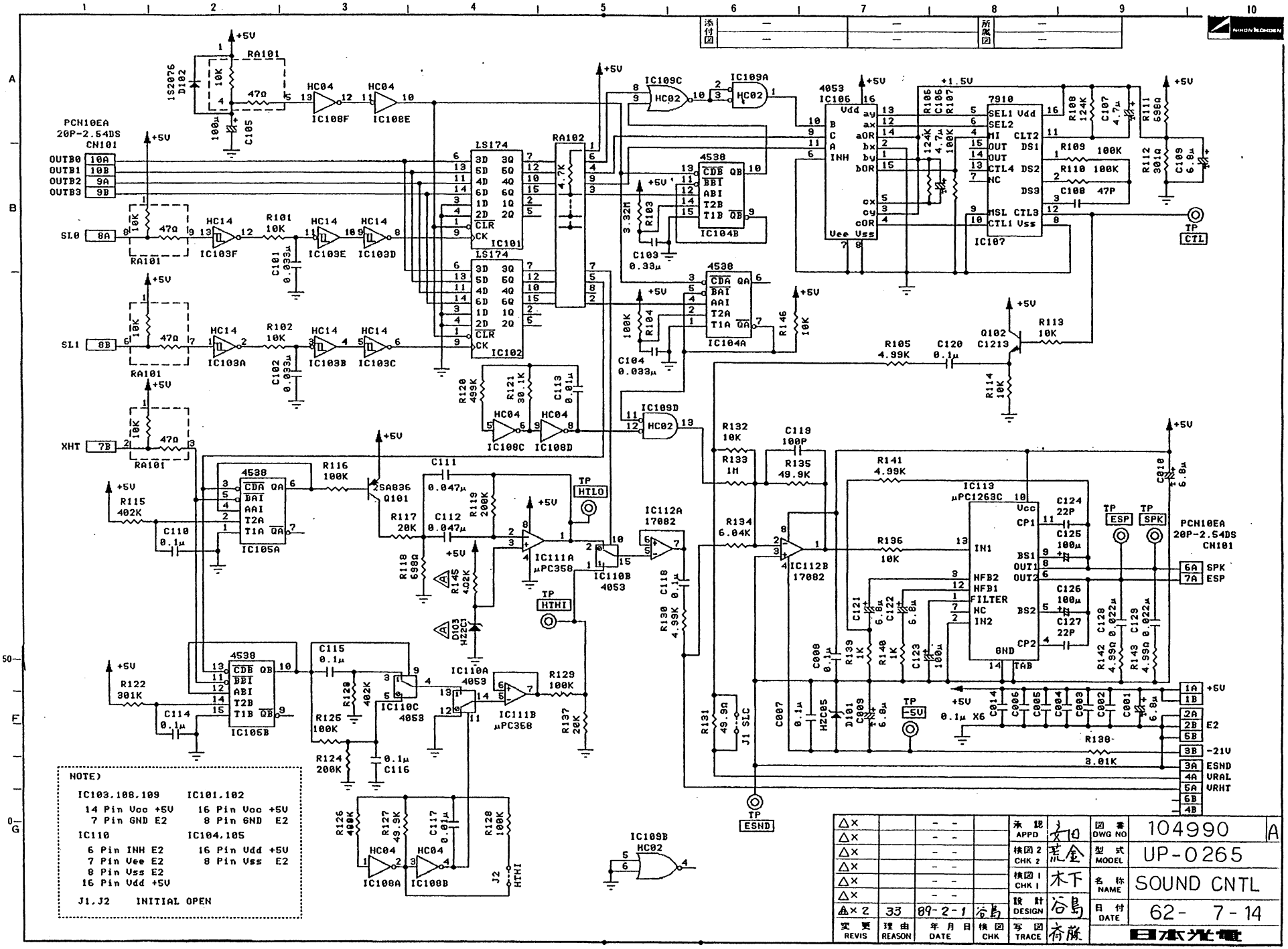
D500~524: 1SS237(SCHOTTKY)

R500~524: 499Ω

R525~549: 1.5KΩ

承認 APPD		図番 DWG NO	106266	A
検図2 CHK 2		型式 MODEL	UP-0507	6/6
検図1 CHK 1	木下	名称 NAME	WS/16 DUAL PORT RAM	
設計 DESIGN	つたき	日付 DATE	88 - 11 - 22	
写図 TRACE	山田	日本光電		

変更 REVIS	理由 REASON	年月日 DATE	検図 CHK
△×2	32	89-1-31	

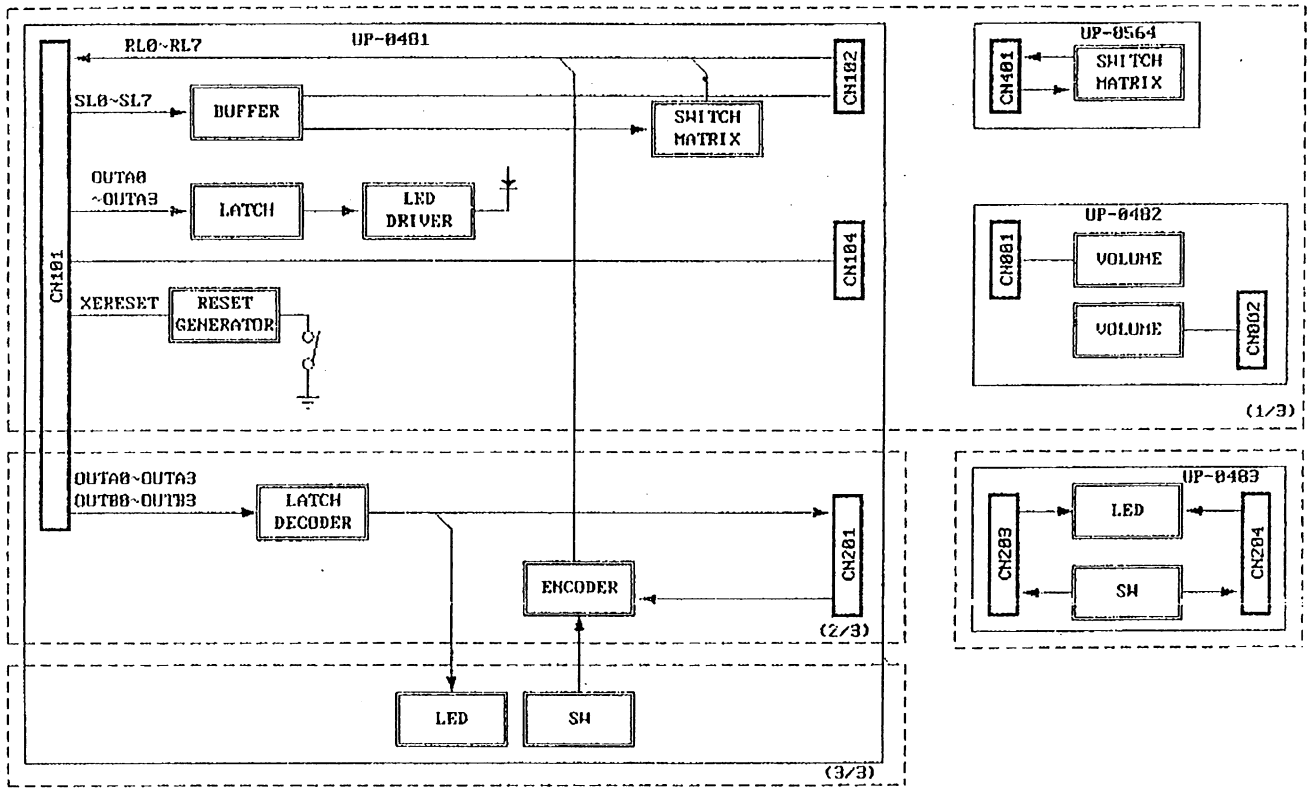


添付図	—	—	所属図	—
	—	—		—

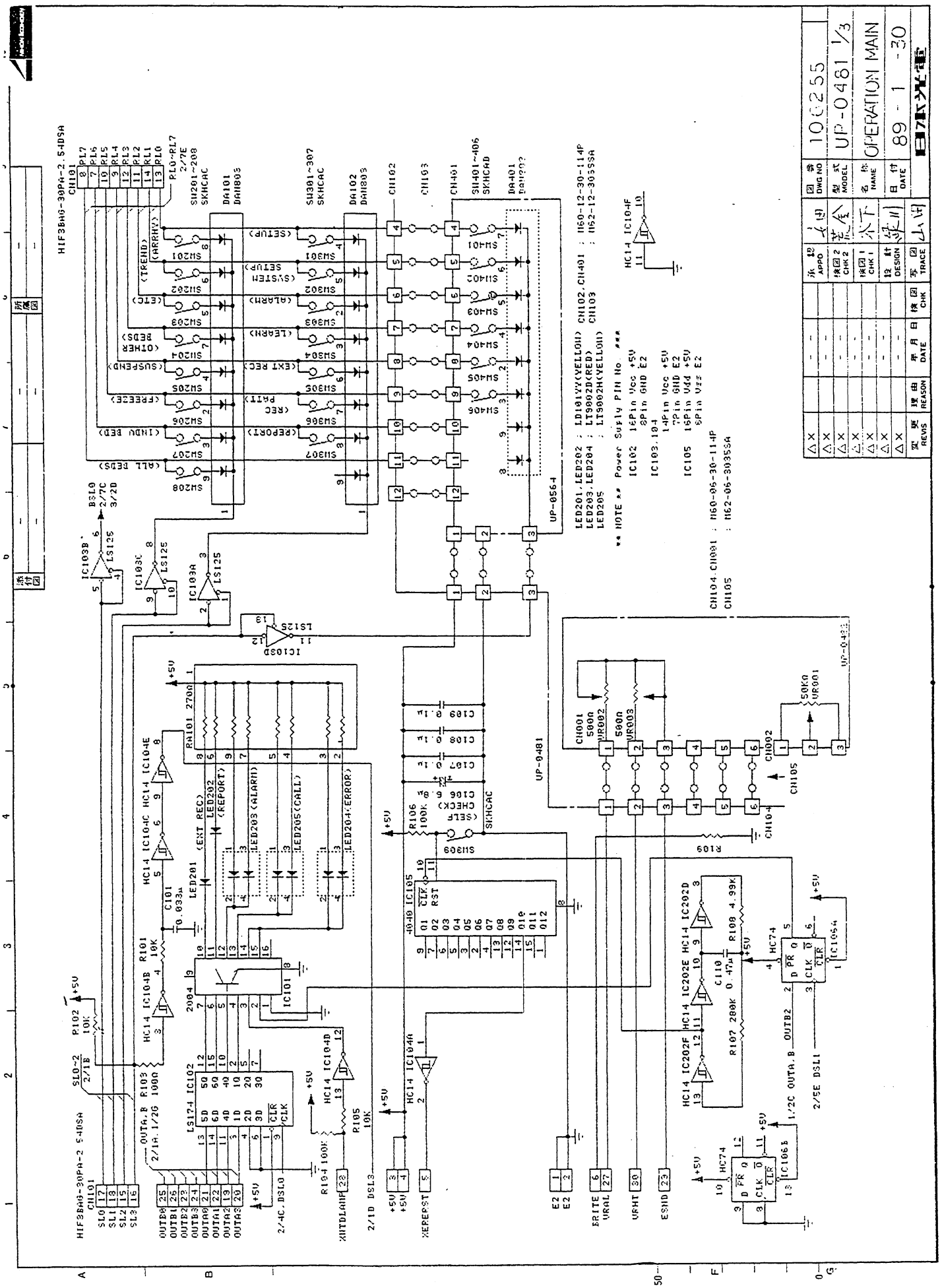
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK		
△×		- -		承認 APPD	高田
△×		- -		検図2 CHK 2	荒金
△×		- -		検図1 CHK 1	木下
△×		- -		設計 DESIGN	谷島
△×		- -		写図 TRACE	斉藤
△× 2	33	89-2-1	谷島		

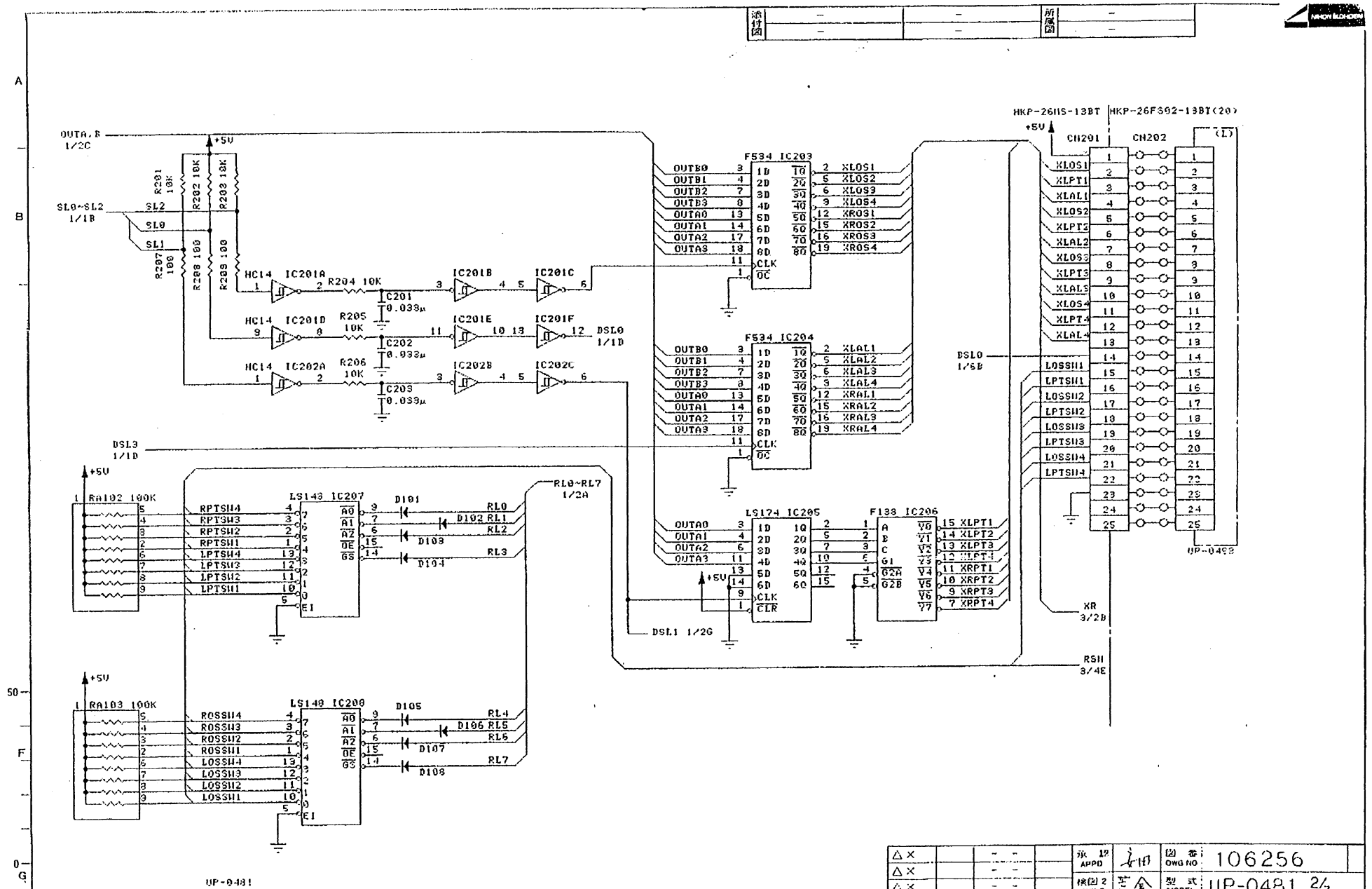
図番 DWG NO	104990 A
型式 MODEL	UP-0265
名称 NAME	SOUND CNTL
日付 DATE	62- 7-14

日本光電



				承認 APPD		図番 DWG NO	106254
				検図2 CHK 2		型式 MODEL	UP-0481
				検図1 CHK 1		名称 NAME	OPERATION MAIN BLOCK DIAGRAM
				設計 DESIGN		日付 DATE	89 - 1 - 30
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	写図 TRACE		日本光電	

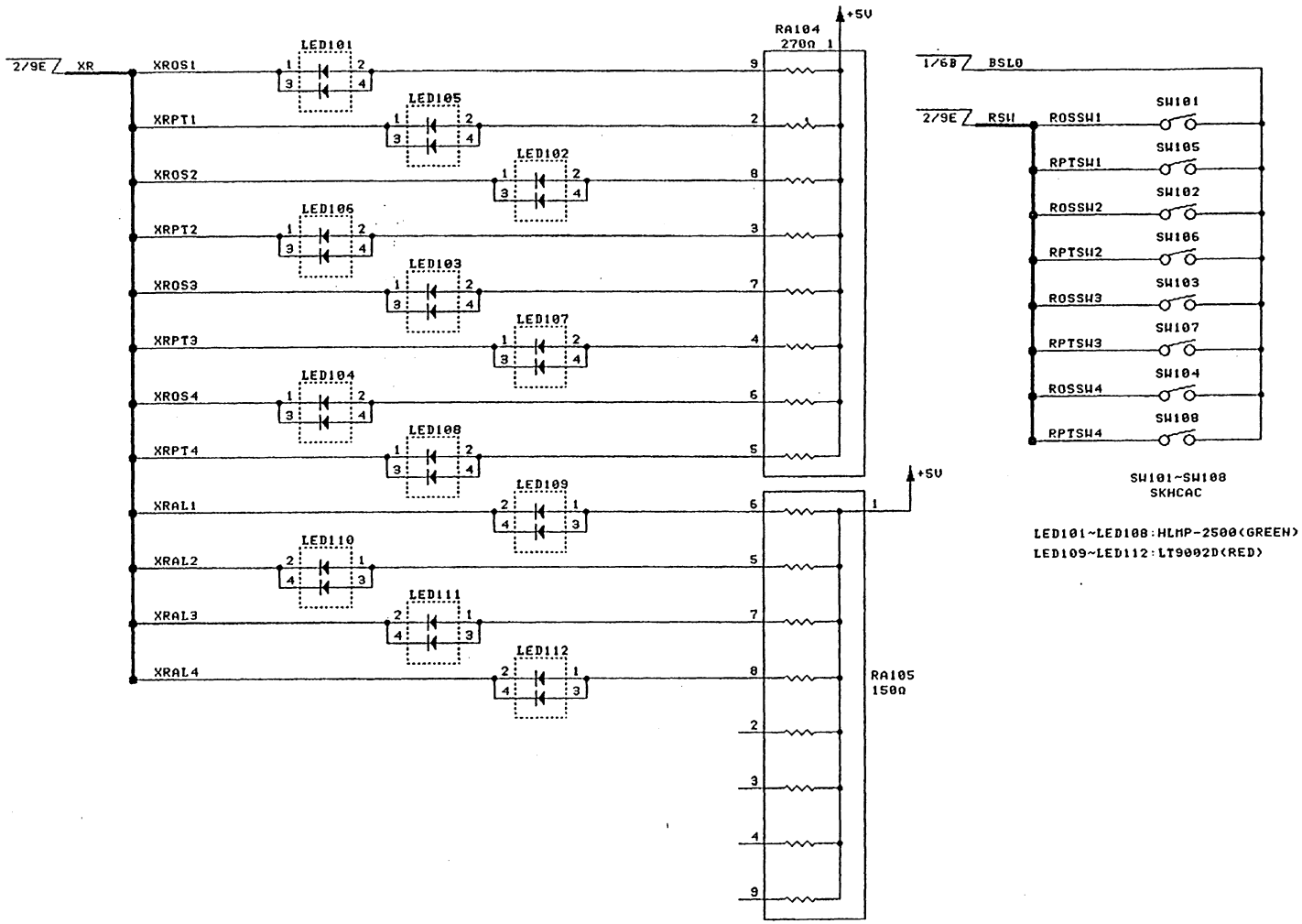

UP-0481 1/3
106255
OPERATION MAIN
89 - 1 - 30
UP-9481
UP-0564
SKHCAC
SKHCAD
LED201,LED202 ; LD101Y(YELLOW) CN102,CN401 ; N60-12-30-114P
LED203,LED204 ; LT9002D(RED) CN103 ; N62-12-303534
LED205 ; LT9002H(YELLOW)
** NOTE ** Power Supply PIN No. ***
IC102 16Pin Vcc +5V
8Pin GND E2
IC103,104 14Pin Vcc +5V
7Pin GND E2
IC105 16Pin Vdd +5V
8Pin Vss E2
CN104,CN001 ; N60-06-30-11-4P
CN105 ; N62-06-303534



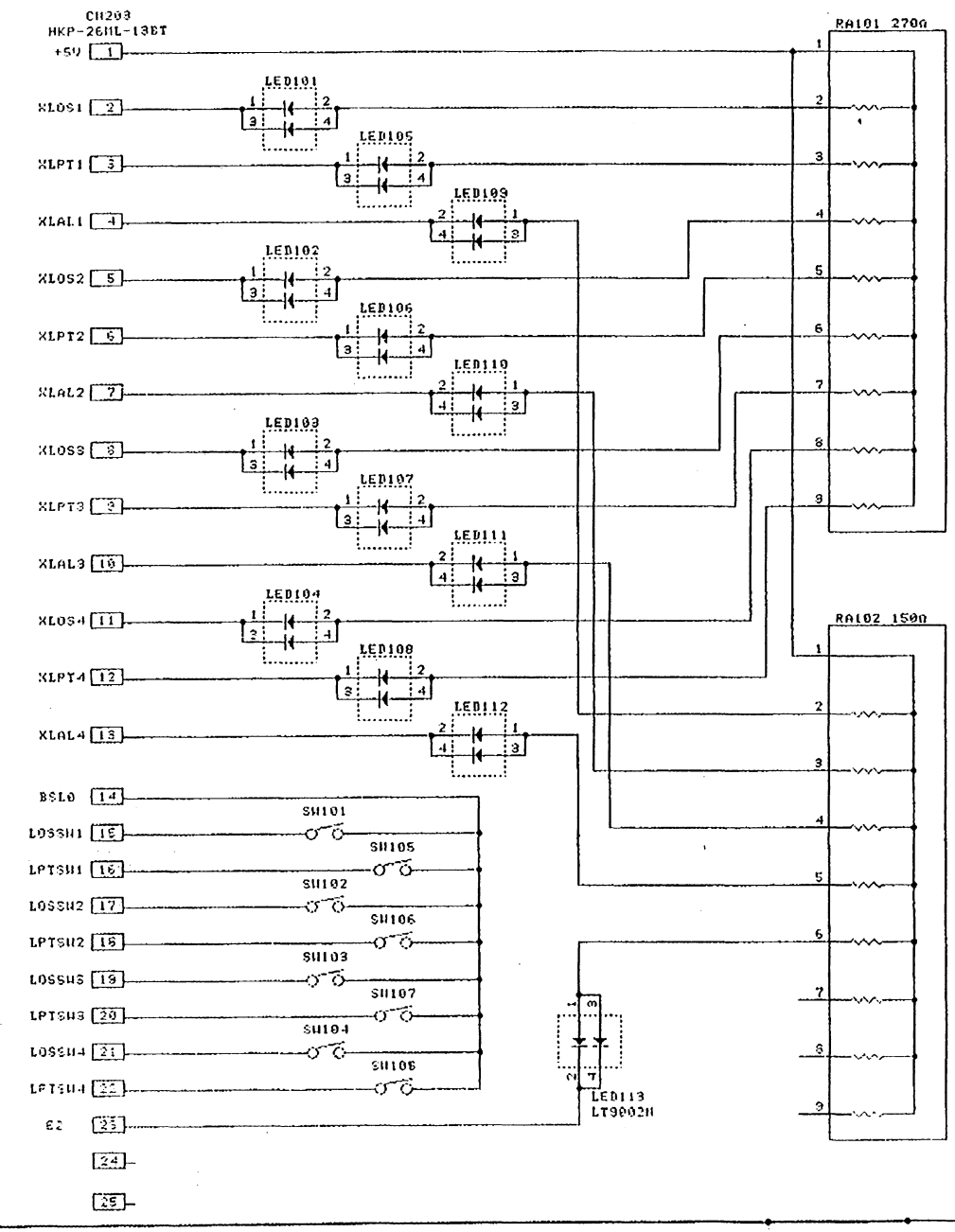
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK
△×		- -	
△×		- -	
△×		- -	
△×		- -	
△×		- -	
△×		- -	
△×		- -	

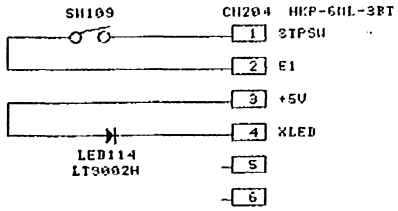
承認 APPD	永田	図番 DWG NO	106256
検図2 CHK 2	芝金	型式 MODEL	UP-0481 2/3
検図1 CHK 1	木下	名称 NAME	OPERATION MAIN
設計 DESIGN	塚川	日付 DATE	89 - 1 - 30
写図 TRACE	山内		日本光電

添付図	–	–	所属図	–
	–	–		–



△×		– –		承認 APPD	安田	図番 DWG NO	106257	
△×		– –		検図2 CHK 2	荒金	型式 MODEL	UP-0481	3/3
△×		– –		検図1 CHK 1	木下	名称 NAME	OPERATION MAIN	
△×		– –		設計 DESIGN	緑川	日付 DATE	89 - 1 - 30	
△×		– –		写図 TRACE	山田			
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK			日本光電		





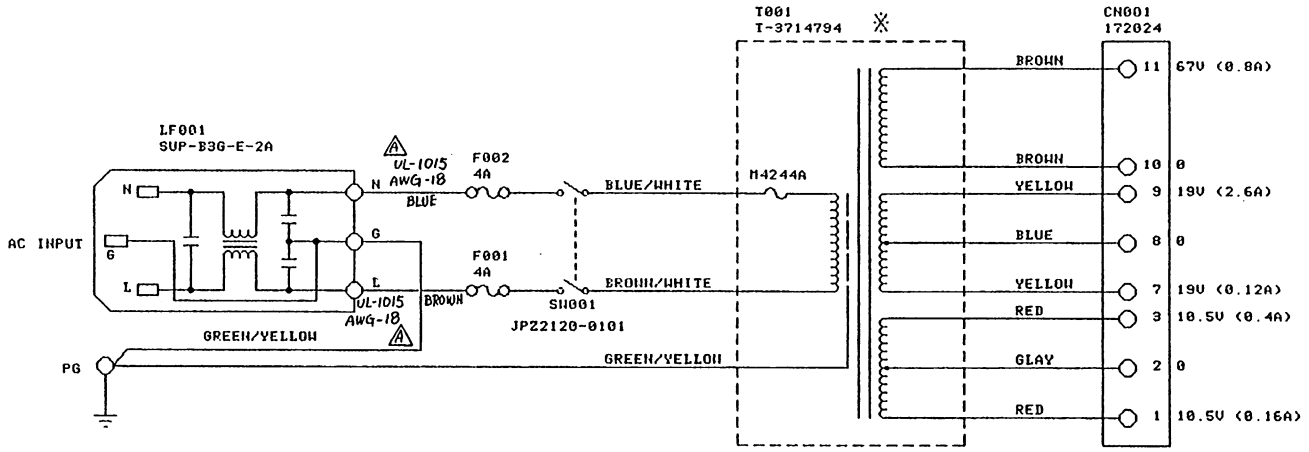
SW101~SW109:SKHC4C
LED101~LED108:HLMP-2500(GREEN)
LED109~LED112:LT9002D(RED)
LED101~LED112:LED114
LED113:LT9002H(GREEN)
LED114:LT9002H(YELLOW)

変更 REVIS	理由 REASON	年月日 DATE	検図 CHK	承認 APPD	検図2 CHK 2	検図1 CHK 1	設計 DESIGN	写図 TRACE
△×		- -						
△×		- -						
△×		- -						
△×		- -						
△×		- -						
△×		- -						
△×		- -						

図番 DWG NO	106258
型式 MODEL	UP-0483
名称 NAME	OPERATION LEFT
日付 DATE	89 - 1 - 30

日本光電

添付図	—	—	所属図	—
	—	—		—



※ NOTE SC-001RA
T001 T-3714802

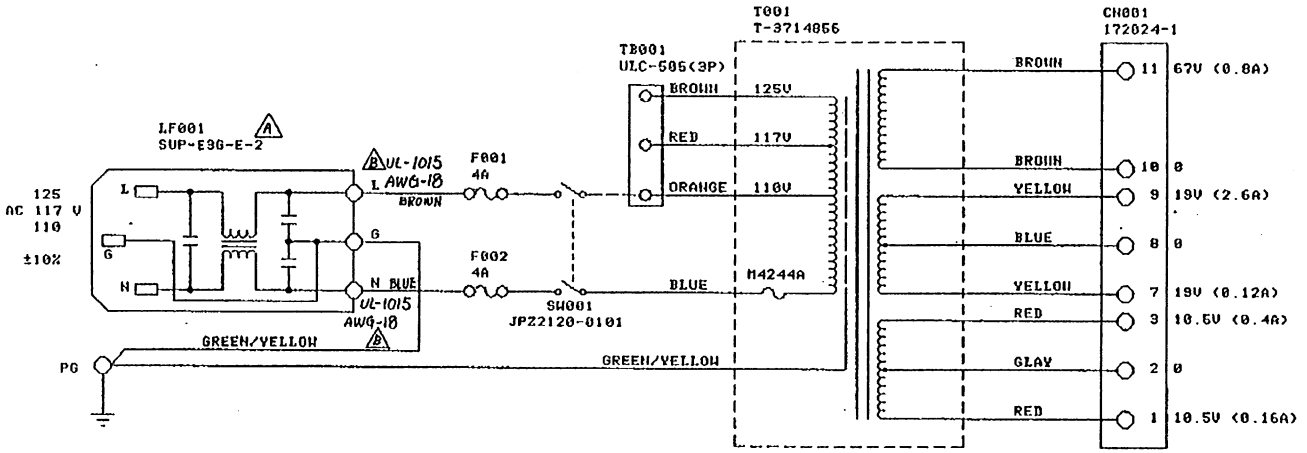
3

REVIS	REASON	DATE	CHK	TRACE
△×		- -		
△×		- -		
△×		- -		
△×		- -		
△×		- -		
△×		- -		
⚠× 2	22	89-1-17	志仏	〃

承認 APPD	安田
検図 2 CHK 2	荒金
検図 1 CHK 1	古島
設計 DESIGN	渡川
写図 TRACE	〃
図番 DWG NO	105598 A
型式 MODEL	SC-001R/SC-001RA
名称 NAME	TRANS UNIT
日付 DATE	62-10-11

日本光電

添付図	—	—	所属図	—
	—	—		—



REVIS	REASON	DATE	CHK	TRACE
△×		— —		
△×		— —		
△×		— —		
△×		— —		
△×		— —		
⚠× 2	22	89-1-17	荒金	
⚠× 1	25	63-7-19	荒金	

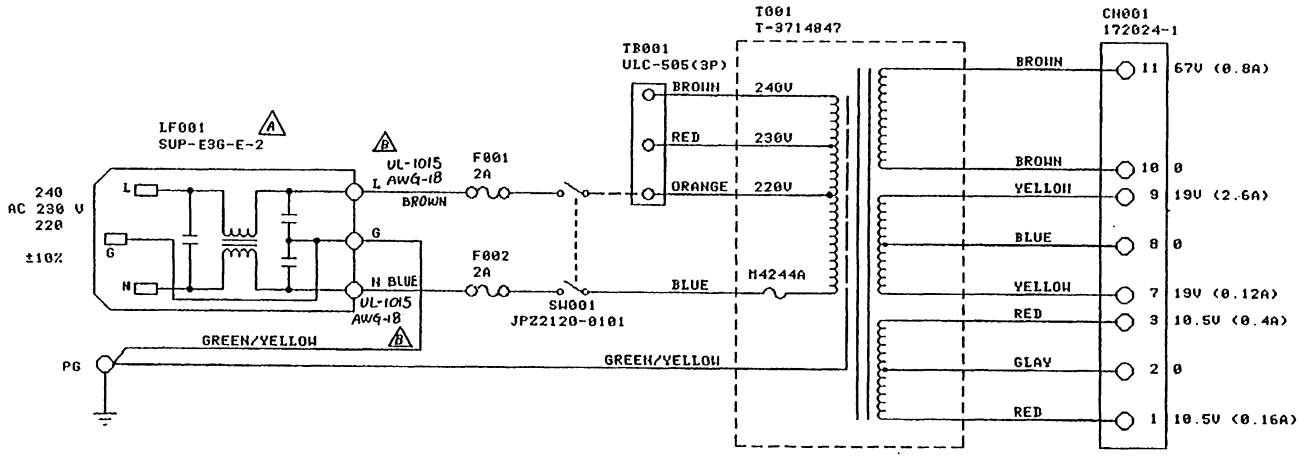
承認 APPD	本田
検図 2 CHK 2	荒金
検図 1 CHK 1	谷島
設計 DESIGN	緑川
写図 TRACE	斉藤

図番 DWG NO	105811 B
型式 MODEL	SC-801RJ
名称 NAME	TRANS UNIT
日付 DATE	62 - 12 - 11

日本光電

3

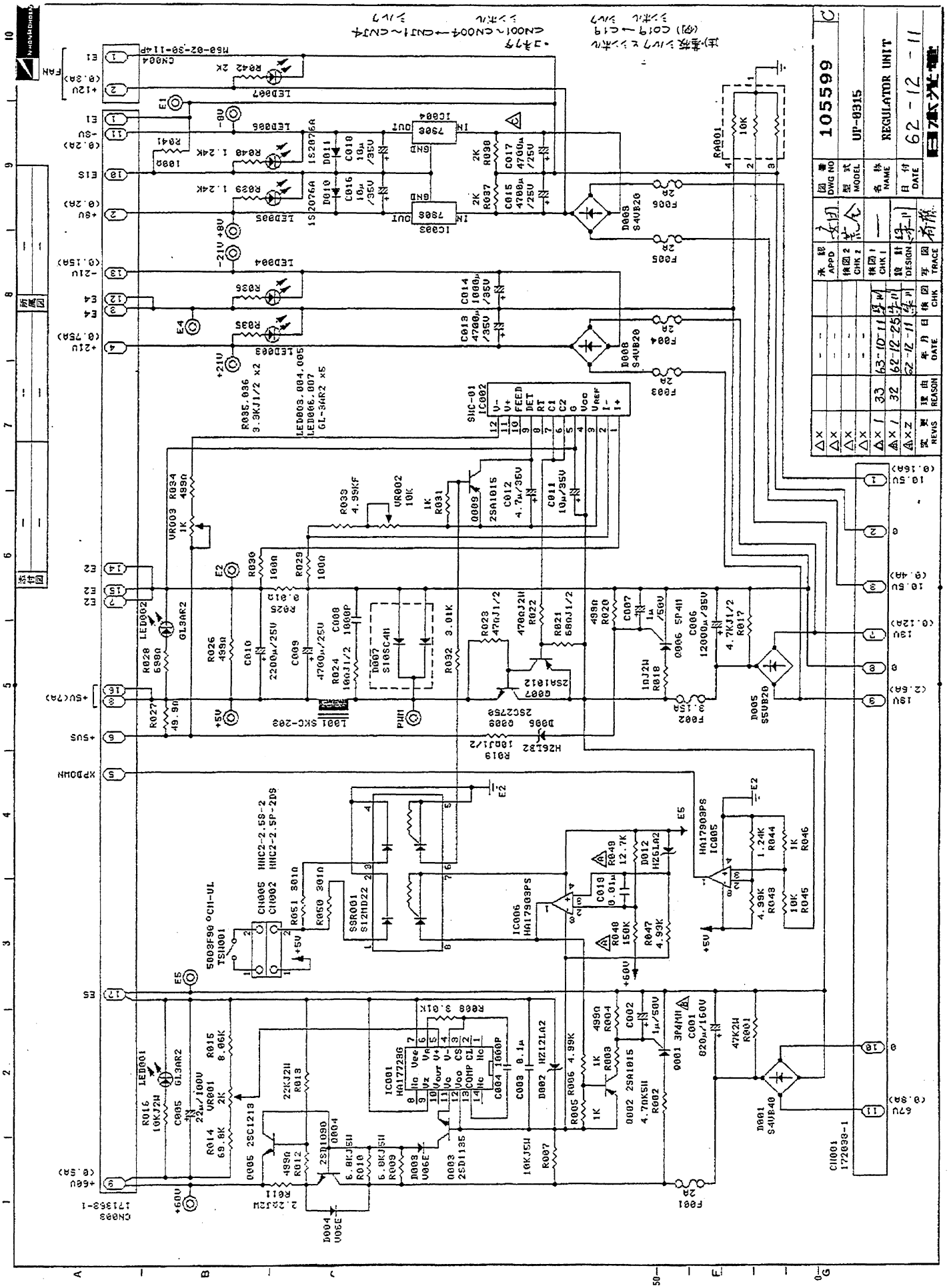
添付図	—	—	所属図	—
	—	—		—



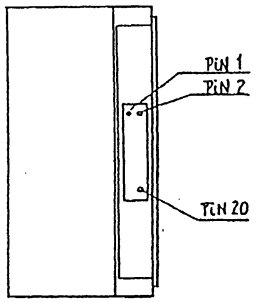
変更 REVIS	理由 REASON	年月日 DATE	検図 CHK
△×		- -	
△×		- -	
△×		- -	
△×		- -	
△×		- -	
⚠×2	22	89-1-17	荒金
⚠×1	25	63-7-19	荒金

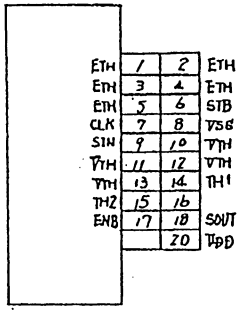
承認 APPD	永田	図番 DWG NO	105812 B
検図2 CHK 2	荒金	型式 MODEL	SC-001RK
検図1 CHK 1	宮島	名称 NAME	TRANS UNIT
設計 DESIGN	東川	日付 DATE	62 - 12 - 11
写図 TRACE	斎藤		日本光電

3


105599
UP-0315
REGULATOR UNIT
62-12-11
日本光電
CN001～CN004→CN11～CN14
CN001～CN004→CN11～CN14
CN009→CN19
CN009→CN19

THERMAL HEAD

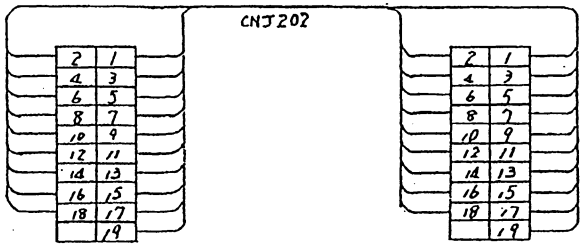


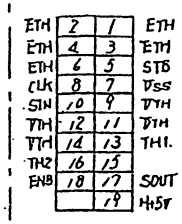


EUX-C18A8HC01

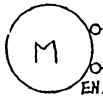
HKP-20FS02-10BT(40)

CNJ202



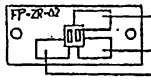


DC MOTOR



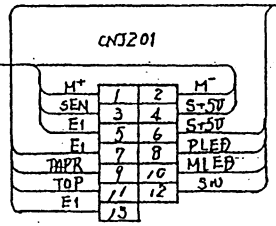
EN35-T107N1B

REVOLUTION SENSOR



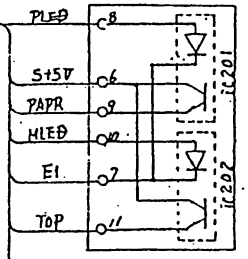
FP-2R-07

CNJ201



HKP-14FS02-7BT(60)

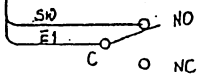
PP5215 PAPER SENSOR



ON-2173

MARK SENSOR

ON-2173



S201
SS5GL2

Paper speed

		標準速度 mm/s	
		25	50
Reduction ratio	減速比	1/20	1/20
Diameter of roller(mm)	送りローラ径(mm)	18	18
No. of teeth	回転検出歯数	50	50
Motor rev.	モータ回転数	531	1061 rpm
Rev. sensor freq.	回転検出周波数	442	884

3

△×				承認 APPD	安田	図番 DWG NO	105274
△×				検図2 CHK 2	小林	型式 MODEL	RG-712P
△×				検図1 CHK 1	—	名称 NAME	RECORDER UNIT
△×				設計 DESIGN	小川	日付 DATE	61 - 11 - 20
△×							
△×							
変更	理由	年月日	検図	原図			